CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a memory array region~~-~~ comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

a control logic region underlying the stack structure and comprising control logic devices configured to effectuate a portion of control operations for the vertically extending strings of memory cells; ~~and~~

an additional control logic region overlying the stack structure and comprising additional control logic devices configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells~~.~~;

conductive pad structures underlying the stack structure and electrically connected to the control logic devices;

additional conductive pad structures overlying the stack structure and electrically connected to the additional control logic devices; and

at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures.

2. The microelectronic device of claim 1, wherein the additional control logic devices of the additional control logic region are configured to operate at applied voltages less than or equal to about 1.4 V.

3. The microelectronic device of claim 1, wherein the additional control logic devices of the additional control logic region are configured to operate at applied voltages within a range of from about 0.7V to about 1.3 V.

4. The microelectronic device of claim 1, wherein the control logic devices and the additional control logic devices each individually comprise CMOS circuitry.

~~5. The microelectronic device of any one of claims 1 through 4, further comprising:~~

~~conductive pad structures underlying the stack structure and electrically connected to the control logic devices; and~~

~~additional conductive pad structures overlying the stack structure and electrically connected to the additional control logic devices.~~

~~6. The microelectronic device of claim 5, further comprising at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures.~~

~~7~~5. The microelectronic device of claim ~~5~~1, further comprising:

conductive line structures vertically between the stack structure and the additional conductive pad structures;

conductive routing structures vertically between the conductive line structures and the additional conductive pad structures; and

interconnect structures vertically between the conductive routing structures and the additional conductive pad structures.

~~8~~6. The microelectronic device of claim ~~7~~5, wherein:

the conductive routing structures comprise aluminum; and

the interconnect structures comprise copper.

~~9~~7. ~~The~~A microelectronic device, comprising: ~~device of any one of claims 1 through 4, further comprising an additional~~

a memory array region ~~underlying the control logic region and~~ comprising:

~~an additional~~ a stack structure comprising vertically alternating ~~additional~~ conductive structures and ~~additional~~ insulating structures; and

vertically extending strings of memory cells within the stack structure;

a control logic region underlying the stack structure and comprising control logic devices configured to effectuate a portion of control operations for the vertically extending strings of memory cells;

an additional control logic region overlying the stack structure and comprising additional control logic devices configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells; and

an additional memory array region underlying the control logic region and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures; and

additional vertically extending strings of memory cells within the additional stack structure.

~~10~~8. A method of forming a microelectronic device, comprising:

forming a first microelectronic device structure comprising:

a control logic region comprising control logic devices; and

a memory array region over the control logic region and comprising:

conductive pad structures electrically connected to the control logic devices;

a stack structure over the conductive pad structures and comprising vertically alternating conductive structures and insulating structures; ~~and~~

additional conductive pad structures overlying the stack structure;

vertically extending strings of memory cells within the stack structure; and

at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures;

forming a second microelectronic device structure comprising an additional control logic region comprising additional control logic devices; and

attaching the first microelectronic device structure to the second microelectronic device structure such that the stack structure vertically intervenes between the control logic region and the additional control logic ~~region~~region, and such that the additional conductive pad structures are electrically connected to the additional control logic devices.

~~11. The method of claim 10, wherein:~~

~~forming a first microelectronic device structure comprises forming the first microelectronic device structure to further comprise a bond pad structure over and in electrical communication with the stack structure;~~

~~forming a second microelectronic device structure comprises forming the second microelectronic device structure to further comprise an additional bond pad structure over and in electrical communication with the additional control logic devices of the additional control logic region; and~~

~~attaching the first microelectronic device structure to the second microelectronic device comprises physically contacting and heating the bond pad structure and the additional bond pad structure to form an interconnect structure therefrom.~~

~~12~~9. The method of claim ~~10~~8, further comprising selecting the additional control logic devices to comprise CMOS circuitry configured to operate at applied voltages within a range of from about 0.7 V to about 1.4 V.

~~13~~10. The method of claim ~~12~~9, further comprising selecting the control logic devices to comprise additional CMOS circuitry configured to operate at other applied voltages greater than the applied voltages effective to operate of the CMOS circuitry of the additional control logic devices.

~~14~~11. ~~The~~A method of ~~any one of claims 10 through 13, further~~forming a microelectronic device, comprising:

forming a first microelectronic device structure comprising:

a control logic region comprising control logic devices; and

a memory array region over the control logic region and comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

forming a second microelectronic device structure comprising an additional control logic region comprising additional control logic devices;

attaching the first microelectronic device structure to the second microelectronic device structure such that the stack structure vertically intervenes between the control logic region and the additional control logic region;

forming a third microelectronic device structure comprising:

a further control logic region comprising further control logic devices; and

an additional memory array region over the further control logic region and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures; and

additional vertically extending strings of memory cells within the additional stack structure; and

attaching the third microelectronic device structure to the first microelectronic device structure such that the additional stack structure vertically underlies the stack structure.

~~15. A microelectronic device, comprising:~~

~~a memory array region comprising:~~

~~a stack structure comprising a vertically alternating sequence of conductive structures and insulating structures; and~~

~~vertically extending strings of memory cells within the stack structure;~~

~~first conductive pad structures underlying the stack structure of the memory array region;~~

~~second conductive pad structures underlying the first conductive pad structures; and~~

a control logic region underlying the second conductive pad structures and comprising control logic devices comprising CMOS circuitry.

16. The microelectronic device of claim 15, wherein the first conductive pad structures are electrically connected to the second conductive pad structures by way of conducive interconnect structures vertically extending therebetween.

17. The microelectronic device of claim 15, wherein the memory array region further comprises:
conductive line structures vertically overlying the stack structure; and
at least one conductive contact structure vertically extending through the stack structure and electrically connected to at least one of the conductive line structures and at least one of the first conductive pad structures.

18. The microelectronic device of claim 17, further comprising:
additional conductive structures overlying the conductive line structures and in electrical communication with at least some of the conductive line structures; and
bond pad structures overlying and in electrical communication with the additional conductive structures.

19. The microelectronic device of claim 18, wherein:
the additional conductive structures comprise aluminum; and
the bond pad structures comprise copper.

20. The microelectronic device of any one of claims 15 through 19, further comprising passive devices underlying the control logic devices of the control logic region.

21. A method of forming a microelectronic device, comprising:
forming a first microelectronic device structure comprising a control logic region comprising control logic devices;
forming a second microelectronic device structure comprising:

a base structure; and

a memory array region overlying the base structure and comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

removing the base structure from the second microelectronic device structure; and

attaching a remainder of the second microelectronic device structure to the first microelectronic device structure such that the control logic region of the first microelectronic device structure underlies the memory array region of the second microelectronic device structure.

22. The method of claim 21, wherein:

forming a first microelectronic device structure comprises forming the first microelectronic device structure to further comprise conductive pad structures overlying the control logic devices;

forming a second microelectronic device structure comprises forming the second microelectronic device structure to further comprise additional conductive pad structures between the base structure and the stack structure of the memory array region; and

attaching a remainder of the second microelectronic device structure to the first microelectronic device structure comprises positioning the additional conductive pad structures of the second microelectronic device structure over the conductive pad structures of the first microelectronic device structure.

23. The method of claim 21, wherein forming a second microelectronic device structure comprises forming the second microelectronic device structure to further comprise an interconnect region overlying the memory array region and comprising bond pad structures.

24. The method of claim 23, further comprising:

attaching a carrier structure to the bond pad structures prior to removing the base structure from the second microelectronic device structure;

positioning the remainder of the second microelectronic device structure over the first microelectronic device structure while the carrier structure is attached to the bond pad structures; and

removing the carrier structure after attaching the remainder of the second microelectronic device structure to the first microelectronic device structure.

25. The method of any one of claims 21 through 24, further comprising forming passive devices under the control logic devices after attaching the remainder of the second microelectronic device structure to the first microelectronic device structure.

26. The method of any one of claims 21 through 24, further comprising:

forming the first microelectronic device structure to further comprise a semiconductive structure overlying the control logic region, the semiconductive structure including a conductively doped source region therein; and

forming the memory array region of the second microelectronic device structure to further comprise conductive source contacts vertically extending through the stack structure.

27. The method of claim 26, wherein attaching a remainder of the second microelectronic device structure to the first microelectronic device structure comprises positioning the conductive source contacts over and in electrical communication with the conductively doped source region of the semiconductive structure.

28. The method of claim 27, further comprising forming the semiconductive structure to comprise monocrystalline silicon.

29. The method of one of claims 27 and 28, further comprising forming the semiconductive structure over the control logic region using epitaxial growth.

30. An electronic system, comprising:

an input device;

an output device;

~~a processor device operably coupled to the input device and the output device; and~~

~~a memory device operably coupled to the processor device and comprising:~~

~~a stack structure comprising tiers each comprising a conductive structure and an insulative structure vertically neighboring the conductive structure;~~

~~vertically extending strings of memory cells within the stack structure;~~

~~control logic devices comprising CMOS circuitry underlying the stack structure, the control logic devices configured to effectuate a portion of control operations for the vertically extending strings of memory cells; and~~

~~additional control logic devices comprising additional CMOS circuitry overlying the stack structure, the additional control logic devices having relatively lower operational voltage requirements than the control logic devices and configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells.~~