

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
07 March 2024 (07.03.2024)



(10) International Publication Number
WO 2024/049617 A1

(51) International Patent Classification:

H01L 23/528 (2006.01) H01L 23/532 (2006.01)
H01L 23/535 (2006.01) H01L 27/088 (2006.01)
H01L 23/522 (2006.01)

(21) International Application Number:

PCT/US2023/029567

(22) International Filing Date:

04 August 2023 (04.08.2023)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

17/823,644 31 August 2022 (31.08.2022) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) Title: BACKSIDE CONTACTS FOR SIGNAL ROUTING

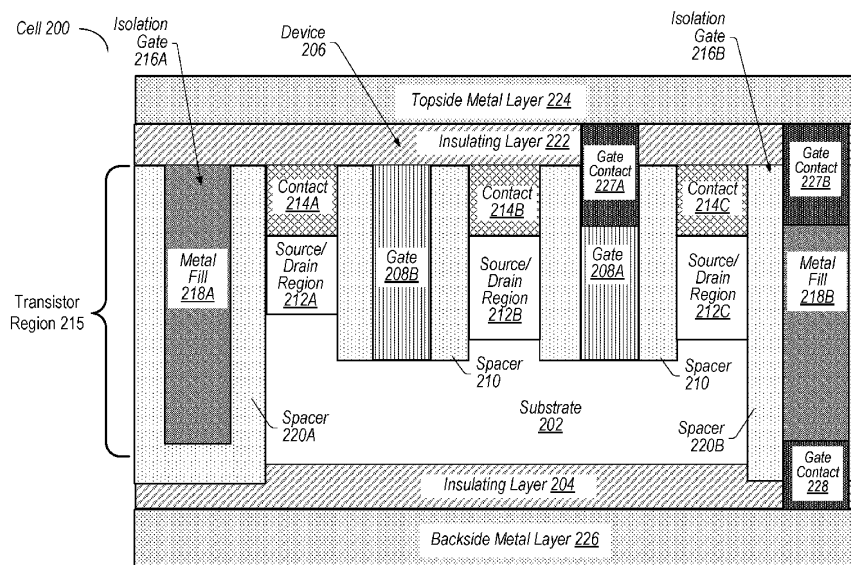


FIG. 4

(57) Abstract: A cell layout that may be implemented in FinFET devices or other FET devices is disclosed. The cell layout utilizes an isolation gate structure to provide routing between a signal input of an active gate and a backside metal layer. The isolation gate structure includes a metal fill surrounded by gate spacers. The metal fill connects between the topside layers in the device and the backside layer in the device. The metal fill may be connected to the signal input of the active gate through routing either in a topside metal layer or a metal wire placed in a topside insulating layer. The isolation gate structure can be part of any standard cell being placed at a cell boundary or inside the cell to provide access to backside signal routing. Additionally, filler cells with isolation gate structures may provide backside routing connections for adjacent functional cells.

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TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))