

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
14 July 2022 (14.07.2022)



(10) International Publication Number
WO 2022/149080 A1

(51) International Patent Classification:
G06F 15/78 (2006.01) *H01L 25/00* (2006.01)

(21) International Application Number:
PCT/IB2022/050082

(22) International Filing Date:
06 January 2022 (06.01.2022)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/135,156 08 January 2021 (08.01.2021) US

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(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,

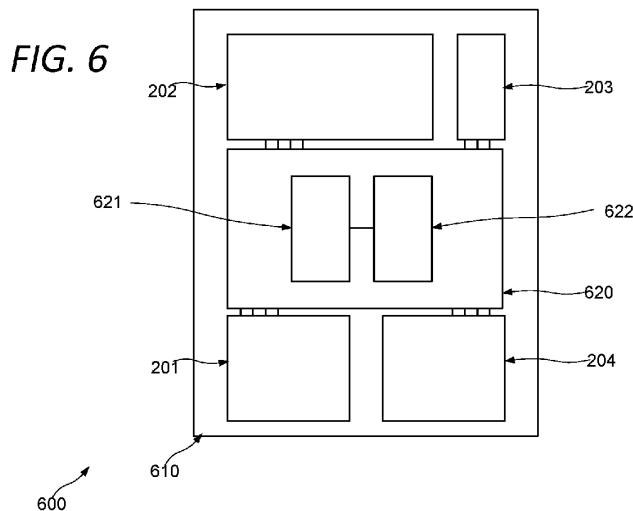
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN,
KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO,
NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW,
SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SYSTEM ON CHIP ARCHITECTURE, INTERPOSER, FPGA AND METHOD OF DESIGN



(57) Abstract: A system on chip device where the active interposer/chassis incorporates an FPGA/eFPGA, which may be used to flexibly implement interposer/chassis operations such as a network on chip communication protocols, state machines, interfaces, or data conversion, digital interfaces operations, data filtering operations, data filtering operations, and the like, or any other digital operation as required, so that analogue and mixed signals only need be addressed in dedicated chiplets.

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