

CLAIMS:

1. A method of planarizing an upper surface of a semiconductor substrate in a plasma etch chamber wherein the semiconductor substrate is supported on a support surface of a substrate support assembly located in the plasma etch chamber, the substrate support assembly including an array of independently controlled thermal control elements therein wherein the thermal control elements of the array of independently controlled thermal control elements are operable to control the spatial and temporal temperature of the support surface of the substrate support assembly to form independently controllable heater zones to correspond to a desired temperature profile across the upper surface of the semiconductor substrate such that the etch rate across the upper surface of the semiconductor substrate can be controlled during plasma etching so that the upper surface of the semiconductor substrate may be planarized, the method comprising:

analyzing the upper surface of the semiconductor substrate thereby measuring nonuniformity of surface topography of the upper surface wherein the upper surface is formed by a Si-containing material;

calculating an amount of Si-containing material to remove from the upper surface of the semiconductor substrate based upon the analysis of the upper surface to achieve a planar upper surface of the semiconductor substrate after plasma etching the semiconductor substrate for a predetermined time;

generating a temperature profile of spatial and temporal temperatures across the support surface of the substrate support assembly which corresponds to desired temperatures across the upper surface of the semiconductor substrate required to remove the calculated amount of the Si-containing material from the upper surface, wherein the etch rate of the Si-containing material forming the upper surface depends on the localized temperature thereof;

inserting the semiconductor substrate into the plasma etch chamber;

supplying process gas into the chamber and energizing the process gas into a plasma state; and

planarizing the upper surface of the semiconductor substrate by plasma etching the upper surface of the semiconductor substrate while powering the array of independently controlled thermal control elements to achieve the desired temperature profile across the upper surface of

the semiconductor substrate thereby removing the calculated amount of the Si-containing material from the upper surface of the semiconductor substrate and achieving a planar upper surface of the semiconductor substrate.

2. The method of Claim 1, wherein

(a) the Si-containing material is Si, and the process gas used to perform the plasma etch is HBr; or

(b) the Si-containing material is Si, and the process gas used to perform the plasma etch is HBr and O₂; or

(c) the Si-containing material is Si, and the process gas used to perform the plasma etch is C₄F₈, NF₃, and CH₂F₂; or

(d) the Si-containing material is SiN, and the process gas used to perform the plasma etch is CH₃F; or

(e) the Si-containing material is SiN, and the process gas used to perform the plasma etch is C₄F₈, NF₃, and CH₂F₂; or

(f) the Si-containing material is SiN, and the process gas used to perform the plasma etch is C₄F₈, NF₃, and He; or

(g) the Si-containing material is SiN, and the process gas used to perform the plasma etch is C₄F₈, NF₃, He, and CH₂F₂; or

(h) the Si-containing material is SiN, and the process gas used to perform the plasma etch is C₄F₈, NF₃, He, CH₂F₂, and Cl₂; or

(i) the Si-containing material is SiO_x, wherein x is greater than or equal to 1, and the process gas used to perform the plasma etch is CH₂F₂ and CF₄; or

(j) the Si-containing material is SiO_x, wherein x is greater than or equal to 1, and the process gas used to perform the plasma etch is C₄F₈, NF₃, and He; or

(k) the Si-containing material is SiO_x, wherein x is greater than or equal to 1, and the process gas used to perform the plasma etch is C₄F₈, NF₃, He, CH₂F₂, O₂, and CF₄; or

(l) the Si-containing material is SiO_x, wherein x is greater than or equal to 1, and the process gas used to perform the plasma etch is C₄F₈, NF₃, He, and O₂; or

(m) the Si-containing material is SiO_x, wherein x is greater than or equal to 1, and the process gas used to perform the plasma etch is C₄F₈, NF₃, He, and CF₄.

3. The method of Claim 1, further comprising depositing a layer of the Si-containing material on the upper surface of the semiconductor substrate prior to inserting the semiconductor substrate in the plasma etch chamber wherein the plasma etch rate of the deposited Si-containing material depends on a localized temperature thereof; and/or subjecting the upper surface to a chemical mechanical planarization process prior to inserting the semiconductor substrate in the plasma etch chamber.
4. The method of Claim 1, wherein the upper surface of the semiconductor surface is formed by more than one material selected from the group consisting of Si, SiN, and SiO_x, wherein x is greater than or equal to 1, the method further comprising optimizing the composition of the process gas such that each material forming the upper surface of the semiconductor substrate is etched at a 1:1 ratio during plasma processing.
5. The method of Claim 1, wherein the temperatures of the independently controllable heater zones across the support surface of the substrate support assembly can achieve temperatures across the support surface of about 20° C to about 90° C.
6. The method of Claim 1, further comprising maintaining a pressure in the chamber at about 5 mTorr to 90 mTorr.
7. The method of Claim 1, wherein the process gas used to perform the plasma etching includes C₄F₈, He, CF₄, CHF₃, or a combination thereof, and wherein the plasma etching forms a passivation layer on portions of the upper surface of the semiconductor substrate.
8. The method of Claim 1, wherein the topography of the upper surface of the semiconductor substrate is analyzed using a light scattering or interferometry technique.
9. The method of Claim 1, wherein the desired temperature profile and the independently controllable heater zones are formed at a spatial frequency independent of the spatial frequency of the thermal control elements of the array of independently controlled thermal control elements included in the substrate support assembly.
10. The method of Claim 1, further comprising controlling the array of independently controlled thermal control elements to form at least 100 independently controllable heater zones across the support surface such that the etch rate of portions of the upper surface of the semiconductor substrate corresponding to each formed independently controllable heater zone is about 0 to 5 nm/min/°C.

11. The method of Claim 1, wherein the method is performed by a software algorithm.
12. A non-transitory computer readable medium comprising program instructions for performing the method of Claim 1.
13. A control system configured to control processes performed by the plasma etch chamber comprising the non-transitory computer readable medium of Claim 12.
14. A method of planarizing an upper surface of a semiconductor substrate in a plasma etch chamber wherein the upper surface of the semiconductor substrate is formed by a Si-containing material, the method comprising:
 - analyzing the upper surface of the semiconductor substrate so as to determine nonuniformity of surface topography of the upper surface;
 - calculating an amount of the Si-containing material to remove from the upper surface of the semiconductor substrate based upon the analysis of the upper surface;
 - supporting the semiconductor substrate on a support surface of a substrate support assembly that includes an array of independently controlled thermal control elements therein wherein the thermal control elements of the array of independently controlled thermal control elements are operable to control the spatial and temporal temperature of the support surface of the substrate support assembly to form independently controllable heater zones;
 - controlling the independently controllable heater zones to correspond to a desired temperature profile across the upper surface of the semiconductor substrate for the analyzed surface topography wherein the etch rate across the upper surface of the semiconductor substrate during plasma etching depends on a localized temperature thereof and wherein the desired temperature profile is determined such that the upper surface of the semiconductor substrate is planarized within a predetermined time period; and
 - plasma etching the semiconductor substrate for the predetermined time period thereby planarizing the upper surface thereof to remove the calculated amount of the Si-containing material from the upper surface of the semiconductor substrate, wherein the process gas used to perform the plasma etch includes HBr, C₄F₈, NF₃, CH₂F₂, CF₄, CH₃F, O₂, He, Cl₂, or a combination thereof.

15. The method of Claim 14, wherein the desired temperature profile is created before supporting the semiconductor substrate on the support surface of the substrate support assembly in the plasma etch chamber.
16. The method of Claim 15, wherein the desired temperature profile and the independently controllable heater zones are controlled at a spatial frequency independent of the spatial frequency of the thermal control elements of the array of independently controlled thermal control elements included in the substrate support assembly.
17. The method of Claim 14, further comprising depositing a layer of the Si-containing material on the upper surface of the semiconductor substrate before supporting the semiconductor substrate on the support surface of the substrate support assembly in the plasma etch chamber.
18. The method of Claim 14, further comprising, controlling the array of independently controlled thermal control elements to form at least 100 independently controllable heater zones across the support surface such that the etch rate of portions of the upper surface of the semiconductor substrate corresponding to each formed independently controllable heater zone is about 5 nm/min/°C or less.
19. The method of Claim 14, wherein the temperatures of the independently controllable heater zones across the support surface of the substrate support assembly can achieve temperatures across the support surface of about 20° C to about 90° C, and/or the pressure in the chamber is maintained at about 5 mTorr to 90 mTorr.
20. The method of claim 14, wherein the array of independent control elements includes at least 50 thermal control elements.