disclosure. Hereinafter, descriptions repetitive to the above description will be omitted.

[0051] Referring to FIG. 3A, a memory cell MC is positioned between a row line 30 and a column line 36. The memory cell MC includes a first electrode 31, a second electrode 33_M, and an active layer interposed between the first electrode 31 and the second electrode ~~layer~~ 33_M. The active layer may be configured as a switching layer 32. The switching layer 32 may be interposed between the first electrode 31 and the second electrode 33_M. In addition, at least one of the first electrode 31 and the second electrode 33_M may be in direct contact with the switching layer 32.

[0052] At least one of the first electrode 31 and the second electrode 33_M may include a stack of conductive layers. For example, one of the first electrode 31 and the second electrode 33_M, which is formed after forming the switching layer 32 may include the stack of conductive layers. In an embodiment, an electrode formed on the switching layer 32 may include the stack of conductive layers.

[0053] In the embodiment of FIG. 3A, it is assumed that the second electrode 33_M includes the stack of conductive layers. The second electrode 33_M may be formed to be in direct contact with the switching layer 32. In addition, the second electrode 33_M may be formed by alternately repeating an

(micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multi-media card (MMC), an embedded MMC (eMMC), and a compact flash (CF) card.

[00129] The storage device 1310 may include a non-volatile memory that semi-permanently stores data. Here, the non-volatile memory may include a read only memory (ROM), a NOR flash memory, a NAND flash memory, a phase change random access memory (PRAM), a resistive random access memory (RRAM), a magnetic random access memory (MRAM), and the like.

[00130] The controller 1320 may control exchange of data between the storage device 1310 and the interface 1330. To this end, the controller 1320 may include a processor 1321 that performs an operation or the like for processing commands input through the interface 1330 from the outside of the data storage system 1300.

[00131] The interface 1330 is for exchanging an instruction, data, and the like between the data storage system 1300 and an external device. When the data storage system 1300 is a card type, the interface 1330 may be compatible with an interface used in a device such as a universal serial bus (USB) memory, a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital high capacity

first active layer interposed between the first electrode and the second electrode. A conductive layer that is in contact with the first active layer, among the conductive layers of the second electrode may have a thickness of 10 to 100 Å. Therefore, a read operation characteristic of the memory 1410 may be improved. As a result, a read operation characteristic of the memory system 1400 may be improved.

[00136] In addition, the memory of the present embodiment may include a read only memory (ROM), a NOR flash memory, a NAND flash memory, a phase change random access memory (PRAM), a resistive random access memory (RRAM), a magnetic random access memory (MRAM), and the like having a non-volatile characteristic.

[00137] The memory controller 1420 may control exchange of data between the memory 1410 and the interface 1430. To this end, the memory controller 1420 may include a processor 1421 for processing and operating commands input through the interface 1430 from the outside of the memory system 1400.

[00138] The interface 1430 is for exchanging an instruction, data, and the like between the memory system 1400 and an external device. The interface 1430 may be compatible with an interface used in a device such as a universal serial bus (USB) memory, a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital

WHAT IS CLAIMED IS:

1. A method of manufacturing an electronic device including a semiconductor memory, the method comprising:

forming a first active layer;

forming a first electrode material over the first active layer;

performing a heat treatment process on the first electrode material and the first active layer; and

forming a second electrode material over the heat-treated first electrode material,

wherein one or more voids are generated in the first active layer when the first electrode material is formed, and a number of voids, or a size of each of the voids, or both are reduced by the heat treatment process.

2. The method of claim 1, wherein the second electrode material is in direct contact with the first electrode material.

3. The method of claim 1, wherein the first electrode material is in direct contact with the first active layer.

4. The method of claim 1, wherein the heat treatment process is a first heat treatment process, the method further comprising:

performing a second heat treatment process on the second electrode material; and

forming a third electrode material over the heat-treated second electrode material.

5. The method of claim 4, wherein the third electrode material is in direct contact with the second electrode material.

6. ~~The method of claim 1, further comprising:~~ A method of manufacturing an electronic device including a semiconductor memory, the method comprising:

forming a first active layer;

forming a first electrode material over the first active layer;

performing a heat treatment process on the first electrode material and the first active layer; and

forming a second electrode material over the heat-treated first electrode material; and

etching a surface of the second electrode material.

7. The method of claim 6, further comprising:

forming a third electrode material over an etched surface of the second electrode material.

~~8. The method of claim 1, wherein one or more voids are generated in the first active layer when the first electrode material is formed, and a number of voids, or a size of each of the voids, or both are reduced by the heat treatment process.~~

8~~9~~. The method of claim 1, wherein the first active layer is configured as a switching layer.

9~~10~~. The method of claim 1, wherein the first active layer is configured as a variable resistance layer.

10~~1~~. The method of claim 1, wherein the first active layer is configured as a switching layer or a variable resistance layer.

11~~2~~. The method of claim 1, wherein the heat treatment process is a first heat treatment process, the method further comprising:

forming a second active layer over the second electrode material;

forming a third electrode material over the second active layer;

performing a second heat treatment process on the third electrode material; and

forming a fourth electrode material over the heat-treated

third electrode material.

123. The method of claim 112, further comprising:

performing a third heat treatment process on the fourth electrode material; and

forming a fifth electrode material over the heat-treated fourth electrode material.

134. The method of claim 112, further comprising:

etching a surface of the fourth electrode material.

145. The method of claim 134, further comprising:

forming a fifth electrode material over the etched surface of the fourth electrode material.

156. The method of claim 112, wherein the first active layer is configured as a switching layer and the second active layer is configured as a variable resistance layer.

167. The method of claim 11, wherein the first active layer is configured as a variable resistance layer and the second active layer is configured as a switching layer.

178. The method of claim 1, wherein a thickness of the

first electrode material is in a range from 10 Å to 100 Å.

189. The method of claim 1, wherein the heat treatment process is performed at a temperature that reduces ~~a~~the number of voids in the first active layer, or ~~a~~ the size of each of the voids, or both.

1920. The method of claim 1, wherein the heat treatment process is performed at a temperature in a range from 100 ℃ to 350 ℃.

201. The method of claim 1, wherein the heat treatment process is performed during a time interval from 1 minute to 20 minutes.

212. The method of claim 1, wherein the heat treatment process is performed at a pressure of 0.1 mTorr to 10 mTorr.

223. The method of claim 1, wherein the heat treatment process is performed in an Ar atmosphere, an N_2 atmosphere, or a vacuum.

234. The method of claim 1, wherein a thickness of the first electrode material is in a range from 10 Å to 100 Å, and the

heat treatment process is performed at a temperature in a range from 100 °C to 350 °C and a pressure in a range from 0.1 mTorr to 10 mTorr for 1 minute to 20 minutes.

245. An electronic device including a semiconductor memory, wherein the semiconductor memory comprises:

a first electrode;

a second electrode including a plurality of conductive layers; and

a first active layer interposed between the first electrode and the second electrode, and

wherein the plurality of conductive layers of the second electrode include a first conductive layer that is in contact with the first active layer, the first conductive layer having a thickness in a range from 10 Å to 100 Å,

wherein the second electrode is a carbon electrode.

256. The electronic device of claim 245, wherein the first active layer is configured as a switching layer.

267. The electronic device of claim 245, wherein the first active layer is configured as a variable resistance layer.

278. The electronic device of claim 245, wherein the first

active layer is configured as a switching layer or a variable resistance layer.

289. The electronic device of claim 245, wherein the plurality of conductive layers of the second electrode are a first plurality of conductive layers, and

wherein the semiconductor memory further comprises:

a third electrode including a second plurality of conductive layers; and

a second active layer interposed between the second electrode and the third electrode.

2930. The electronic device of claim 289, wherein the second plurality of the conductive layers include a second conductive layer that is in contact with the second active layer, the second conductive layer having a thickness in a range from 10 Å to 100 Å.

301. The electronic device of claim 289, wherein the first active layer is configured as a switching layer and the second active layer is configured as a variable resistance layer.

312. The electronic device of claim 289, wherein the first active layer is configured as a variable resistance layer and the

second active layer is configured as a switching layer.

~~33. The electronic device of claim 25, wherein the second electrode is a carbon electrode.~~