CLAIMS

1. A semiconductor device, comprising: a substrate; a plurality of channel structures disposed over the substrate, the plurality of channel structures of a first field effect transistor (FET); one or more shallow trench isolation (STI) trenches, each STI trench formed between a corresponding pair of channel structures of the plurality of channel structures and comprising: a bottom region filled with a lower quality oxide; and a top region formed above the bottom region and filled with a higher quality oxide; a gate of the first FET disposed over the plurality of channel structures and the top region of each STI trench of the one or more STI trenches; a source of the first FET disposed on a first side the plurality of channel structures and the one or more STI trenches; and a drain of the first FET disposed on a second side of the plurality of channel structures and the one or more STI trenches opposite of the first side, wherein the top region of each STI trench of the one or more STI trenches is filled with the higher quality oxide such that a void is not formed in the top region, and wherein the top region of each STI trench of the one or more STI trenches electrically isolates the gate from the source and the drain.

2. The semiconductor device of claim 1, wherein the lower quality oxide comprises a high aspect ratio oxide configured to fill an area having a height to width ratio of greater than ten-to-one (10:1).

3. The semiconductor device of claim 2, wherein the higher quality oxide comprises a low aspect ratio oxide configured to fill an area having a height to width ratio of less than ten-to-one (10:1).

4. The semiconductor device of claim 3, wherein the lower quality oxide is selected from the group consisting of: spin-on-dielectric oxide (SOD); and flowable chemical vapor deposition (CVD) (FCVD) oxide.

5. The semiconductor device of claim 4, wherein the higher quality oxide comprises silicon oxide.

6. The semiconductor device of claim 1, wherein: each channel structure of the plurality of channel structures comprises a Fin; and the first FET comprises a FinFET.

7. The semiconductor device of claim 1, wherein the first FET comprises a nanowire FET.

8. The semiconductor device of claim 1 integrated into an integrated circuit (IC).

9. The semiconductor device of claim 1 integrated into a device selected from the group consisting of: a set top box; an entertainment unit; a navigation device; a communications device; a fixed location data unit; a mobile location data unit; a mobile phone; a cellular phone; a smart phone; a tablet; a phablet; a server; a computer; a portable computer; a desktop computer; a personal digital assistant (PDA); a monitor; a computer monitor; a television; a tuner; a radio; a satellite radio; a music player; a digital music player; a portable music player; a digital video player; a video player; a digital video disc (DVD) player; a portable digital video player; and an automobile.

10. A semiconductor device, comprising: a substrate; a plurality of channel structures

disposed over the substrate, the plurality of channel structures of a first field effect transistor (FET); one or more shallow trench isolation (STI) trenches, each STI trench formed between a corresponding pair of channel structures of the plurality of channel structures and comprising: a bottom region filled with a lower quality oxide; and a top region formed above the bottom region and filled with a higher quality oxide; a gate of the first FET disposed over the plurality of channel structures and the top region of each STI trench of the one or more STI trenches; a source of the first FET disposed on a first side of the plurality of channel structures and the one or more STI trenches; a drain of the first FET disposed on a second side of the plurality of channel structures and the one or more STI trenches opposite of the first side; a second plurality of channel structures disposed over the substrate, the second plurality of channel structures of a second FET; one or more STI trenches, each STI trench formed between a corresponding pair of channel structures of the second plurality of channel structures of the second FET and comprising: a bottom region filled with the lower quality oxide; and a top region formed above the bottom region and filled with the higher quality oxide; and a deep STI trench formed between the first FET and the second FET and configured to electrically isolate the first FET and the second FET.

11. The semiconductor device of claim 10, wherein the deep STI trench is filled with the higher quality oxide.

12. The semiconductor device of claim 10, wherein the deep STI trench comprises: a bottom region filled with the lower quality oxide; and a top region filled with the higher quality oxide.

13. A method for manufacturing semiconductor devices employing Field Effect Transistors (FETs) with multiple channel structures without shallow trench isolation (STI) void-induced electrical shorts, comprising: providing a substrate comprising a plurality of channel structures of a first field effect transistor (FET) disposed over the substrate, and one or more STI trenches, each STI trench formed between a corresponding pair of channel structures of the plurality of channel structures; disposing a lower quality oxide in a bottom region of each STI trench; disposing a higher quality oxide in a top region of each STI trench above the bottom region, wherein the higher quality oxide fills voids formed in the lower quality oxide that are adjacent to the top region; disposing a gate of the first FET over the plurality of channel structures and the top region of each STI trench of the one or more STI trenches; disposing a source of the first FET on a first side the plurality of channel structures and the one or more STI trenches; disposing a drain of the first FET on a second side of the plurality of channel structures and the one or more STI trenches opposite of the first side, disposing a hard mask over the plurality of channel structures such that an opening is formed over a first subset of channel structures and the hard mask covers a second subset of channel structures and a third subset of channel structures disposed on either side of the first subset of channel structures; and etching the first subset of channel structures and the substrate to form a deep STI trench between the second subset of channel structures and the third subset of channel structures, wherein the second subset of channel structures are of the first FET and the third subset of channel structures are of a second FET.

14. The method of claim 13, further comprising disposing the higher quality oxide in the deep STI trench.

15. The method of claim 13, further comprising: disposing the lower quality oxide in the deep STI trench; etching the lower quality oxide in the deep STI trench to a top level of a bottom

region of the deep STI trench; and disposing the higher quality oxide in a top region of the deep STI trench over the lower quality oxide.

16. The method of claim 13, further comprising annealing the lower quality oxide.

17. The method of claim 13, wherein disposing the lower quality oxide comprises disposing a high aspect ratio oxide configured to fill an area having a height to width ratio of greater than ten-to-one (10:1).

18. The method of claim 17, wherein disposing the higher quality oxide comprises disposing a low aspect ratio oxide configured to fill an area having a height to width ratio of less than ten-to-one (10:1).

19. The method of claim 13, further comprising etching the lower quality oxide in each STI trench to a top level of the bottom region of each STI trench.