

ELECTRICAL BRIDGE PACKAGE WITH INTEGRATED OFF-BRIDGE PHOTONIC CHANNEL INTERFACE

RELATED APPLICATIONS

[001] This application claims priority to and the benefit of United States Provisional Patent Application Serial No. 63/437,639, filed January 6, 2023 and this application claims priority to and the benefit of United States Provisional Patent Application Serial No. 63/437,641, filed January 6, 2023. This application also claims priority to United States Patent Application No. 18/217,898, Filed July 3, 2023, which is a continuation-in-part of United States Patent Application No. 18/076,196, filed December 6, 2022, and is a continuation-in-part of United States Patent Application No. 18/076,210, filed December 6, 2022, and this application claims the priority to and benefit of United States Provisional Patent Application No. 63/392,475, filed July 26, 2022. All of these applications are incorporated by reference in their entireties.

BACKGROUND

[002] Demands for artificial intelligence (AI) computing, such as machine learning (ML) and deep learning (DL), are increasing faster than they can be met by increases in available processing capacity. This rising demand and the growing complexity of AI models contribute to the need to connect many chips into a system where the chips can send data between each other with low latency and at high speed.

BRIEF SUMMARY

[003] This summary is provided to introduce a selection of concepts that are further described below in the detailed description. This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

[004] Additional features and advantages of embodiments of the disclosure will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by the practice of such embodiments. The features and advantages of such embodiments may be realized and obtained by means of the instruments and combinations particularly pointed out in the appended claims. These and other features will become more fully apparent from the following description and appended claims, or may be learned by the practice of such embodiments as set forth hereinafter.

[005] At least one implementation of the techniques described herein relates to a circuit package, including: a photonic interposer; a second interposer; a die partially overlapping and connected to both the photonic interposer and the second interposer.

[006] In some implementations, the die is a first die. In some implementations, the die is in an electrical coupling with both the photonic interposer and the second interposer. In some implementations, the die includes an analog-mixed signal portion to enable a first processing element to transmit and/or receive data using the photonic interposer and an electronic portion to enable a second processing element to transmit and/or receive data using the second interposer.

[007] In some implementations, the die partially vertically overlaps both the photonic interposer and the second interposer. In some implementations, the second interposer is a non-photonic interposer. In some implementations, the second interposer is an electrical interposer.

[008] In some implementations, the second interposer is a second photonic interposer. In some implementations, one or more of the photonic interposer and the second interposer are photonic integrated circuits. In some implementations, one or more of the photonic interposer and the second interposer are photonic integrated circuits. In some implementations, the second interposer is an SI interposer. In some implementations, the second interposer is an SI bridge.

[009] In some implementations, the photonic interposer and the second interposer are separated by a mold. In some implementations, the photonic interposer and the second interposer are adjacent. In some implementations, the photonic interposer and the second interposer are directly adjacent. In some implementations, the photonic interposer and the second interposer abut. In some implementations, the photonic interposer and the second interposer do not vertically overlap.

[010] In some implementations, the die is an ASIC die. In some implementations, the die is a processor die. In some implementations, the die is an ARM processor die. In some implementations, the die is an image processor die.

[011] In some implementations, one or more of the photonic interposer and the second interposer are formed of silicon or a silicon alloy. In some implementations, the photonic interposer and the second interposer are laterally surrounded by a mold. In some implementations, the mold formed of silicon or a silicon alloy. In some implementations, the mold includes a material that matches a thermal expansion of one or more of the photonic interposer and the second interposer.

[012] In some implementations, the second interposer is a mold. In some implementations, the second interposer includes a through mold via. In some implementations, the second interposer includes a bond via array.

[013] In some implementations, the circuit package further includes a second die. In some implementations, the second die does not vertically overlap the photonic interposer. In some implementations, the second die includes general purpose memory. In some implementations, the second die includes a processor. In some implementations, the processor is one or more of an image processor, a video processor, and a general purpose processor. In some implementations, the second die includes high bandwidth memory. In some implementations, the high bandwidth memory is HBM3.

[014] In some implementations, the circuit package further includes a third die. In some implementations, the third die includes one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor. In some implementations, the third die does not vertically overlap the photonic interposer. In some implementations, the third die vertically overlaps the photonic interposer. In some implementations, the third die vertically overlaps the photonic interposer and the second interposer.

[015] In some implementations, the circuit package further includes a fourth die. In some implementations, the circuit package further includes a second photonic interposer. In some implementations, the circuit package further includes a third photonic interposer. In some implementations, the circuit package further includes a third interposer. In some implementations, the circuit package further includes a substrate.

[016] In some implementations, one or more dies (e.g., the die, the second die, the third die, the fourth die) include one or more processing elements. In some implementations, the one or more processing elements are one or more of a CPU, a GPU, a TPU, a tensor engine, a neural network, an AI accelerator, a router, a memory, a switch, a controller, an ASIC, an image processor, a video processor, and a bus.

[017] In some implementations, one or more components of the circuit package described or claimed herein are connected to the substrate. In some implementations, the circuit package further includes a redistribution layer. In some implementations, the redistribution layer electrically connects the die to one or more of the second die, the third die, or the fourth die as described or claimed herein. In some implementations, the redistribution layer electrically connects to a top surface of the die to a top surface of the one or more of the second die, the third die, or the fourth die as described or claimed herein.

In some implementations, the redistribution layer electrically connects to a bottom surface of the die to a top surface of the one or more of the second die, the third die, or the fourth die as described or claimed herein. In some implementations, the redistribution layer is about ten microns line per space. In some implementations, the redistribution layer is less than two microns thick in the vertical direction. In some implementations, the redistribution layer is less than two layers thick in the vertical direction.

[018] In some implementations, the circuit package further includes one or more optical elements. In some implementations, the one or more optical elements include fiber array units. In some implementations, the optical elements are optically connected to one or more of the photonic interposer, the second interposer, the second photonic interposer, the third interposer, and the third photonic interposer as described or claimed herein. In some implementations, any redistribution layer material on the one or more of the photonic interposer, the second interposer, the second photonic interposer, the third interposer, and the third photonic interposer as described or claimed herein vertically below at least a portion of the one or more optical elements are omitted or removed.

[019] At least one implementation of the techniques described herein relates to a circuit package, including: a photonic interposer, an electrical interposer, and a first die in an electrical coupling with both the photonic and electrical interposers. The first die includes an analog-mixed signal portion to enable a first processing element therein to transmit and/or receive data using the photonic interposer and an electronic portion to enable a second processing element therein to transmit and/or receive data using the electrical interposer. The circuit package includes a plurality of vias in the electrical interposer to enable the second processing element to transmit and receive data to one or more additional dies in electrical coupling with the electrical interposer.

BRIEF DESCRIPTION OF THE DRAWINGS

[020] In order to describe the manner in which the above-recited and other features of the disclosure can be obtained, a more particular description will be rendered by reference to specific implementations thereof which are illustrated in the appended drawings. For better understanding, the like elements have been designated by like reference numbers throughout the various accompanying figures. While some of the drawings may be schematic or exaggerated representations of concepts, at least some of the drawings may be drawn to scale. Understanding that the drawings depict some example implementations,

the implementations will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[021] Figure 1 is a top view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

5 [022] Figure 2 is a cutaway side view of the embodiment of a circuit package shown in Figure 1, according to at least one embodiment of the present disclosure.

[023] Figure 3 is a top view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

10 [024] Figure 4-1 is a cutaway side view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

[025] Figure 4-2 is a cutaway side view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

[026] Figure 4-3 is a cutaway side view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

15 [027] Figure 5 is a cutaway side view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

[028] Figure 6 is a top view of an embodiment of a circuit package, according to at least one embodiment of the present disclosure.

20 [029] Figure 7 is an embodiment of a method of manufacturing a circuit package, according to at least one embodiment of the present disclosure.

[030] Figure 8 is an embodiment of a method of manufacturing a circuit package, according to at least one embodiment of the present disclosure.

[031] Figure 9 is an embodiment of a method of manufacturing a circuit package, according to at least one embodiment of the present disclosure.

25 [032] Figure 10 is an embodiment of a method of manufacturing a circuit package, according to at least one embodiment of the present disclosure.

[033] FIG. 11 is an embodiment of a method of manufacturing a circuit package, according to at least one embodiment of the present disclosure.

30 DETAILED DESCRIPTION

[034] The present disclosure is related to circuit packages and methods of manufacturing circuit packages. More specifically, the present disclosure is related to one or more circuit packages with a die that connects to a photonic interposer and a second interposer and methods of manufacturing the same.

[035] Photonic interposers are very expensive to manufacture and/or purchase. At least one embodiment described and/or claimed herein reduces the overall cost of a circuit package by reducing the size of the photonic interposer. For example, dies that do not need to be connected to a photonic interposer may be connected to a non-photonic interposer (e.g., an electric interposer) while one or more dies that do need to be connected to the photonic interposer may be connected to both the photonic interposer and a second interposer (e.g., the non-photonic interposer or a second photonic interposer). Using a second interposer may reduce the overall cost of the circuit package as two smaller interposers may be less expensive to manufacture and/or purchase than a single large interposer. Using a non-photonic interposer with a photonic interposer may reduce the cost even more, as the costs of a non-photonic interposer is less expensive to manufacture and/or purchase than a photonic interposer of the same size.

[036] Figure 1 is a top view of an embodiment of an electrical bridge package with integrated off-bridge photonic channel interface (as used herein, circuit package 100). Figure 2 is a cutaway side view of the embodiment of a circuit package shown in Figure 1. The circuit package 100 may be manufactured according to one or more methods described herein. For example, the circuit package 100 may be manufactured by the method 600 shown in Figure 7, by the method 700 shown in Figure 8, by the method 800 shown in Figure 9, and by the method 900 shown in Figure 10.

[037] The circuit package 100 includes a photonic interposer 110, a second interposer 120, and a die 130 partially overlapping and connected to both the photonic interposer 110 and the second interposer 120. As shown, the die 130 vertically overlaps both the photonic interposer 110 and the second interposer 120. In accordance with at least one embodiment of the present disclosure, the photonic interposer 110 may be any type of photonic interposer. For example, the photonic interposer 110 may include a photonic integrated circuit.

[038] In some embodiments, the second interposer 120 may be a photonic interposer (e.g., second photonic interposer). One or more photonic interposers (e.g., photonic interposer 110 or second interposer 120), in some embodiments, are photonic integrated circuits. In some embodiments, the second interposer 120 is a non-photonic interposer. Non-photonic interposers, in some embodiments, may include one or more of a silicon (SI) interposer, an SI bridge, electronic interposers, other interposer materials, other bridge materials, or combinations thereof. In some embodiments, the photonic interposer 110 and the second interposer 120 are formed of silicon or a silicon alloy.

[039] In some embodiments, the photonic interposer 110 and the second interposer 120 are adjacent each other. For example, the photonic interposer 110 and the second interposer 120 may be only separated by a space or a spacer (e.g., a mold). The photonic interposer 110 and the second interposer 120, in some embodiments, are directly adjacent.

5 For example, the photonic interposer 110 and the second interposer 120 may be only separated by a space. In some embodiments, the photonic interposer 110 and the second interposer 120 abut each other. For example, the photonic interposer 110 and the second interposer 120 may directly touch.

[040] As shown in Figure 1, the photonic interposer 110 and the second interposer 10 120 do not vertically overlap each other. In some embodiments, the photonic interposer 110 and the second interposer 120 at least partially vertically overlap each other.

[041] The die 130 may include any applicable integrated circuit, such as an ASIC, a processor, and ARM processor, an image processor, a tensor engine, a neural-compute engine, a video processor, a general-purpose processor, or combinations thereof. As shown, 15 the die 130 may be larger in at least one dimension than the photonic interposer 110. As shown, the die 130 is larger in the x-direction than the photonic interposer 110. In some embodiments, the die 130 is larger than the photonic interposer 110 in two or more dimensions.

[042] The die 130 may include various portions. For example, the die 130 may include 20 an analog-mixed signal portion 132-1 and/or an electronic portion 132-2. The analog-mixed signal portion 132-1 may include a first processing element 134-1. The first processing element 134-1 may transmit and/or receive data using the photonic interposer 110. For example, the first processing element 134-1 may transmit and/or receive data photonically using the photonic interposer 110. The electronic portion 132-2 may include a second 25 processing element 134-2. The second processing element 134-2 may transmit and/or receive data using the second interposer 120. For example, the second interposer 120 may be an electrical-only interposer (e.g., not a photonic interposer) such that the second processing element 134-2 may transmit and/or receive data electrically using the second interposer 120.

30 [043] In accordance with at least one embodiment of the present disclosure, the first processing element 134-1 may include processing elements that are configured to communicate with elements of the photonic interposer 110. In some embodiments, information may be communicated with the photonic interposer 110 through a photonic channel of the photonic interposer 110 and is received at an optical-to-electrical (OE)

interface between the photonic interposer 110 and analog-mixed signal portion 132-1. The OE interface may be implemented, for example, by a photodetector (e.g., photodiode) in the photonic interposer 110 to convert the optical signal into an electronic signal, in conjunction with related electronic circuitry in the analog-mixed signal portion 132-1, which may include, e.g., a transimpedance amplifier (TIA), optional gain control to normalize the signal level, and slicer to extract the bit stream. The information can then be buffered in electronic form in a register such as “first in first out” (FIFO) register. Similarly, an EO interface can be used in the same photonic channel to send data via the photonic interposer.

[044] The first processing element 134-1 may communicate with the elements of the photonic interposer 110 using any type of connection. For example, the circuit package 100 may include one or more electrical interconnects. The electrical interconnects may be any type of electrical interconnect, including one or more of soldering bumps, wires, copper pillars, wirebonds, through-substrate vias (TSVs), through-dielectric via (TDVs), redistribution layers (RDLs), landing pads, any other electrical interconnect, and combinations thereof. In some embodiments, the electrical interconnect copper pillar may be embedded in a landing pad. The copper pillar may protrude from the landing pad to connect with a photonic component on the photonic interposer 110. This may electrically couple the electrical component to the photonic component. The landing pad may have a larger surface area than a cross sectional area of the copper pillar. In some embodiments, the copper pillar is electrically connected to a cathode of a modulator. In some embodiments, the landing pad is shaped as a polygon or a circle, and the copper pillar is landed on the landing pad at a position away from a center of the polygon or circle.

[045] As discussed herein, the photonic interposer 110 may include any type of photonic elements. For example, the photonic interposer 110 may include a modulator. The modulator may be any type of modulator discussed herein. For example, the modulator may be a thermally stable modulator. In some examples, the modulator may be an electro-absorption modulator (EAM). The first processing element 134-1 of the analog-mixed signal portion 132-1 of the die 130 may include a driver. The driver may be connected to the modulator. For example, the modulator may be connected to the driver using an electrical interconnect. This may allow the analog-mixed signal portion 132-1 of the die 130 to communicate with the modulator of the photonic interposer 110.

[046] In some examples, the photonic interposer 110 may include a photodetector. The photodetector may be any type of photodetector, such as a photodiode. The first

processing element 134-1 of the analog-mixed signal portion 132-1 of the die 130 may include a transimpedance amplifier (TIA). The TIA and the photodetector may be in communication with an electrical interconnect. This may allow the analog-mixed signal portion 132-1 of the die 130 to communicate with the photonic interposer 110.

5 **[047]** As shown in Figure 2, the die 130 partially overlaps and is connected to both the photonic interposer 110 and the second interposer 120. As shown in Figure 2, the die 130 vertically overlaps both the photonic interposer 110 and the second interposer 120. The analog-mixed signal portion 132-1 vertically overlaps the photonic interposer 110 and the electronic portion 132-2 vertically overlaps the second interposer 120.

10 **[048]** In some embodiments, the photonic interposer 110 is optically connected to the die 130. For example, optical signals may be sent from the photonic interposer 110 and received by the die 130 and/or sent from the die 130 and received by the photonic interposer 110. In embodiments where the second interposer is a photonic interposer, the second interposer 120 is optically connected to the die 130. For example, optical signals may be
15 sent from the second interposer 120 and received by the die 130 and/or sent from the die 130 and received by the second interposer 120.

[049] In embodiments where the second interposer is a non-photonic interposer, the second interposer 120 is electrically connected to the die 130. For example, electrical signals may be sent from the second interposer 120 and received by the die 130 and/or sent
20 from the die 130 and received by the second interposer 120. In some embodiments, the second interposer 120 may include one or more through substrate vias (TSVs) that electrically connect to the die 130. For example, the second interposer 120 may electrically connect to the portion of the die 130 that overlaps the second interposer 120 through the TSVs. In some embodiments, the photonic interposer 110 may include one or more TSVs.

25 **[050]** As shown in Figure 2, the circuit package 100 may optionally include a second die 130-2. The second processing element 134-2 may be configured to communicate with the second die 130-2 through a communication path. The second die 130-2 may be electrically connected to the second interposer 120 over an electronic portion of the communication path. This may allow the second die 130-2 to communicate with the second
30 interposer 120 and/or the photonic interposer 110. In some embodiments, the second die 130-2 may be a third-party die or chip. In some embodiments, the second die 130-2 may be a different type of die or chip than the die 130.

[051] In some embodiments, the second die 130-2 may be electrically connected and/or in electrical communication with the electronic portion 132-2 of the die 130 over

the communication path. For example, the second die 130-2 may be electrically connected and/or in electrical communication with the electronic portion 132-2 through the second interposer 120. In some examples, the second die 130-2 may be electrically connected and/or in electrical communication with the electronic portion 132-2 through the communication path that travels through the second interposer 120.

[052] The second die 130-2 may include a third processing element 134-3. The third processing element 134-3 may communicate with the second processing element 134-2 in the electronic portion 132-2 over the communication path. For example, the third processing element 134-3 may receive signals and/or information from the electronic portion 132-2 of the die 130 over the communication path.

[053] In some embodiments, the second die 130-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 132-1 of the die 130 over the communication path. For example, the second die 130-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 132-1 through the electronic portion 132-2 and the second interposer 120. In some examples, the second die 130-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 132-1 through the communication path that travels through the second interposer 120 and the electronic portion 132-2. This may allow the third processing element 134-3 to communicate with the first processing element 134-1 of the analog-mixed signal portion 132-1.

[054] In some embodiments, the second die 130-2 may be electrically connected and/or in electrical communication with the photonic interposer 110 over the communication path. For example, the second die 130-2 may be electrically connected and/or in electrical communication with the photonic interposer 110 through the analog-mixed signal portion 132-1, the electronic portion 132-2, and the second interposer 120. In some examples, the second die 130-2 may be electrically connected and/or in electrical communication with the photonic interposer 110 through the communication path that travels through the second interposer 120, the electronic portion 132-2, and the analog-mixed signal portion 132-1. This may allow the third processing element 134-3 to communicate with the first processing element 134-1 of the analog-mixed signal portion 132-1.

[055] In some embodiments, the second die 130-2 may be optically connected and/or in optical communication with other optical elements of the circuit package 100 (such as an FAU) through the photonic interposer 110 and electrically connected and/or in electrical

communication with the photonic interposer 110 over the communication path. For example, the second die 130-2 may optically connected and/or in optical communication with the other optical elements through the photonic interposer 110 and be electrically connected and/or in electrical communication with the photonic interposer 110 through the analog-mixed signal portion 132-1, the electronic portion 132-2, and the second interposer 120. In some examples, the second die 130-2 may be optically connected and/or in optical communication with the other optical elements of the circuit package 100 through an optical portion of the communication path that travels through the photonic interposer 110 and electrically connected and/or in electrical communication with the photonic interposer 110 through the communication path that travels through the second interposer 120, the electronic portion 132-2, and the analog-mixed signal portion 132-1. This may allow the third processing element 134-3 to communicate with the other optical elements.

[056] Figure 3 is a top view of an embodiment of an electrical bridge package with integrated off-bridge photonic channel interface (as used herein circuit package 200). The circuit package 200 may be manufactured according to one or more methods described herein. For example, the circuit package 200 may be manufactured by the method 600 shown in Figure 7, by the method 700 shown in Figure 8, by the method 800 shown in Figure 9, and by the method 900 shown in Figure 10.

[057] The circuit package 200 includes a photonic interposer 210, a second interposer 220, and a die 230 partially overlapping and connected to both the photonic interposer 210 and the second interposer 220. As shown, the die 230 vertically overlaps both the photonic interposer 210 and the second interposer 220.

[058] In some embodiments, the second interposer 220 may be a photonic interposer (e.g., second photonic interposer). One or more photonic interposers (e.g., photonic interposer 210 or second interposer 220), in some embodiments, are photonic integrated circuits. In some embodiments, the second interposer 220 is a non-photonic interposer. Non-photonic interposers, in some embodiments, may include one or more of a silicon (SI) interposer, an SI bridge, other interposer materials, other bridge materials, or combinations thereof. In some embodiments, the photonic interposer 210 and the second interposer 220 are formed of silicon or a silicon alloy.

[059] In some embodiments, the photonic interposer 210 and the second interposer 220 are adjacent each other. For example, as shown, the photonic interposer 210 and the second interposer 220 may be only separated by a spacer (e.g., optional mold 240). The optional mold 240 may surround one or more lateral surfaces of the photonic interposer

210 and/or the second interposer 220. As shown, the optional mold 240 surrounds the entirety of the lateral surfaces of the photonic interposer 210 and the second interposer 220 including the space between the photonic interposer 210 and the second interposer 220. The photonic interposer 210 and the second interposer 220, in some embodiments, are directly adjacent. For example, the photonic interposer 210 and the second interposer 220 may be only separated by a space not a spacer (e.g., mold 240). In some embodiments, the photonic interposer 210 and the second interposer 220 abut each other. For example, the photonic interposer 210 and the second interposer 220 may directly touch (e.g., no mold 240).

10 **[060]** The die 230 may include various portions. For example, the die 230 may include an analog-mixed signal portion 232-1 and/or an electronic portion 232-2. The analog-mixed signal portion 232-1 may include a first processing element 234-1. The first processing element 234-1 may transmit and/or receive data using the photonic interposer 210. For example, the first processing element 234-1 may transmit and/or receive data photonically using the photonic interposer 210. The electronic portion 232-2 may include a second processing element 234-2. The second processing element 234-2 may transmit and/or receive data using the second interposer 220. For example, the second interposer 220 may be an electrical-only interposer (e.g., not a photonic interposer) such that the second processing element 234-2 may transmit and/or receive data electrically using the second interposer 220.

20 **[061]** As shown, the circuit package 200 may optionally include a substrate 201 that electrically connects to the photonic interposer 210 and/or the second interposer 220. The circuit package 200, as shown, may optionally include a second die 230-2 and/or a third die 230-3.

25 **[062]** The second die 230-2 and/or the third die 230-3 may include one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor.

30 **[063]** In embodiments where the second interposer 220 is a non-photonic interposer, the second die 230-2 and/or the third die 230-3 are electrically connected to the second interposer 220 by, for example, two or more TSVs. In embodiments where the second interposer 220 is a photonic interposer, the second die 230-2 and/or the third die 230-3 are optically connected to the second interposer 220.

[064] In some embodiments, at least a portion of the second interposer 220 beneath at least one die (e.g., second die 230-2 or third die 230-3) may be a mold (like mold 240). The

mold beneath at least one die may include a through mold via and/or a bond via array to facilitate communication with the at least one die.

5 [065] The circuit package 200, as shown, may optionally include one or more optical elements (e.g., fiber array units 250). The one or more optical elements are optically connected to the photonic interposer 210.

[066] As shown in Figure 3, the photonic interposer 210 and the second interposer 220 do not vertically overlap each other. In some embodiments, the photonic interposer 210 and the second interposer 220 at least partially vertically overlap each other. The analog-mixed signal portion 232-1 vertically overlaps the photonic interposer 210 and the
10 electronic portion 232-2 vertically overlaps the second interposer 220.

[067] The die 230 may include an ASIC, a processor, an image processor, a video processor, a general-purpose processor, or combinations thereof. As shown, the die 230 may be larger in at least one dimension than the photonic interposer 210. As shown, the die 230 is larger in the x-direction than the photonic interposer 210. In some embodiments, the
15 die 230 is larger than the photonic interposer 210 in two or more dimensions.

[068] Figure 4-1 is a cutaway side view of an embodiment of an electrical bridge package with integrated off-bridge photonic channel interface (as used herein circuit package 300). The circuit package 300 may be manufactured according to one or more methods described herein. For example, the circuit package 300 may be manufactured by
20 the method 600 shown in Figure 7, by the method 700 shown in Figure 8, and by the method 900 shown in Figure 10.

[069] As shown in Figure 4-1, a die 330 partially overlaps and is connected to both a photonic interposer 310 and a second interposer 320. As shown in Figure 4-1, the die 330 vertically overlaps both the photonic interposer 310 and the second interposer 320.

25 [070] In some embodiments, the second interposer 320 may be a photonic interposer (e.g., second photonic interposer). One or more photonic interposers (e.g., photonic interposer 310 or second interposer 320), in some embodiments, are photonic integrated circuits. In some embodiments, the second interposer 320 is a non-photonic interposer. Non-photonic interposers, in some embodiments, may include one or more of a silicon (SI)
30 interposer, an SI bridge, other interposer materials, other bridge materials, or combinations thereof. In some embodiments, the photonic interposer 310 and the second interposer 320 are formed of silicon or a silicon alloy.

[071] As shown, the photonic interposer 310 and the second interposer 320 are adjacent each other. For example, as shown, the photonic interposer 310 and the second

interposer 320 are only separated by an optional mold 340. The photonic interposer 310 and the second interposer 320, in some embodiments, are directly adjacent. For example, the photonic interposer 310 and the second interposer 320 may be only separated by a space. In some embodiments, the photonic interposer 310 and the second interposer 320 abut each other. For example, the photonic interposer 310 and the second interposer 320 may directly touch (e.g., without optional mold 340).

[072] The die 330 may include various portions. For example, the die 330 may include an analog-mixed signal portion 332-1 and/or an electronic portion 332-2. The analog-mixed signal portion 332-1 may include a first processing element 334-1. The first processing element 334-1 may transmit and/or receive data using the photonic interposer 310. For example, the first processing element 334-1 may transmit and/or receive data photonically using the photonic interposer 310. For example, the first processing element 334-1 may transmit and/or receive data using an electrical interface, as discussed herein. The electronic portion 332-2 may include a second processing element 334-2. The second processing element 334-2 may transmit and/or receive data using the second interposer 320. For example, the second interposer 320 may be an electrical-only interposer (e.g., not a photonic interposer) such that the second processing element 334-2 may transmit and/or receive data electrically using the second interposer 320.

[073] As shown, the circuit package 300 may optionally include a substrate 301 that electrically connects to the photonic interposer 310 and/or the second interposer 320. An optional redistribution layer (RDL) 360 may be applied to the substrate 301 to facilitate electrical connection to the photonic interposer 310 and/or the second interposer 320.

[074] The circuit package 300, as shown, may optionally include a second die 330-2. The second die 330-2 and/or a third die may include one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor. The second processing element 334-2 may be configured to communicate with the second die 330-2 through a communication path. The second die 330-2 may include a third processing element 334-3. The third processing element 334-3 may transmit and/or receive data using the second interposer 320. For example, the second interposer 320 may be an electrical-only interposer (e.g., not a photonic interposer) such that the third processing element 334-3 may transmit and/or receive data electrically using the second interposer 320.

[075] As discussed herein, The second die 330-2 may be electrically connected to the second interposer 320 over an electronic portion of the communication path. This may

allow the second die 330-2 to communicate with the second interposer 320 and/or the photonic interposer 310. In some embodiments, the second die 330-2 may be a third-party die or chip. In some embodiments, the second die 330-2 may be a different type of die or chip than the die 330.

5 **[076]** In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the electronic portion 332-2 of the die 330 over the communication path. For example, the second die 330-2 may be electrically connected and/or in electrical communication with the electronic portion 332-2 through the second interposer 320. In some examples, the second die 330-2 may be electrically connected
10 and/or in electrical communication with the electronic portion 332-2 through the communication path that travels through the second interposer 320.

[077] The second die 330-2 may include a third processing element 334-3. The third processing element 334-3 may communicate with the second processing element 334-2 in the electronic portion 332-2 over the communication path. For example, the third
15 processing element 334-3 may receive signals and/or information from the electronic portion 332-2 of the die 330 over the communication path.

[078] In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 of the die 330 over the communication path. For example, the second die 330-2 may be electrically
20 connected and/or in electrical communication with the analog-mixed signal portion 332-1 through the electronic portion 332-2 and the second interposer 320. In some examples, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 through the communication path that travels through the second interposer 320 and the electronic portion 332-2. This may allow the third
25 processing element 334-3 to communicate with the first processing element 334-1 of the analog-mixed signal portion 332-1.

[079] In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 over the communication path. For example, the second die 330-2 may be electrically connected
30 and/or in electrical communication with the photonic interposer 310 through the analog-mixed signal portion 332-1, the electronic portion 332-2, and the second interposer 320. In some examples, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 through the communication path that travels through the second interposer 320, the electronic portion 332-2, and the analog-

mixed signal portion 332-1. This may allow the third processing element 334-3 to communicate with the first processing element 334-1 of the analog-mixed signal portion 332-1.

[080] In some embodiments, the second die 330-2 may be optically connected and/or in optical communication with the FAU 350 through the photonic interposer 310 and electrically connected and/or in electrical communication with the photonic interposer 310 over the communication path. For example, the second die 330-2 may optically connected and/or in optical communication with the FAU 350 through the photonic interposer 310 and be electrically connected and/or in electrical communication with the photonic interposer 310 through the analog-mixed signal portion 332-1, the electronic portion 332-2, and the second interposer 320. In some examples, the second die 330-2 may be optically connected and/or in optical communication with the FAU 350 of the circuit package 300 through an optical portion of the communication path that travels through the photonic interposer 310 and electrically connected and/or in electrical communication with the photonic interposer 310 through the communication path that travels through the second interposer 320, the electronic portion 332-2, and the analog-mixed signal portion 332-1. This may allow the third processing element 334-3 to communicate with the FAU 350.

[081] The second die 330-2 may be connected to the second interposer 320 by an RDL layer 361. The RDL layer 361 may extend under a portion of the second die 330-2, under the entire second die 330-2, over a portion of the second interposer 320, over an entirety of the second interposer 320, under a portion of the photonic interposer 310, over a portion of the optional mold 340, over a portion photonic interposer 310, over a portion of the optional mold 340 and a portion photonic interposer 310, over an entirety of photonic interposer 310, under an entirety of die 330, over a portion of the second interposer 320 and over a portion the optional mold 340 and under a portion of the second die 330-2 and under a portion of the die 330 and over a portion of the photonic interposer 310, or combinations thereof. In embodiments where the RDL layer 361 extends over the photonic interposer 310, portions of the RDL layer 361 may be removed. For example, portions of RDL layer 361 that impede optical communication with the photonic interposer 310 may be at least partially or completely removed from the photonic interposer 310 to facilitate optical communication with the photonic interposer 310.

[082] In embodiments where the second interposer 320 is a non-photonic interposer, the second die 330-2 is electrically connected to the second interposer 320 by, for example, an optional RDL layer 361 and/or one or more TSVs 370. In embodiments where the

second interposer 320 is a photonic interposer, the second die 330-2 is optically connected to the second interposer 320.

[083] In some embodiments, at least a portion of the second interposer 320 beneath at least one die (e.g., second die 330-2 or an additional die) may be a mold (like mold 340).

5 The mold beneath at least one die may include a through mold via and/or a bond via array to facilitate communication with the at least one die.

[084] The circuit package 300, as shown, may optionally include one or more optical elements (e.g., fiber array units 350). The one or more optical elements are optically connected to the photonic interposer 310. In some embodiments, the circuit package 300
10 includes a fiber array unit (FAU) 350 for each photonic interposer 310. In accordance with at least one embodiment of the present disclosure, the FAU 350 is in communication with the photonic interposer 310 using one or more FAU connections that are portions of photonic channels. In some embodiments, the circuit package 300 may include multiple FAUs 350. For example, the circuit package 300 may include multiple FAUs 350 in
15 communication with a single photonic interposer 310. In some examples, the circuit package 300 may include multiple FAUs 250 connected to and/or in communication with different photonic interposers 310.

[085] In accordance with at least one embodiment of the present disclosure, the FAU 350 may be in communication with the photonic interposer 310 through a FAU connection
20 343. The FAU connection 343 may be any type of connection. For example, the FAU connection 343 may be manufactured to be in an optical coupling with light entering or exiting the photonic interposer via a photonic channel. For example, the FAU connection 343 may be a portion of a bidirectional channel. In some examples, the FAU connection 343 (e.g., the bidirectional channel) may include a waveguide or fiber.

25 **[086]** As shown in Figure 4-1, the photonic interposer 310 and the second interposer 320 do not vertically overlap each other. In some embodiments, the photonic interposer 310 and the second interposer 320 at least partially vertically overlap each other.

[087] The die 330 may include an ASIC, a processor, an image processor, a video processor, a general-purpose processor, or combinations thereof. As shown, the die 330
30 may be larger in at least one dimension than the photonic interposer 310. As shown, the die 330 is larger in the x-direction than the photonic interposer 310. In some embodiments, the die 330 is larger than the photonic interposer 310 in two or more dimensions.

[088] In some embodiments, the photonic interposer 310 is optically connected to the die 330. For example, optical signals may be sent from the photonic interposer 310 and

received by the die 330 and/or sent from the die 330 and received by the photonic interposer 310.

[089] In embodiments where the second interposer 320 is a photonic interposer, the second interposer 320 is optically connected to the die 330 and the second die 330-2. For example, optical signals may be sent from the second interposer 320 and received by the die 330 and the second die 330-2 and/or sent from the die 330 and the second die 330-2 and received by the second interposer 320.

[090] In embodiments where the second interposer is a non-photonic interposer, the second interposer 320 is electrically connected to the die 330 and the second die 330-2. For example, electrical signals may be sent from the second interposer 320 and received by the die 330 and/or the second die 330-2 and/or sent from the die 330 and/or the second die 330-2 and received by the second interposer 320. In some embodiments, the second interposer 320 may include one or more TSVs 370 that electrically connect to the die 330 and the second die 330-2. For example, the second interposer 320 may electrically connect to the portion of the die 330 that overlaps the second interposer 320 and/or the second die 330-2 through the TSVs 370. In some embodiments, the photonic interposer 310 may include one or more TSVs 370.

[091] As discussed herein, the second interposer 320 may be electrically connected to the electronic portion 332-2 of the die 330 with an electrical interconnect 333. The electrical interconnect 333 may be any type of electrical interconnect, including one or more of soldering bumps, wires, copper pillars, wirebonds, through-substrate vias (TSVs), through-dielectric via (TDVs), re-distribution layers (RDLs), landing pads, any other electrical interconnect, and combinations thereof. In some embodiments, the electrical interconnect copper pillar may be embedded in a landing pad. The copper pillar may protrude from the landing pad to connect with a photonic component on the photonic interposer 110. This may electrically couple the electrical component to the photonic component. The landing pad may have a larger surface area than a cross sectional area of the copper pillar. In some embodiments, the copper pillar is electrically connected to a cathode of a modulator. In some embodiments, the landing pad is shaped as a polygon or a circle, and the copper pillar is landed on the landing pad at a position away from a center of the polygon or circle.

[092] The electrical interconnect 333 may have an interconnect length that is the distance between the electronic portion 332-2 and the second interposer 320. The interconnect length may be any value. For example, the interconnect length may be no more than 50 microns, no more than 60 microns, no more than 70 microns, no more than 80

microns, no more than 90 microns, no more than 100 microns, no more than 110 microns, no more than 120 microns, no more than 130 microns, no more than 140 microns, no more than 150 microns, or any value therebetween. As a specific, non-limiting example, the interconnect length may be less than 100 microns to facilitate fast and efficient communication between the electrical component and the photonic component.

[093] The electrical interconnect 333 may have an interconnect diameter. The interconnect diameter may be any value. For example, the interconnect diameter may be 10 microns or less, 15 microns or less, 20 microns or less, 25 microns or less, 30 microns or less, 35 microns or less, 40 microns or less, 45 microns or less, 50 microns or less, or any value therebetween.

[094] FIG. 4-2 is a cutaway side view of an embodiment of a circuit package 300. The circuit package 300 may be manufactured according to one or more methods described herein. For example, the circuit package 300 may be manufactured by the method 600 shown in Figure 7, by the method 700 shown in Figure 8, and by the method 900 shown in Figure 10.

[095] As shown in Figure 4-2, a die 330 partially overlaps and is connected to both a photonic interposer 310 and a second interposer 320. As shown in Figure 4-2, the die 330 vertically overlaps both the photonic interposer 310 and the second interposer 320.

[096] The die 330 may include various portions. For example, the die 330 may include an analog-mixed signal portion 332-1 and/or an electronic portion 332-2. The analog-mixed signal portion 332-1 may include one or more processing elements. For example, the analog-mixed signal portion 332-1 may include a driver 335 and/or a transimpedance amplifier (TIA) 337. The processing elements of the analog-mixed signal portion 332 may transmit and/or receive data using the photonic interposer 310.

[097] The photonic interposer 310 may include a modulator 339 and/or a photodetector 341. As discussed herein, the processing elements of the analog-mixed signal portion 332-1, including the driver 335 and the TIA 337, may transmit and/or receive data with the photonic interposer 310. For example, the driver 335 of the analog-mixed signal portion 332-1 may be in communication with the modulator 339 of the photonic interposer 310. The driver 335 of the analog-mixed signal portion 332-1 may be connected to a first end of a first electrical interconnect 333-1. The modulator 339 of the photonic interposer 310 may be connected to a second end of the first electrical interconnect 333-1. In this manner, the driver 335 of the analog-mixed signal portion 332-1 and the modulator 339 of

the photonic interposer 310 may be in communication through the first electrical interconnect 333-1.

[098] In some examples, the TIA 337 of the analog-mixed signal portion 332-1 may be in communication with the photodetector 341 of the photonic interposer 310. The TIA 337 of the analog-mixed signal portion 332-1 may be connected to a first end of a second electrical interconnect 333-2. The photodetector 341 of the photonic interposer 310 may be connected to a second end of the second electrical interconnect 333-2. In this manner, the TIA 337 of the analog-mixed signal portion 332-1 and the photodetector 341 of the photonic interposer 310 may be in communication through the second electrical interconnect 333-2.

[099] As shown, the circuit package 300 may optionally include a substrate 301 that electrically connects to the photonic interposer 310 and/or the second interposer 320. An optional redistribution layer (RDL) 360 may be applied to the substrate 301 to facilitate electrical connection to the photonic interposer 310 and/or the second interposer 320.

[0100] The circuit package 300, as shown, may optionally include a second die 330-2. The second die 330-2 may include one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor. The second die 330-2 may include a second electronic portion (similar to the electronic portion 332-2) of the die 330. The second electronic portion may include one or more processing elements that may be configured to communicate with the second interposer 320 through a communication path. The second electronic portion may transmit and/or receive data using the second interposer 320. For example, the second interposer 320 may be an electrical-only interposer (e.g., not a photonic interposer) such that the second electronic portion may transmit and/or receive data electrically using the second interposer 320.

[0101] As discussed herein, The second die 330-2 may be electrically connected to the second interposer 320 over an electronic portion of a communication path. This may allow the second die 330-2 to communicate with the second interposer 320 and/or the photonic interposer 310. In some embodiments, the second die 330-2 may be a third-party die or chip. In some embodiments, the second die 330-2 may be a different type of die or chip than the die 330.

[0102] In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the electronic portion 332-2 of the die 330 over the communication path. For example, the second die 330-2 may be electrically connected

and/or in electrical communication with the electronic portion 332-2 through the second interposer 320. In some examples, the second die 330-2 may be electrically connected and/or in electrical communication with the electronic portion 332-2 through the communication path that travels through the second interposer 320.

5 **[0103]** The second die 330-2 may include a third processing element 334-3. The third processing element 334-3 may communicate with the second processing element 334-2 in the electronic portion 332-2 over the communication path. For example, the third processing element 334-3 may receive signals and/or information from the electronic portion 332-2 of the die 330 over the communication path.

10 **[0104]** In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 of the die 330 over the communication path. For example, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 through the electronic portion 332-2 and the second interposer 320. In some examples, the
15 second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 through the communication path that travels through the second interposer 320 and the electronic portion 332-2. This may allow the third processing element 334-3 to communicate with the first processing elements the analog-mixed signal portion 332-1, such as the driver 335 and/or the TIA 337.

20 **[0105]** In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 over the communication path. For example, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 through the analog-mixed signal portion 332-1 (including the driver 335 and/or the TIA 337), the electronic
25 portion 332-2, and the second interposer 320. In some examples, the second die 130-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 through the communication path that travels through the second interposer 320, the electronic portion 332-2, and the analog-mixed signal portion 332-1. In some examples, the second die 130-2 may be electrically connected and/or in electrical communication
30 with the photonic interposer 310 through the modulator 339 and/or the photodetector 341 of the photonic interposer 310.

[0106] In some embodiments, the second die 330-2 may be optically connected and/or in optical communication with the FAU 350 through the photonic interposer 310 and electrically connected and/or in electrical communication with the photonic interposer 310

over the communication path. For example, the second die 330-2 may optically connected and/or in optical communication with the FAU 350 through the photonic interposer 310 and be electrically connected and/or in electrical communication with the photonic interposer 310 through the analog-mixed signal portion 332-1, the electronic portion 332-2, and the second interposer 320. In some examples, the second die 330-2 may be optically connected and/or in optical communication with the FAU 350 of the circuit package 300 through an optical portion of the communication path that travels through the photonic interposer 310 and electrically connected and/or in electrical communication with the photonic interposer 310 through the communication path that travels through the second interposer 320, the electronic portion 332-2, and the analog-mixed signal portion 332-1. This may allow the third processing element 334-3 to communicate with the FAU 350.

[0107] The second die 330-2 may be connected to the second interposer 320 by an RDL layer 361. The RDL layer 361 may extend under a portion of the second die 330-2, under the entire second die 330-2, over a portion of the second interposer 320, over an entirety of the second interposer 320, under a portion of the photonic interposer 310, over a portion of the optional mold 340, over a portion photonic interposer 310, over a portion of the optional mold 340 and a portion photonic interposer 310, over an entirety of photonic interposer 310, under an entirety of die 330, over a portion of the second interposer 320 and over a portion the optional mold 340 and under a portion of the second die 330-2 and under a portion of the die 330 and over a portion of the photonic interposer 310, or combinations thereof. In embodiments where the RDL layer 361 extends over the photonic interposer 310, portions of the RDL layer 361 may be removed. For example, portions of RDL layer 361 that impede optical communication with the photonic interposer 310 may be at least partially or completely removed from the photonic interposer 310 to facilitate optical communication with the photonic interposer 310.

[0108] In embodiments where the second interposer 320 is a non-photonic interposer, the second die 330-2 is electrically connected to the second interposer 320 by, for example, an optional RDL layer 361 and/or one or more TSVs 370. In embodiments where the second interposer 320 is a photonic interposer, the second die 330-2 is optically connected to the second interposer 320.

[0109] In some embodiments, at least a portion of the second interposer 320 beneath at least one die (e.g., second die 330-2 or an additional die) may be a mold (like mold 340). The mold beneath at least one die may include a through mold via and/or a bond via array to facilitate communication with the at least one die.

[0110] FIG. 4-3 is a cutaway side view of an embodiment of a circuit package 300. The circuit package 300 may be manufactured according to one or more methods described herein. For example, the circuit package 300 may be manufactured by the method 600 shown in Figure 7, by the method 700 shown in Figure 8, and by the method 900 shown in
5 Figure 10.

[0111] As shown in Figure 4-3, a die 330 partially overlaps and is connected to both a photonic interposer 310 and a second interposer 320. As shown in Figure 4-3, the die 330 vertically overlaps both the photonic interposer 310 and the second interposer 320.

[0112] The die 330 may include various portions. For example, the die 330 may include
10 an analog-mixed signal portion 332-1 and/or an electronic portion 332-2. The analog-mixed signal portion 332-1 may include one or more processing elements. For example, the analog-mixed signal portion 332-1 may include a driver 335 and/or a transimpedance amplifier (TIA) 337. The processing elements of the analog-mixed signal portion 332-1 may transmit and/or receive data using the photonic interposer 310.

[0113] The photonic interposer 310 may include a modulator 339-1 and/or a photodetector 341. As discussed herein, the processing elements of the analog-mixed signal portion 332-1, including the driver 335 and the TIA 337, may transmit and/or receive data with the photonic interposer 310. For example, the driver 335 of the analog-mixed signal portion 332-1 may be in communication with the modulator 339 of the photonic interposer
20 310. The driver 335 of the analog-mixed signal portion 332-1 may be connected to a first end of a first electrical interconnect 333-1. The modulator 339 of the photonic interposer 310 may be connected to a second end of the first electrical interconnect 333-1. In this manner, the driver 335 of the analog-mixed signal portion 332-1 and the modulator 339 of the photonic interposer 310 may be in communication through the first electrical
25 interconnect 333-1.

[0114] In some examples, the TIA 337 of the analog-mixed signal portion 332-1 may be in communication with the photodetector 341 of the photonic interposer 310. The TIA 337 of the analog-mixed signal portion 332-1 may be connected to a first end of a second electrical interconnect 333-2. The photodetector 341 of the photonic interposer 310 may be
30 connected to a second end of the second electrical interconnect 333-2. In this manner, the TIA 337 of the analog-mixed signal portion 332-1 and the photodetector 341 of the photonic interposer 310 may be in communication through the second electrical interconnect 333-2.

[0115] As shown, the circuit package 300 may optionally include a substrate 301 that electrically connects to the photonic interposer 310 and/or the second interposer 320. An optional redistribution layer (RDL) 360 may be applied to the substrate 301 to facilitate electrical connection to the photonic interposer 310 and/or the second interposer 320.

5 [0116] The circuit package 300, as shown, may optionally include a second die 330-2. The second die 330-2 may include one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor. The second die 330-2 may include a second analog-mixed signal portion (similar to the analog-mixed signal portion 332-1) of the die 330. The second analog-mixed signal
10 portion may include one or more processing elements that may be configured to communicate with the photonic interposer 310 through a communication path. The second analog-mixed signal portion may transmit and/or receive data using the photonic interposer 310. For example, the photonic interposer 310 may be a photonic integrated circuit (PIC) such that the second analog-mixed signal portion may transmit and/or receive data
15 electrically using the photonic interposer 310.

[0117] In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 of the die 330 over the communication path. For example, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1
20 through the electronic portion 332-2 and the second interposer 320. In some examples, the second die 330-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 332-1 through the communication path that travels through the second interposer 320 and the electronic portion 332-2. This may allow the third processing element 334-3 to communicate with the first processing elements the analog-mixed signal portion 332-1, such as the driver 335 and/or the TIA 337.

[0118] In some embodiments, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 over the communication path. For example, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 through the analog-mixed signal portion 332-1 (including the driver 335 and/or the TIA 337), the electronic
30 portion 332-2, and the second interposer 320. In some examples, the second die 330-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 through the communication path that travels through the second interposer 320, the electronic portion 332-2, and the analog-mixed signal portion 332-1. In some examples,

the second die 130-2 may be electrically connected and/or in electrical communication with the photonic interposer 310 through the modulator 339 and/or the photodetector 341 of the photonic interposer 310.

[0119] In some embodiments, the second die 330-2 may be optically connected and/or in optical communication with the FAU 350 through the photonic interposer 310 and electrically connected and/or in electrical communication with the photonic interposer 310 over the communication path. For example, the second die 330-2 may optically connected and/or in optical communication with the FAU 350 through the photonic interposer 310 and be electrically connected and/or in electrical communication with the photonic interposer 310 through the analog-mixed signal portion 332-1, the electronic portion 332-2, and the second interposer 320. In some examples, the second die 330-2 may be optically connected and/or in optical communication with the FAU 350 of the circuit package 300 through an optical portion of the communication path that travels through the photonic interposer 310 and electrically connected and/or in electrical communication with the photonic interposer 310 through the communication path that travels through the second interposer 320, the electronic portion 332-2, and the analog-mixed signal portion 332-1. This may allow the third processing element 334-3 to communicate with the FAU 350.

[0120] As may be seen, the circuit package 300 may further include a third die 330-3. The third die 330-3 may include a fourth processing element 334-4. The third die 330-3 may be connected to the photonic interposer 310. For example, the fourth processing element 334-4 may be in communication with optical elements 345 of the photonic interposer 310. For example, the fourth processing element 334-4 may include a driver and a TIA in communication with the optical elements 345 including a modulator and a photodetector, respectively of the photonic interposer 310. The communication path may include an optical connection between the third die 330-3 and the die 330. For example, the optical elements 345 may be in optical communication with the modulator 339 and the photodetector 341 that are connected to the driver 335 and the 337 of the analog-mixed signal portion 332-1. This may allow the third die 330-3 to be in communication with the die 330 and/or the second die 330-2. The third die 330-3 may be an optical die, or a die that includes optical elements to communicate with the photonic interposer 310.

[0121] The second die 330-2 and/or the third die 330-3 may be connected to the photonic interposer 310 by an RDL layer 361. The RDL layer 361 may extend under a portion of the second die 330-2, under the entire second die 330-2, over a portion of the photonic interposer 310, over an entirety of the photonic interposer 310, under a portion of

the second interposer 320, over a portion of the optional mold 340, over a portion of the second interposer 320, over a portion of the optional mold 340 and a portion of the second interposer 320, over an entirety of the second interposer 320, under an entirety of die 330, over a portion of the photonic interposer 310 and over a portion the optional mold 340 and under a portion of the second die 330-2 and under a portion of the die 330 and over a portion of the second interposer 320, or combinations thereof. In embodiments where the RDL layer 361 extends over the photonic interposer 310, portions of the RDL layer 361 may be removed. For example, portions of RDL layer 361 that impede optical communication with the photonic interposer 310 may be at least partially or completely removed from the photonic interposer 310 to facilitate optical communication with the photonic interposer 310.

[0122] Figure 5 is a cutaway side view of an embodiment of an electrical bridge package with integrated off-bridge photonic channel interface (as used herein circuit package 400). The circuit package 400 may be manufactured according to one or more methods described herein. For example, the circuit package 4F00 may be manufactured by the method 600 shown in Figure 7 and by the method 800 shown in Figure 9.

[0123] As shown in Figure 5, a die 430 partially overlaps and is connected to both a photonic interposer 410 and a second interposer 420. As shown in Figure 5, the die 430 vertically overlaps both the photonic interposer 410 and the second interposer 420.

[0124] In some embodiments, the second interposer 420 may be a photonic interposer (e.g., second photonic interposer). One or more photonic interposers (e.g., photonic interposer 410 or second interposer 420), in some embodiments, are photonic integrated circuits. In some embodiments, the second interposer 420 is a non-photonic interposer. Non-photonic interposers, in some embodiments, may include one or more of a silicon (SI) interposer, an SI bridge, other interposer materials, other bridge materials, or combinations thereof. In some embodiments, the photonic interposer 410 and the second interposer 420 are formed of silicon or a silicon alloy.

[0125] As shown, the photonic interposer 410 and the second interposer 420 are adjacent each other. For example, as shown, the photonic interposer 410 and the second interposer 420 are only separated by an optional mold 440. The photonic interposer 410 and the second interposer 420, in some embodiments, are directly adjacent. For example, the photonic interposer 410 and the second interposer 420 may be only separated by a space. In some embodiments, the photonic interposer 410 and the second interposer 420 abut each

other. For example, the photonic interposer 410 and the second interposer 420 may directly touch (e.g., without optional mold 440).

[0126] The die 430 may include various portions. For example, the die 430 may include an analog-mixed signal portion 432-1 and/or an electronic portion 432-2. The analog-mixed signal portion 432-1 may include a first processing element 434-1. The first processing element 434-1 may transmit and/or receive data using the photonic interposer 410. For example, the first processing element 434-1 may transmit and/or receive data photonically using the photonic interposer 410. The electronic portion 432-2 may include a second processing element 434-2. The second processing element 434-2 may transmit and/or receive data using the second interposer 420. For example, the second interposer 420 may be an electrical-only interposer (e.g., not a photonic interposer) such that the second processing element 434-2 may transmit and/or receive data electrically using the second interposer 420.

[0127] As shown, the circuit package 400 may optionally include a substrate 401 that electrically connects to the photonic interposer 410 and/or the second interposer 420. An optional RDL layer 460 may be applied to the substrate 401 to facilitate electrical connection to the photonic interposer 410 and/or the second interposer 420. An additional optional RDL layer 461 may be applied above the first RDL layer 460 to the substrate 401 to facilitate electrical connection to the photonic interposer 410 and/or the second interposer 420.

[0128] The circuit package 400, as shown, may optionally include a second die 430-2. The second die 430-2 and/or the third die 430-3 may include one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor. The second processing element 434-2 may be configured to communicate with the second die 430-2 through a communication path (shown in red). The second die 430-2 may include a third processing element 434-3. The third processing element 434-3 may transmit and/or receive data using the second interposer 420. For example, the second interposer 420 may be an electrical-only interposer (e.g., not a photonic interposer) such that the third processing element 434-3 may transmit and/or receive data electrically using the second interposer 420.

[0129] As discussed herein, The second die 430-2 may be electrically connected to the second interposer 420 over an electronic portion of the communication path. This may allow the second die 430-2 to communicate with the second interposer 420 and/or the photonic interposer 410. In some embodiments, the second die 430-2 may be a third-party

die or chip. In some embodiments, the second die 430-2 may be a different type of die or chip than the die 430.

[0130] In some embodiments, the second die 430-2 may be electrically connected and/or in electrical communication with the electronic portion 432-2 of the die 430 over the communication path. For example, the second die 430-2 may be electrically connected and/or in electrical communication with the electronic portion 432-2 through the second interposer 420. In some examples, the second die 430-2 may be electrically connected and/or in electrical communication with the electronic portion 432-2 through the communication path that travels through the second interposer 420.

[0131] The second die 430-2 may include a third processing element 434-3. The third processing element 434-3 may communicate with the second processing element 434-2 in the electronic portion 432-2 over the communication path. For example, the third processing element 434-3 may receive signals and/or information from the electronic portion 432-2 of the die 430 over the communication path.

[0132] In some embodiments, the second die 430-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 432-1 of the die 430 over the communication path. For example, the second die 430-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 432-1 through the electronic portion 432-2 and the second interposer 420. In some examples, the second die 430-2 may be electrically connected and/or in electrical communication with the analog-mixed signal portion 432-1 through the communication path that travels through the second interposer 420 and the electronic portion 432-2. This may allow the third processing element 434-3 to communicate with the first processing element 434-1 of the analog-mixed signal portion 432-1.

[0133] In some embodiments, the second die 430-2 may be electrically connected and/or in electrical communication with optical elements 445 of the photonic interposer 410 over the communication path. For example, the second die 430-2 may be electrically connected and/or in electrical communication with the photonic interposer 410 through the analog-mixed signal portion 432-1, the electronic portion 432-2, and the second interposer 420. In some examples, the second die 430-2 may be electrically connected and/or in electrical communication with the photonic interposer 410 through the communication path that travels through the second interposer 420, the electronic portion 432-2, and the analog-mixed signal portion 432-1. This may allow the third processing element 434-3 to communicate with the optical elements 445 of the photonic interposer 410.

- [0134] In some embodiments, the second die 430-2 may be optically connected and/or in optical communication with the FAU 450 through the photonic interposer 410 and electrically connected and/or in electrical communication with the photonic interposer 410 over the communication path. For example, the second die 430-2 may optically connected and/or in optical communication with the FAU 450 through the photonic interposer 410 and be electrically connected and/or in electrical communication with the photonic interposer 410 through the analog-mixed signal portion 432-1, the electronic portion 432-2, and the second interposer 420. In some examples, the second die 430-2 may be optically connected and/or in optical communication with the FAU 450 of the circuit package 400 through an optical portion of the communication path that travels through the photonic interposer 410 and electrically connected and/or in electrical communication with the photonic interposer 410 through the communication path that travels through the second interposer 420, the electronic portion 432-2, and the analog-mixed signal portion 432-1. This may allow the third processing element 434-3 to communicate with the FAU 450.
- [0135] The second die 430-2 may be connected to the second interposer 420 by an optional RDL layer 462. The RDL layer 462 may extend under a portion of the second die 430-2, under the entire second die 430-2, over a portion of the second interposer 420, over an entirety of the second interposer 420, under a portion of the photonic interposer 410, over a portion of the optional mold 440, over a portion photonic interposer 410, over a portion of the optional mold 440 and a portion photonic interposer 410, over an entirety of photonic interposer 410, under an entirety of die 430, over a portion of the second interposer 420 and over a portion the optional mold 440 and under a portion of the second die 430-2 and under a portion of the die 430 and over a portion of the photonic interposer 410, or combinations thereof.
- [0136] The RDL layer 462 and/or the second interposer 420 may combine with the photonic interposer 410 to create high precision pads. For example, because the die 430 overlaps both the photonic interposer 410 and the second interposer 420, the connection (e.g., RDL layer 462) between the die 430 and the photonic interposer 410 and between the die 430 and the second interposer 420 may require high levels of precision. The high precision pads may include a top surface that is substantially the same vertical height over the photonic interposer 410 and second interposer 420. The high precision pads may remove one or more the tolerance issues between photonic interposer 410 and second interposer 420 in one or more of the X-direction, the Y-direction, and the vertical direction.

[0137] In embodiments where the RDL layer 462 extends over the photonic interposer 410, portions of the RDL layer 462 may be removed. For example, portions of RDL layer 462 that impede optical communication with the photonic interposer 410 may be at least partially or completely removed from the photonic interposer 410 to facilitate optical communication with the photonic interposer 410.

[0138] In embodiments where the second interposer 420 is a non-photonic interposer, the second die 430-2 is electrically connected to the second interposer 420 by, for example, an optional RDL layer 462 and/or one or more TSVs 470. In embodiments where the second interposer 420 is a photonic interposer, the second die 430-2 is optically connected to the second interposer 420.

[0139] The circuit package 400, as shown, may optionally include one or more optical elements (e.g., fiber array units 450). The one or more optical elements are optically connected to the photonic interposer 410. As shown in Figure 5, the RDL 462 is removed beneath the one or more fiber array units 450 to form, for example, optional opening 490.

[0140] In some embodiments, at least a portion of the second interposer 420 beneath at least one die (e.g., second die 430-2 or an additional die) may be a mold. The mold beneath at least one die may include a through mold via and/or a bond via array to facilitate communication with the at least one die.

[0141] As shown in Figure 5, the photonic interposer 410 and the second interposer 420 do not vertically overlap each other. In some embodiments, the photonic interposer 410 and the second interposer 420 at least partially vertically overlap each other.

[0142] The die 430 may include an ASIC, a processor, an image processor, a video processor, a general-purpose processor, or combinations thereof. As shown, the die 430 may be larger in at least one dimension than the photonic interposer 410. As shown, the die 430 is larger in the x-direction than the photonic interposer 410. In some embodiments, the die 430 is larger than the photonic interposer 410 in two or more dimensions.

[0143] In some embodiments, the photonic interposer 410 is optically connected to the die 430. For example, optical signals may be sent from the photonic interposer 410 and received by the die 430 and/or sent from the die 430 and received by the photonic interposer 410.

[0144] In embodiments where the second interposer 420 is a photonic interposer, the second interposer 420 is optically connected to the die 430 and the second die 430-2. For example, optical signals may be sent from the second interposer 420 and received by the

die 430 and the second die 430-2 and/or sent from the die 430 and the second die 430-2 and received by the second interposer 420.

[0145] In embodiments where the second interposer is a non-photonic interposer, the second interposer 420 is electrically connected to the die 430 and the second die 430-2. For example, electrical signals may be sent from the second interposer 420 and received by the die 430 and/or the second die 430-2 and/or sent from the die 430 and/or the second die 430-2 and received by the second interposer 420. In some embodiments, the second interposer 420 may include one or more TSVs 470 that electrically connect to the die 430 and the second die 430-2. For example, the second interposer 420 may electrically connect to the portion of the die 430 that overlaps the second interposer 420 and/or the second die 430-2 through the TSVs 470. In some embodiments, the photonic interposer 410 may include one or more TSVs 470.

[0146] Figure 6 is a top view of an embodiment of an electrical bridge package with integrated off-bridge photonic channel interface (as used herein circuit package 500). The circuit package 500 may be manufactured according to one or more methods described herein. For example, the circuit package 500 may be manufactured by the method 600 shown in Figure 7, by the method 700 shown in Figure 8, by the method 800 shown in Figure 9, and by the method 900 shown in Figure 10.

[0147] The circuit package 500 includes multiple photonic interposers (e.g., photonic interposer 510, second photonic interposer 510-2, and third photonic interposer 510-3), multiple additional interposers (e.g., second interposer 520 and third interposer 520-2), and multiple dies (e.g., die 530, second die 530-2, third die 530-3, fourth die 530-4, fifth die 530-5, sixth die 530-6). One or more of the multiple dies may partially overlap and be connected to one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers.

[0148] The multiple dies may include one or more portions. The die 530 includes an analog-mixed signal portion 532-1 and an electronic portion 532-2. The analog-mixed signal portion 532-1 may include a first processing element 534-1. The first processing element 534-1 may transmit and/or receive data using the photonic interposer 510. For example, the first processing element 534-1 may transmit and/or receive data photonically using the photonic interposer 510. The electronic portion 532-2 may include a second processing element 534-2. The second processing element 534-2 may transmit and/or receive data using the second interposer 520. For example, the second interposer 520 may be an electrical-only interposer (e.g., not a photonic interposer) such that the second

processing element 534-2 may transmit and/or receive data electrically using the second interposer 520.

[0149] The second die 530-2 includes multiple portions. For example, the second die 530-2 is shown with an electronic portion over the second interposer 520 with a third processing element 534-3 which may transmit and/or receive data photonicall
5 y using the second interposer 520, shown with an analog-mixed signal portion over the second photonic interposer 510-2 with a fourth processing element 534-4 which may transmit and/or receive data photonicall using the second photonic interposer 510-2, shown with an electronic portion over the third interposer 520-2 with a fifth processing element 534-5
10 y which may transmit and/or receive data electrically using the third interposer 510-2, and shown with an analog-mixed signal portion over the third photonic interposer 510-3 with a sixth processing element 534-6 which may transmit and/or receive data photonicall using the third photonic interposer 510-3. The third die 530-3 includes an analog-mixed signal portion over the second photonic interposer 510-2 with a seventh processing element 534-
15 y 7 which may transmit and/or receive data photonicall using the second photonic interposer 510-2 and an electronic portion over the third interposer 520-2 with an eighth processing element 534-8 which may transmit and/or receive data electrically using the third interposer 520-2. The fourth die 530-4 only includes an electronic portion over the third interposer 520-2 with a ninth processing element 534-9 which may transmit and/or receive data
20 y electrically using the third interposer 520-2. The fifth die 530-5 only includes an analog-mixed signal portion over the third photonic interposer 510-3 with a tenth processing element 534-10 which may transmit and/or receive data photonicall using the third photonic interposer 510-3. More or fewer dies with more or fewer portions and/or more or fewer processing elements that interact with more or fewer interposers (electro-photonic,
25 y electrical-only, or otherwise) may be used. All combinations are contemplated.

[0150] As shown, the die 530 vertically overlaps both the photonic interposer 510 and the second interposer 520. The second die 530-2 vertically overlaps the second interposer 520, the second photonic interposer 510-2, the third photonic interposer 510-3, and the third interposer 520-2. Overlapping multiple interposers may facilitate communication between
30 y one or more components while reducing the cost of a photonic interposer sized to connect to all of the multiple dies (e.g., the size of the dotted box surrounding all of the interposers).

[0151] In some embodiments, the multiple additional interposers (e.g., second interposer 520 and third interposer 520-2) may be a photonic interposer (e.g., second photonic interposer). One or more photonic interposers (e.g., photonic interposer 510,

second photonic interposer 510-2, third photonic interposer 510-3, second interposer 520, and third interposer 520-2), in some embodiments, are photonic integrated circuits. In some embodiments, one or more of the multiple additional interposers (e.g., second interposer 520 and third interposer 520-2) are a non-photonic interposer. Non-photonic interposers, in
5 some embodiments, may include one or more of a silicon (SI) interposer, an SI bridge, other interposer materials, other bridge materials, or combinations thereof. In some embodiments, one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers are formed of silicon or a silicon alloy.

[0152] In some embodiments, one or more of the multiple photonic interposers and/or
10 one or more of the multiple additional interposers are adjacent each other. For example, one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers may be only separated by a space or a spacer (e.g., a mold). The one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers, in some embodiments, are directly adjacent. For example, the one or more of
15 the multiple photonic interposers and/or one or more of the multiple additional interposers may be only separated by a space. In some embodiments, the photonic one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers abut each other. For example, one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers may directly touch. In some embodiments, two
20 or more interposers may be adjacent, two or more interposers may be directly adjacent, two or more interposers may abut, or combinations thereof.

[0153] As shown in Figure 5, one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers do not vertically overlap each other. In some embodiments, one or more of the multiple photonic interposers and/or one or more
25 of the multiple additional interposers at least partially vertically overlap each other.

[0154] The multiple dies may include an ASIC, a processor, an image processor, a video processor, a general-purpose processor, or combinations thereof. The multiple die may be larger in at least one dimension than one or more of the multiple photonic interposers and/or one or more of the multiple additional interposers. As shown, the die 530
30 is larger in the x-direction than the photonic interposer 510 and the second die 530-2 is larger than the second interposer 520-2 in its entirety. In some embodiments, one or more of the multiple die are larger than one or more of the multiple photonic interposers and/or one or more of the multiple interposers in two or more dimensions.

[0155] In some embodiments, the circuit package 500 may include one or more optical elements, a substrate, various RDL layers, openings in one or more RDL layers, TSVs, any other component described herein, or combinations thereof.

[0156] The one or more RDL layers described herein may be ten microns line per inch, may be less than two microns in the vertical direction, may be less than two layers thick in the vertical direction, or combinations thereof.

[0157] Figure 7 is an embodiment of a method 600 of manufacturing a circuit package (e.g., circuit package 100, 200, 300, 400, 500). The method 600 includes connecting a photonic interposer (e.g., photonic interposer 110, 210, 310, 410, 510, 510-2, 510-3) and a second interposer (e.g., second interposer 120, 220, 320, 420, 520, third interposer 510-2) at act 610. The method 600 includes connecting a die (e.g., die 130, 230, 330, 330-2, 430, 430-2, 530, 530-2, 530-3, 530-4) to both the photonic interposer and the second interposer, where the die partially overlaps both the photonic interposer and the second interposer. The method 600 includes connecting an optical element (e.g., FAU 250, 350, 450) to the photonic interposer.

[0158] The method 600 optionally includes applying a mold (e.g., mold 240, 340, 440) to the photonic interposer and the second interposer to form a rigid unit. In some embodiments the mold is silicon or silicon alloy. In some embodiments, the mold includes a material that matches a thermal expansion of one or more of the photonic interposer and the second interposer.

[0159] The method 600 optionally includes forming the second interposer as a mold. The method 600 optionally includes providing one or more through substrate vias, through mold vias, bond via arrays, or combinations thereof through the mold.

[0160] The method 600 optionally includes attaching a second die to one or more of the photonic interposer and the second interposer. The method 600 optionally includes attaching a third die to one or more of the photonic interposer, the second interposer, or a third interposer.

[0161] Figure 8 is an embodiment of a method 700 of manufacturing a circuit package (e.g., circuit package 100, 200, 300, 400, 500). The method 700 optionally includes forming a photonic interposer (e.g., photonic interposer 110, 210, 310, 410, 510, 510-2, 510-3) and a second interposer (e.g., second interposer 120, 220, 320, 420, 520, third interposer 510-2) on a carrier at act 710.

[0162] The method 700 includes connecting a photonic interposer and a second interposer at act 720. The method 700 optionally includes rigidly connecting a photonic interposer and a second interposer at act 730.

5 [0163] The method 700 optionally includes applying redistribution layer to a bottom surface of one or more of photonic interposer and second interposer at act 740. The method 700 optionally includes debonding photonic interposer and second interposer from carrier at act 750. The method optionally includes applying redistribution layer to a top surface of second interposer at act 760.

10 [0164] The method 700 includes connecting a die (e.g., die 130, 230, 330, 330-2, 430, 430-2, 530, 530-2, 530-3, 530-4) to both the photonic interposer and the second interposer, where the die partially overlaps both the photonic interposer and the second interposer at act 770. The method 700 optionally includes exposing a portion of a top surface of photonic interposer at act 780. Exposing the portion of the top surface of the photonic interposer may include one or more of laser drilling, etching, or clearing. The method 700 includes
15 connecting an optical element (e.g., FAU 250, 350, 450) to the photonic interposer at act 790 optionally at the exposed portion of act 780.

[0165] The method 700 optionally includes applying a mold (e.g., mold 240, 340, 440) to the photonic interposer and the second interposer to form a rigid unit. In some embodiments the mold is silicon or silicon alloy. In some embodiments, the mold includes
20 a material that matches a thermal expansion of one or more of the photonic interposer and the second interposer.

[0166] The method 700 optionally includes forming the second interposer as a mold. The method 700 optionally includes providing one or more through substrate vias, through mold vias, bond via arrays, or combinations thereof through the mold.

25 [0167] The method 700 optionally includes attaching a second die to one or more of the photonic interposer and the second interposer. The method 700 optionally includes attaching a third die to one or more of the photonic interposer, the second interposer, or a third interposer.

30 [0168] Figure 9 is an embodiment of a method 800 of manufacturing a circuit package (e.g., circuit package 100, 200, 300, 400, 500). The method 800 optionally includes applying redistribution layer (e.g., RDL layer 460) to a substrate (e.g., substrate 201, 301, 401) at act 810. The method 800 includes connecting a photonic interposer (e.g., photonic interposer 110, 210, 310, 410, 510, 510-2, 510-3) and a second interposer (e.g., second

interposer 120, 220, 320, 420, 520, third interposer 510-2) to the redistribution layer on the substrate at act 820.

[0169] The method 800 optionally includes rigidly connecting a photonic interposer and a second interposer at act 830. The method 800 optionally includes applying
5 redistribution layer to a portion of photonic interposer and second interposer at act 840.

[0170] In some implementations, applying redistribution layer to a portion of photonic interposer and second interposer forms a plurality of high precision pads on two or more of the photonic interposer, the second interposer, a second photonic interposer, a third interposer, and a third photonic interposer. In some implementations, forming the plurality
10 of high precision pads facilitate connecting the die to the two or more of the photonic interposer, the second interposer, a second photonic interposer, a third interposer, and a third photonic interposer. In some implementations, facilitating connecting the die to the two or more of the photonic interposer, the second interposer, a second photonic interposer, a third interposer, and a third photonic interposer includes forming a top surface on the high
15 precision pads that is substantially the same vertical height. In some implementations, the high precision pads remove the tolerance issues between two or more of the photonic interposer, the second interposer, a second photonic interposer, a third interposer, and a third photonic interposer in one or more of the X-direction, the Y-direction, and the vertical direction.

[0171] The method 800 optionally includes exposing a portion of a top surface of the photonic interposer at act 850.

[0172] The method includes connecting a die (e.g., die 130, 230, 330, 330-2, 430, 430-2, 530, 530-2, 530-3, 530-4) to both the photonic interposer and the second interposer, where the die partially overlaps both the photonic interposer and the second interposer at
25 act 860. The method 800 optionally includes connecting an optical element (e.g., FAU 250, 350, 450) to the photonic interposer at act 870.

[0173] The method 800 optionally includes applying a mold (e.g., mold 240, 340, 440) to the photonic interposer and the second interposer to form a rigid unit. In some embodiments the mold is silicon or silicon alloy. In some embodiments, the mold includes
30 a material that matches a thermal expansion of one or more of the photonic interposer and the second interposer.

[0174] The method 800 optionally includes forming the second interposer as a mold. The method 800 optionally includes providing one or more through substrate vias, through mold vias, bond via arrays, or combinations thereof through the mold.

[0175] The method 800 optionally includes attaching a second die to one or more of the photonic interposer and the second interposer. The method 800 optionally includes attaching a third die to one or more of the photonic interposer, the second interposer, or a third interposer.

5 [0176] Figure 10 is an embodiment of a method 900 of manufacturing a circuit package (e.g., circuit package 100, 200, 300, 400, 500). The method 900 includes connecting a photonic interposer (e.g., photonic interposers 110, 210, 310, 410, 510, 510-2, 510-3) and an electrical interposer (e.g., second interposers 120, 220, 320, 420, 520, and third interposer 520-2) at act 910. The method 900 includes receiving a die (e.g., die 130, 230,
10 330, 430, 530, 530-2, 530-3, 530-4, 530-5, 530-6) partitioned into first and second portions (e.g., analog-mixed signal portions 132-1, 232-1, 332-1, 432-1, 532-1, electronic portions 132-2, 232-2, 332-2, 432-2, 532-2, other portions) at act 920.

[0177] The method 900 includes connecting the first portion of the die to the photonic interposer and the second portion of the die to the electrical interposer at act 930. The
15 method 900 includes forming one or more vias in the electrical interposer configured to enable an electrical connection between the second portion of the die and at least one additional die at act 940. The method 900 includes connecting an optical element (e.g., FAU 250, 350, 450) to the photonic interposer at act 950.

[0178] FIG. 11 is an embodiment of a method 1000 for manufacturing a circuit package
20 (e.g., circuit package 100, 200, 300, 400, 500). The method 1000 includes connecting a photonic interposer (e.g., photonic interposers 110, 210, 310, 410, 510, 510-2, 510-3) and an electrical interposer (e.g., second interposers 120, 220, 320, 420, 520, and third interposer 520-2) at act 1010. The method 1000 includes connecting an analog-mixed signal portion (e.g., analog-mixed signal portions 132-1, 232-1, 332-1, 432-1, 532-1) of a
25 die (e.g., die 130, 230, 330, 430, 530, 530-2, 530-3, 530-4, 530-5, 530-6) to the photonic interposer at act 1020.

[0179] The method 1000 further includes connecting an electronic portion (e.g., electronic portions 132-2, 232-2, 332-2, 432-2, 532-2) of the die to the electrical interposer at act 1030. The die partially overlaps both the photonic interposer and the electrical
30 interposer. The method 1000 includes connecting an optical element (e.g., FAU 250, 350, 450) to the photonic interposer at act 1040.

[0180] In some embodiments, the method 1000 includes connecting a driver of the analog-mixed signal portion of the die to a modulator of the photonic interposer. The modulator may be any type of modulator, including a thermally stable modulator and/or an

electro-absorption modulator. In some embodiments, the method 1000 includes connecting a TIA of the analog-mixed signal portion of the die to a photodetector of the photonic interposer.

5 [0181] In some embodiments, the method 1000 includes rigidly connecting the photonic interposer and the electrical interposer. The method 1000 may include applying a mold to the photonic interposer and the electrical interposer to form a rigid unit. The mold may be formed from silicon and/or a silicon alloy. In some embodiments, the mold includes a material that matches a thermal expansion of one or more of the photonic interposer and the electrical interposer. In some embodiments, the electrical interposer is formed as a
10 mold. In some embodiments, the electrical interposer includes a through mold via.

[0182] In some embodiments, the electrical interposer includes a bond via array. In some embodiments, the method 1000 includes forming the photonic interposer and the electrical interposer on a carrier. In some embodiments, the method 1000 includes applying redistribution layer to a bottom surface of one or more of the photonic interposer and the
15 electrical interposer. In some embodiments, the photonic interposer and the electrical interposer are debonded from the carrier.

[0183] In some embodiments, the method 1000 includes applying a redistribution layer to the electrical interposer. In some embodiments, the redistribution layer is applied to a top surface of the electrical interposer. In some embodiments, the method 1000 includes
20 attaching the die to the redistribution layer on the top surface of the electrical interposer.

[0184] In some embodiments, a second die is attached to one or more of the photonic interposer and the electrical interposer. In some embodiments, a third die is attached to one or more of the photonic interposer, the electrical interposer, or a third interposer. The third interposer may be a second photonic interposer. In some embodiments, the third interposer
25 is a non-photonic interposer.

[0185] In some embodiments, one or more of the photonic interposer and the third interposer are photonic integrated circuits. In some embodiments, the electrical interposer is an SI interposer. In some embodiments, the electrical interposer is an SI bridge.

[0186] In some embodiments, the method 1000 includes attaching a third die to one or
30 more of the photonic interposer, the electrical interposer, and the third interposer. In some embodiments, the method 1000 includes exposing a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer. In some embodiments, exposing the portion of the top surface of one or more of the photonic

interposer, the electrical interposer, and the third interposer includes one or more of laser drilling, etching, or clearing.

[0187] In some embodiments, the method 1000 includes applying one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer. In some embodiments, applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer includes directly applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer. In some embodiments, directly applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer includes directly applying the one or more optical elements to the exposed portion of the one or more of the photonic interposer, the electrical interposer, and the third interposer.

[0188] In some embodiments, the method includes applying a redistribution layer to a substrate. In some embodiments, the method 1000 includes attaching two or more of photonic interposers, the electrical interposer, and the third interposer to the redistribution layer on the substrate. In some embodiments, the method 1000 includes applying the redistribution layer to a portion of two or more of the photonic interposers, the electrical interposer, and the third interposer. In some embodiments, applying the redistribution layer to the portion of the two or more of the photonic interposer, the electrical interposer, and the third interposer forms a plurality of high precision pads on the two or more of the photonic interposer, the electrical interposer, and the third interposer. In some embodiments, forming the plurality of high precision pads on the two or more of the photonic interposer, the electrical interposer, and the third interposer facilitate connecting the die to the two or more of the photonic interposer, the electrical interposer, and the third interposer. In some embodiments, facilitating connecting the die to the two or more of the photonic interposer, the electrical interposer, and the third interposer includes forming a top surface on the high precision pads that is substantially the same vertical height. In some embodiments, the high precision pads remove the tolerance issues between the two or more of the photonic interposer, the electrical interposer, and the third interposer in one or more of the X-direction, the Y-direction, and the vertical direction.

[0189] One or more specific embodiments of the present disclosure are described herein. These described embodiments are examples of the presently disclosed techniques. Additionally, in an effort to provide a concise description of these embodiments, not all

features of an actual embodiment may be described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous embodiment-specific decisions will be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one embodiment to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

[0190] The articles “a,” “an,” and “the” are intended to mean that there are one or more of the elements in the preceding descriptions. The terms “comprising,” “including,” and “having” are intended to be inclusive and mean that there may be additional elements other than the listed elements. Additionally, it should be understood that references to “one embodiment” or “an embodiment” of the present disclosure are not intended to be interpreted as excluding the existence of additional embodiments that also incorporate the recited features. For example, any element described in relation to an embodiment herein may be combinable with any element of any other embodiment described herein. Numbers, percentages, ratios, or other values stated herein are intended to include that value, and also other values that are “about” or “approximately” the stated value, as would be appreciated by one of ordinary skill in the art encompassed by embodiments of the present disclosure. A stated value should therefore be interpreted broadly enough to encompass values that are at least close enough to the stated value to perform a desired function or achieve a desired result. The stated values include at least the variation to be expected in a suitable manufacturing or production process, and may include values that are within 5%, within 1%, within 0.1%, or within 0.01% of a stated value.

[0191] A person having ordinary skill in the art should realize in view of the present disclosure that equivalent constructions do not depart from the spirit and scope of the present disclosure, and that various changes, substitutions, and alterations may be made to embodiments disclosed herein without departing from the spirit and scope of the present disclosure. Equivalent constructions, including functional “means-plus-function” clauses are intended to cover the structures described herein as performing the recited function, including both structural equivalents that operate in the same manner, and equivalent structures that provide the same function. It is the express intention of the applicant not to invoke means-plus-function or other functional claiming for any claim except for those in which the words ‘means for’ appear together with an associated function. Each addition,

deletion, and modification to the embodiments that falls within the meaning and scope of the claims is to be embraced by the claims.

[0192] The terms “approximately,” “about,” and “substantially” as used herein represent an amount close to the stated amount that still performs a desired function or achieves a desired result. For example, the terms “approximately,” “about,” and “substantially” may refer to an amount that is within less than 5% of, within less than 1% of, within less than 0.1% of, and within less than 0.01% of a stated amount. Further, it should be understood that any directions or reference frames in the preceding description are merely relative directions or movements. For example, any references to “up” and “down” or “above” or “below” are merely descriptive of the relative position or movement of the related elements.

[0193] The present disclosure may be embodied in other specific forms without departing from its spirit or characteristics. The described embodiments are to be considered as illustrative and not restrictive. The scope of the disclosure is, therefore, indicated by the appended claims rather than by the foregoing description. Changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

CLAIMS

What is claimed is:

1. A circuit package, comprising:
a photonic interposer;
5 an electrical interposer;
a die including an analog-mixed signal portion and an electronic portion, the die partially overlapping both the photonic interposer and the electrical interposer, the analog-mixed signal portion connected to the photonic interposer, the electronic portion connected to the electrical interposer; and
10 a plurality of electrical interconnects between the photonic interposer and the die.
2. The circuit package of claim 1, wherein the photonic interposer includes a modulator.
3. The circuit package of claim 2, wherein the modulator is a thermally stable
15 modulator.
4. The circuit package of claim 3, wherein the thermally stable modulator is an electro-absorption modulator (EAM).
5. The circuit package of any of claims 1–4, wherein the analog-mixed signal portion includes a driver.
- 20 6. The circuit package of claim 5, wherein the plurality of electrical interconnects includes a first electrical interconnect connecting the photonic interposer to the analog-mixed signal portion, and wherein the driver is connected to a first end of the first electrical interconnect.
7. The circuit package of claim 6, wherein the photonic interposer includes the
25 modulator of any of claims 2–6, wherein the modulator is connected to a second end of the first electrical interconnect.
8. The circuit package of any of claims 1–7, wherein the photonic interposer includes a photodetector.
9. The circuit package of claim 8, wherein the photodetector includes a photodiode.

10. The circuit package of any of claims 1–9, wherein the analog-mixed signal portion includes a transimpedance amplifier (TIA).
11. The circuit package of claim 10, wherein the plurality of electrical interconnects includes a second electrical interconnect connecting the photonic interposer and the analog-mixed signal portion, and wherein the TIA is connected to a first end of the second electrical interconnect.
12. The circuit package of claim 11, wherein the photonic portion includes the photodetector of any of claims 8 or 9, and wherein the photodetector is connected to a second end of the second electrical interconnect of the plurality of electrical interconnects.
13. The circuit package of any of claims 1–12, further comprising a second die including a processing element, the processing element electrically connected to the electrical interposer.
14. The circuit package of claim 13, wherein the second die is electrically connected to the electronic portion through the electrical interposer.
15. The circuit package of claim 14, wherein the second die is electrically connected to the analog-mixed signal portion through the electronic portion and the electrical interposer.
16. The circuit package of claim 15, wherein the second die is electrically connected to the photonic interposer through the analog-mixed signal portion, the electronic portion, and the electrical interposer.
17. The circuit package of claim 16, wherein the second die is electrically connected to the photonic interposer through a driver in the analog-mixed signal portion.
18. The circuit package of claim 17, wherein the second die is electrically connected to the photonic interposer through a modulator in the photonic interposer.
19. The circuit package of any of claims 16–18, wherein the second die is electrically connected to the photonic interposer through the analog-mixed signal portion, the electronic portion, and the electrical interposer and optically connected to a fiber array unit through the photonic interposer.

20. The circuit package of any of claims 1–19, wherein one or more of the plurality of electrical interconnects are less than 100 microns in length.
21. The circuit package of any of claims 1–20, wherein one or more of the plurality of electrical interconnects is one or more of one or more of soldering bumps, wires, copper pillars, wirebonds, through-substrate vias (TSVs), through-dielectric via (TDVs), re-distribution layers (RDLs), or landing pads.
22. The circuit package of any of claims 1–21, further comprising a fiber array unit (FAU) between the photonic interposer and the die.
23. The circuit package of any of claims 1–22, wherein one or more of the modulator of any of claims 2–7 or the photodetector of any of claims 8 or 9 are connected to the FAU with an FAU connection.
24. The circuit package of claim 23, wherein the FAU connection is a bidirectional channel.
25. The circuit package of claim 24, wherein the bidirectional channel includes one or more waveguides.
26. The circuit package of any of claims 1–25, wherein the photonic interposer includes a photonic integrated circuit.
27. A circuit package, comprising:
a photonic interposer;
a second interposer; and
a die partially overlapping and connected to both the photonic interposer and the second interposer.
28. The circuit package of claim 27, wherein the die partially vertically overlaps both the photonic interposer and the second interposer.
29. The circuit package of any of claims 27 or 28, wherein the second interposer is a non-photonic interposer.
30. The circuit package of any of claims 27–29, wherein the second interposer is a second photonic interposer.

31. The circuit package of any of claims 27–30, wherein one or more of the photonic interposer and the second interposer are photonic integrated circuits.
32. The circuit package of any of claims 27–31, further comprising a third interposer.
33. The circuit package of any of claims 27–32, wherein one or more of the second
5 interposer and the third interposer is an SI interposer.
34. The circuit package of any of claims 27–33, wherein one or more of the second interposer and the third interposer is an SI bridge.
35. The circuit package of any of claims 27–34, wherein two or more of the photonic interposer, the second interposer, and the third interposer are separated by a mold.
- 10 36. The circuit package of any of claims 27–35, wherein two or more of the photonic interposer, the second interposer, and the third interposer are adjacent.
37. The circuit package of any of claims 27–36, wherein two or more of the photonic interposer, the second interposer, and the third interposer are directly adjacent.
38. The circuit package of any of claims 27–37, wherein two or more of the photonic
15 interposer, the second interposer, and the third interposer abut.
39. The circuit package of any of claims 27–38, wherein two or more of the photonic interposer, the second interposer, and the third interposer do not vertically overlap.
40. The circuit package of any of claims 27–39, wherein the die is an ASIC die, a processor die, an ARM processor die, an image processor die, a tensor engine, a neural-
20 compute engine, or combinations thereof.
41. The circuit package of any of claims 27–40, wherein one or more of the photonic interposer and the second interposer are formed of silicon or a silicon alloy.
42. The circuit package of any of claims 27–41, wherein the photonic interposer and the second interposer are laterally surrounded by a mold.
- 25 43. The circuit package of claim 42, wherein the mold formed of silicon or a silicon alloy.

44. The circuit package of any of claims 42 or 43, wherein the mold includes a material that matches a thermal expansion of one or more of the photonic interposer and the second interposer.
45. The circuit package of any of claims 27–44, wherein the second interposer is a mold.
46. The circuit package of claim 45, wherein the second interposer includes a through mold via.
47. The circuit package of any of claims 45 or 46, wherein the second interposer includes a bond via array.
48. The circuit package of any of claims 27–47, further comprising a second die.
49. The circuit package of claim 48, wherein the second die does not vertically overlap the photonic interposer.
50. The circuit package of any of claims 48 or 49, wherein the second die includes general purpose memory.
51. The circuit package of any of claims 48–50, wherein the second die includes a processor.
52. The circuit package of claim 51, wherein the processor is one or more of an image processor, a video processor, and a general purpose processor.
53. The circuit package of any of claims 48–52, wherein the second die includes high bandwidth memory.
54. The circuit package of claim 53, wherein the high bandwidth memory is HBM3.
55. The circuit package of any of claims 27–54, further comprising a third die.
56. The circuit package of claim 55, wherein the third die includes one or more of general purpose memory, high bandwidth memory, HBM3, a processor, an image processor, a video processor, and a general purpose processor.

57. The circuit package of any of claims 55 or 56, wherein the third die does not vertically overlap the photonic interposer.
58. The circuit package of any of claims 55 or 56, wherein the third die vertically overlaps the photonic interposer.
- 5 59. The circuit package of any of claims 55, 56, or 58, wherein the third die vertically overlaps the photonic interposer and the second interposer.
60. The circuit package of any of claims 27–59, further comprising a fourth die.
61. The circuit package of any of claims 27–60, further comprising a second photonic interposer.
- 10 62. The circuit package of any of claims 27–61, further comprising a substrate.
63. The circuit package of claim 62, wherein one or more components described or claimed herein are connected to the substrate.
64. The circuit package of any of claims 27–63, further comprising a redistribution layer.
- 15 65. The circuit package of claim 64, wherein the redistribution layer electrically connects the die to one or more of the second die, the third die, or the fourth die as described or claimed herein.
66. The circuit package of claim 65, wherein the redistribution layer electrically connects to a top surface of the die to a top surface of the one or more of the second die,
20 the third die, or the fourth die as described or claimed herein.
67. The circuit package of any of claims 65 or 66, wherein the redistribution layer electrically connects to a bottom surface of the die to a top surface of the one or more of the second die, the third die, or the fourth die as described or claimed herein.
68. The circuit package of any of claims 65–67, wherein the redistribution layer is about
25 ten microns line per space.
69. The circuit package of any of claims 65–68, wherein the redistribution layer is less than two microns thick in the vertical direction.

70. The circuit package of any of claims 65–69, wherein the redistribution layer is less than two layers thick in the vertical direction.

71. The circuit package of any of claims 27–70, further comprising one or more optical elements.

5 72. The circuit package of claim 71, wherein the one or more optical elements include optical elements are optically connected to one or more of the photonic interposer, the second interposer, the second photonic interposer, the third interposer, and the third photonic interposer as described or claimed herein.

73. The circuit package of any of claims 71 or 72, wherein any redistribution layer
10 material on the one or more of the photonic interposer, the second interposer, the second photonic interposer, the third interposer, and the third photonic interposer as described or claimed herein vertically below at least a portion of the one or more optical elements are omitted or removed.

74. A circuit package, comprising:
15 a photonic interposer;
an electrical interposer;
a first die in an electrically connected to both the photonic and electrical interposers, the first die including an analog-mixed signal portion to enable a first processing element therein to transmit and receive data using the photonic interposer and
20 an electronic portion to enable a second processing element therein to transmit and receive data using the electrical interposer; and
a plurality of vias in the electrical interposer to enable the second processing element to transmit and receive data to one or more additional dies in electrical coupling with the electrical interposer.

25 75. The circuit package of claim 74, wherein the first and second processing elements are selected from the group consisting of a CPU, a GPU, a TPU, a tensor engine, a neural network, an AI accelerator, a router, a memory, a switch, a controller, an ASIC, an image processor, a video processor, and a bus.

76. A method of manufacturing a circuit package, comprising:
30 connecting a photonic interposer and an electrical interposer;

- connecting an analog-mixed signal portion of a die to the photonic interposer;
connecting an electronic portion of the die to the electrical interposer, where the
die partially overlaps both the photonic interposer and the electrical
interposer; and
5 connecting an optical element to the photonic interposer.
77. The method of claim 76, further comprising connecting a driver of the analog-
mixed signal portion of the die to a modulator of the photonic interposer.
- 10 78. The method of claim 77, wherein the modulator is a thermally stable modulator.
79. The method of claim 78, wherein the thermally stable modulator is an electro-
absorption modulator (EAM).
- 15 80. The method of any of claims 76–79, further comprising connecting a TIA of the
analog-mixed signal portion of the die to a photodetector of the photonic
interposer.
81. The method of any of claims 76–80, further comprising electrically connecting a
20 second die to the electrical interposer.
82. The method of claim 81, further comprising electrically connecting the second die
to the electrical portion through the electrical interposer.
- 25 83. The method of claim 82, further comprising electrically connecting the second die
to the analog-mixed signal portion through the electrical portion and the electrical
interposer.
84. The method of claim 83, further comprising electrically connecting the second die
30 to the photonic interposer through the analog-mixed signal portion, the electrical
portion, and the electrical interposer.

85. The method of any of claims 83 or 84, wherein electrically connecting the second die to the photonic interposer includes electrically connecting the second die to the photonic interposer through a driver in the analog-mixed signal portion.
- 5 86. The method of claim 85, wherein electrically connecting the second die to the photonic interposer includes electrically connecting the second die to the photonic interposer through a modulator in the photonic interposer.
87. The method of any of claims 83–86, wherein electrically connecting the second
10 die to the photonic interposer includes electrically connecting the second die to the photonic interposer through a transimpedance amplifier (TIA) in the analog-mixed signal portion.
88. The method of claim 87, wherein electrically connecting the second die to the
15 photonic interposer includes electrically connecting the second die to the photonic interposer through a photodetector in the photonic interposer.
89. The method of any of claims 83–88, further comprising optically connecting the second die to a fiber array unit through the photonic interposer and electrically
20 connecting the second die to the photonic interposer through the analog-mixed signal portion, the electrical portion, and the electrical interposer.
90. The method of any of claims 76–89, further comprising rigidly connecting the photonic interposer and the electrical interposer.
- 25 91. The method of any of claims 76–90, further comprising applying a mold to the photonic interposer and the electrical interposer to form a rigid unit.
92. The method of claim 91, wherein the mold includes a silicon or a silicon alloy.
- 30 93. The method of any of claims 91 or 92, wherein the mold includes a material that matches a thermal expansion of one or more of the photonic interposer and the electrical interposer.

94. The method of any of claims 76–93, further comprising forming the electrical interposer as a mold.
95. The method of any of claims 76–94, wherein the electrical interposer includes a
5 through mold via.
96. The method of any of claims 76–95, wherein the electrical interposer includes a bond via array.
- 10 97. The method of any of claims 76–96, further comprising forming the photonic interposer and the electrical interposer on a carrier.
98. The method of any of claims 76–97, further comprising applying redistribution layer to a bottom surface of one or more of the photonic interposer and the
15 electrical interposer.
99. The method of any of claims 97 or 98, further comprising debonding the photonic interposer and the electrical interposer from the carrier.
- 20 100. The method of any of claims 76–99, further comprising applying redistribution layer to the electrical interposer.
101. The method of any of claims 76–99, further comprising applying a redistribution layer to a top surface of the electrical interposer.
- 25 102. The method of claim 101, further comprising attaching the die to the redistribution layer on the top surface of the electrical interposer.
103. The method of any of claims 76–102, further comprising attaching a second die to
30 one or more of the photonic interposer and the electrical interposer.
104. The method of any of claims 76–103, further comprising attaching a third die to one or more of the photonic interposer, the electrical interposer, or a third interposer.

105. The method of claim 104, wherein the third interposer is a second photonic interposer.
- 5 106. The method of claim 105, wherein the third interposer is a non-photonic interposer.
107. The method of any of claims 76–103 or 104–106, wherein one or more of the photonic interposer and the third interposer are photonic integrated circuits.
- 10 108. The method of any of claims 76–107, wherein the electrical interposer is an SI interposer.
109. The method of any of claims 76–108, wherein the electrical interposer is an SI bridge.
- 15 110. The method of any of claims 76–103 or 104–109, further comprising attaching a third die to one or more of the photonic interposer, the electrical interposer, and the third interposer.
- 20 111. The method of any of claims 76–103 or 104–110, further comprising exposing a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer.
- 25 112. The method of claim 111, wherein exposing the portion of the top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer includes one or more of laser drilling, etching, or clearing.
- 30 113. The method of any of claims 76–103 or 104–111, further comprising applying one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer.
114. The method of claim 113, wherein applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical

interposer, and the third interposer includes directly applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer.

- 5 115. The method of claim 114, wherein directly applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the electrical interposer, and the third interposer includes directly applying the one or more optical elements to the exposed portion of any of claims 102–109 of the one or more of the photonic interposer, the electrical interposer, and the third interposer.
- 10 116. The method of any of claims 76–115, further comprising applying redistribution layer to a substrate.
- 15 117. The method of any of claims 76–116, further comprising attaching two or more of the photonic interposer of any of claims 87–115, the electrical interposer of any of claims 87–115, and the third interposer of any of claims 103–115 to the redistribution layer of claim 115 on the substrate of claim 115.
- 20 118. The method of any of claims 76–117, further comprising applying redistribution layer to a portion of two or more of the photonic interposer of any of claims 87–117, the electrical interposer of any of claims 87–117, and the third interposer of any of claims 103–117.
- 25 119. The method of claim 118, wherein the act of applying the redistribution layer to the portion of the two or more of the photonic interposer, the electrical interposer, and the third interposer forms a plurality of high precision pads on the two or more of the photonic interposer, the electrical interposer, and the third interposer.
- 30 120. The method of claim 119, wherein the act of forming the plurality of high precision pads on the two or more of the photonic interposer, the electrical interposer, and the third interposer facilitate connecting the die to the two or more of the photonic interposer, the electrical interposer, and the third interposer.

121. The method of claim 120, wherein the act of facilitating connecting the die to the two or more of the photonic interposer, the electrical interposer, and the third interposer includes forming a top surface on the high precision pads that is substantially the same vertical height.
- 5
122. The method of any of claims 120 or 121, wherein the high precision pads remove the tolerance issues between the two or more of the photonic interposer, the electrical interposer, and the third interposer in one or more of the X-direction, the Y-direction, and the vertical direction.
- 10
123. A method of manufacturing a circuit package, comprising:
connect a photonic interposer and a second interposer;
connect a die to both the photonic interposer and the second interposer, where the
die partially overlaps both the photonic interposer and the second
15 interposer; and
connect an optical element to the photonic interposer.
124. The method of claim 123, further comprising rigidly connecting the photonic interposer and the second interposer.
- 20
125. The method of any of claims 123 or 124, further comprising applying a mold to the photonic interposer and the second interposer to form a rigid unit.
126. The method of claim 125, wherein the mold includes a silicon or a silicon alloy.
- 25
127. The method of any of claims 125 or 126, wherein the mold includes a material that matches a thermal expansion of one or more of the photonic interposer and the second interposer.
- 30
128. The method of any of claims 123–127, further comprising forming the second interposer as a mold.
129. The method of any of claims 123–128, wherein the second interposer includes a through mold via.

130. The method of any of claims 123–129, wherein the second interposer includes a bond via array.
- 5 131. The method of any of claims 123–130, further comprising forming the photonic interposer and the second interposer on a carrier.
132. The method of any of claims 123–131, further comprising applying redistribution layer to a bottom surface of one or more of the photonic interposer and the second
10 interposer.
133. The method of any of claims 131 or 132, further comprising debonding the photonic interposer and the second interposer from the carrier.
- 15 134. The method of any of claims 123–133, further comprising applying redistribution layer to the second interposer.
135. The method of any of claims 123–134, further comprising applying redistribution layer to a top surface of the second interposer.
20
136. The method of claim 135, further comprising attaching the die to the redistribution layer on the top surface of the second interposer.
137. The method of any of claims 123–136, further comprising attaching a second die
25 to one or more of the photonic interposer and the second interposer.
138. The method of any of claims 123–137, further comprising attaching a third die to one or more of the photonic interposer, the second interposer, or a third interposer.
139. The circuit package of any of claims 123–138, wherein the second interposer is a
30 second photonic interposer.
140. The method of any of claims 123–138, wherein the second interposer is a non-photonic interposer.

141. The method of any of claims 123–140, wherein one or more of the photonic interposer and the second interposer are photonic integrated circuits.
142. The method of any of claims 123–141, wherein one or more of the photonic interposer and the second interposer are photonic integrated circuits.
143. The method of any of claims 123–142, wherein the second interposer is an SI interposer.
144. The method of any of claims 123–143, wherein the second interposer is an SI bridge.
145. The method of any of claims 123–144, further comprising attaching a third die to one or more of the photonic interposer, the second interposer, and the third interposer.
146. The method of any of claims 123–145, further comprising exposing a portion of a top surface of one or more of the photonic interposer, the second interposer, and the third interposer.
147. The method of claim 146, wherein exposing the portion of the top surface of one or more of the photonic interposer, the second interposer, and the third interposer includes one or more of laser drilling, etching, or clearing.
148. The method of any of claims 123–147 further comprising applying one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the second interposer, and the third interposer.
149. The method of claim 148, wherein applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the second interposer, and the third interposer includes directly applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the second interposer, and the third interposer.

150. The method of claim 149, wherein directly applying the one or more optical elements to a portion of a top surface of one or more of the photonic interposer, the second interposer, and the third interposer includes directly applying the one or more optical elements to the exposed portion of claim 124 of the one or more of the photonic interposer, the second interposer, and the third interposer.
151. The method of any of claims 123–150, further comprising applying redistribution layer to a substrate.
152. The method of claim 151, further comprising attaching two or more of the photonic interposer, the second interposer, and the third interposer to the redistribution layer on the substrate.
153. The method of any of claims 123–152, further comprising applying redistribution layer to a portion of two or more of the photonic interposer, the second interposer, and the third interposer.
154. The method of claim 153, wherein applying redistribution layer to a portion of two or more of the photonic interposer, the second interposer, and the third interposer forms a plurality of high precision pads on two or more of the photonic interposer, the second interposer, and the third interposer.
155. The method of claim 154, wherein forming the plurality of high precision pads on two or more of the photonic interposer, the second interposer, and the third interposer facilitate connecting the die to the two or more of the photonic interposer, the second interposer, and the third interposer.
156. The method of claim 155, wherein facilitating connecting the die to the two or more of the photonic interposer, the second interposer, and the third interposer includes forming a top surface on the high precision pads that is substantially the same vertical height.
157. The method of any of claims 155 or 156, wherein the high precision pads remove the tolerance issues between two or more of the photonic interposer, the second

interposer, and the third interposer in one or more of the X-direction, the Y-direction, and the vertical direction.

158. A method of manufacturing a circuit package, comprising:
- 5 connect a photonic interposer and an electrical interposer;
receive a die partitioned into first and second portions;
connect the first portion of the die to the photonic interposer and the second
portion of the die to the electrical interposer;
form one or more vias in the electrical interposer configured to enable an
10 electrical connection between the second portion of the die and at least one
additional die; and
connect an optical element to the photonic interposer.
159. The method of claim 158, wherein the optical element is selected from the group
15 consisting of a fiber array unit, a fiber, a multi-core fiber, a waveguide, an edge coupler,
and an optical cable.