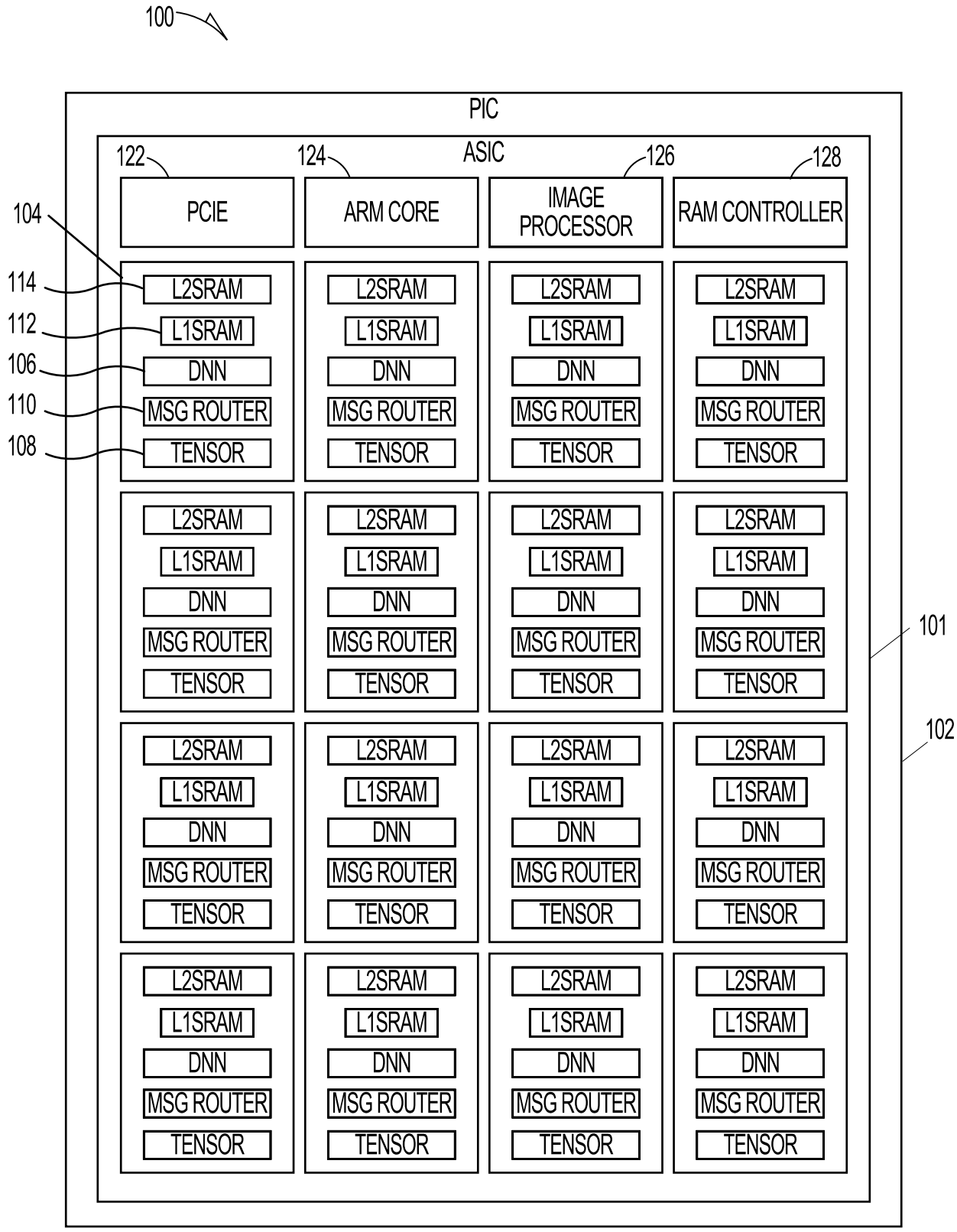

100
PIC
ASIC
122
124
126
128
PCIE
ARM CORE
IMAGE PROCESSOR
RAM CONTROLLER
104
114
112
106
110
108
L2SRAM
L1SRAM
DNN
MSG ROUTER
TENSOR
101
102

FIG. 1A

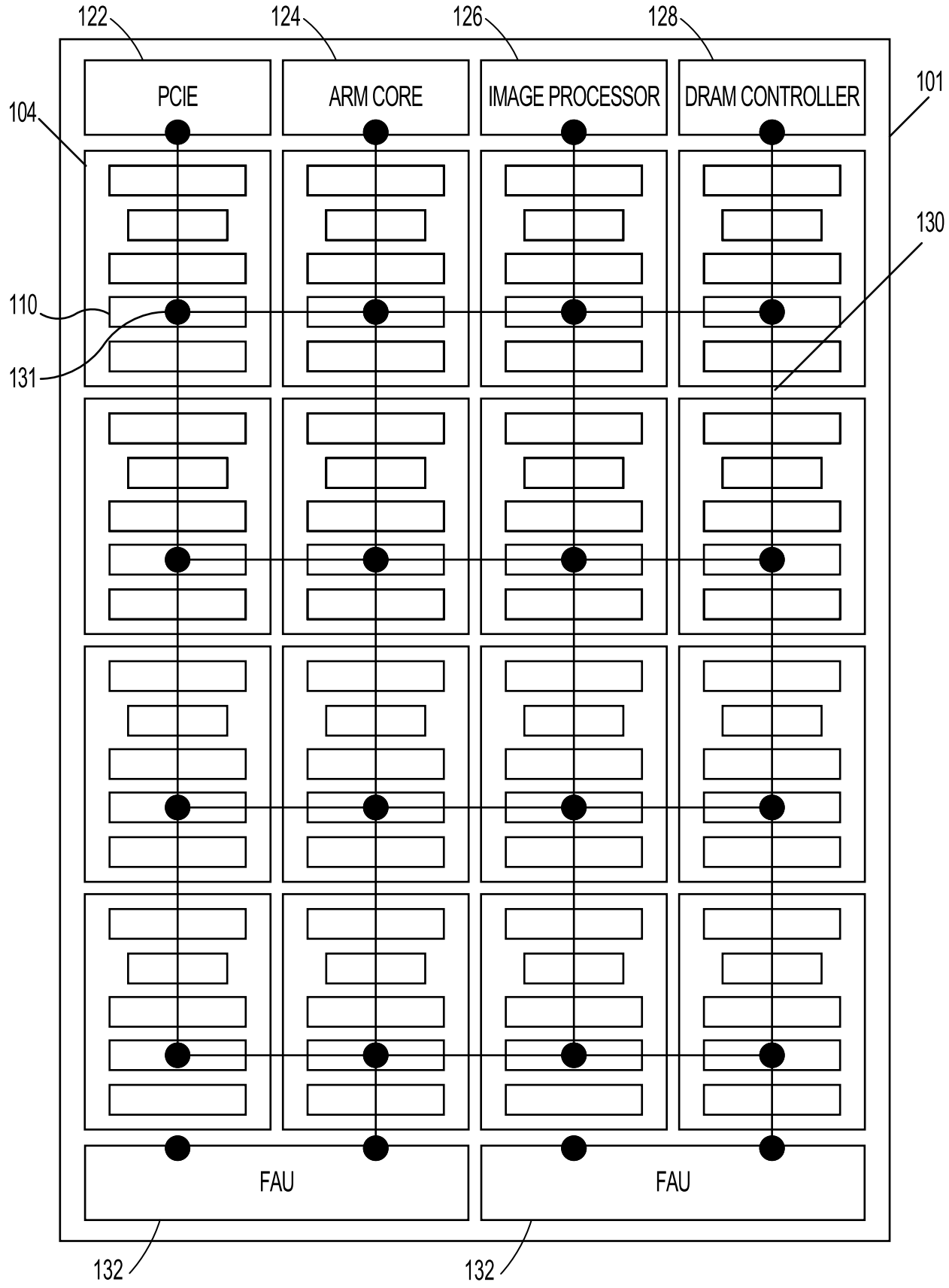

122
124
126
128
PCIE
ARM CORE
IMAGE PROCESSOR
DRAM CONTROLLER
101
104
130
110
131
FAU
FAU
132
132

FIG. 1B

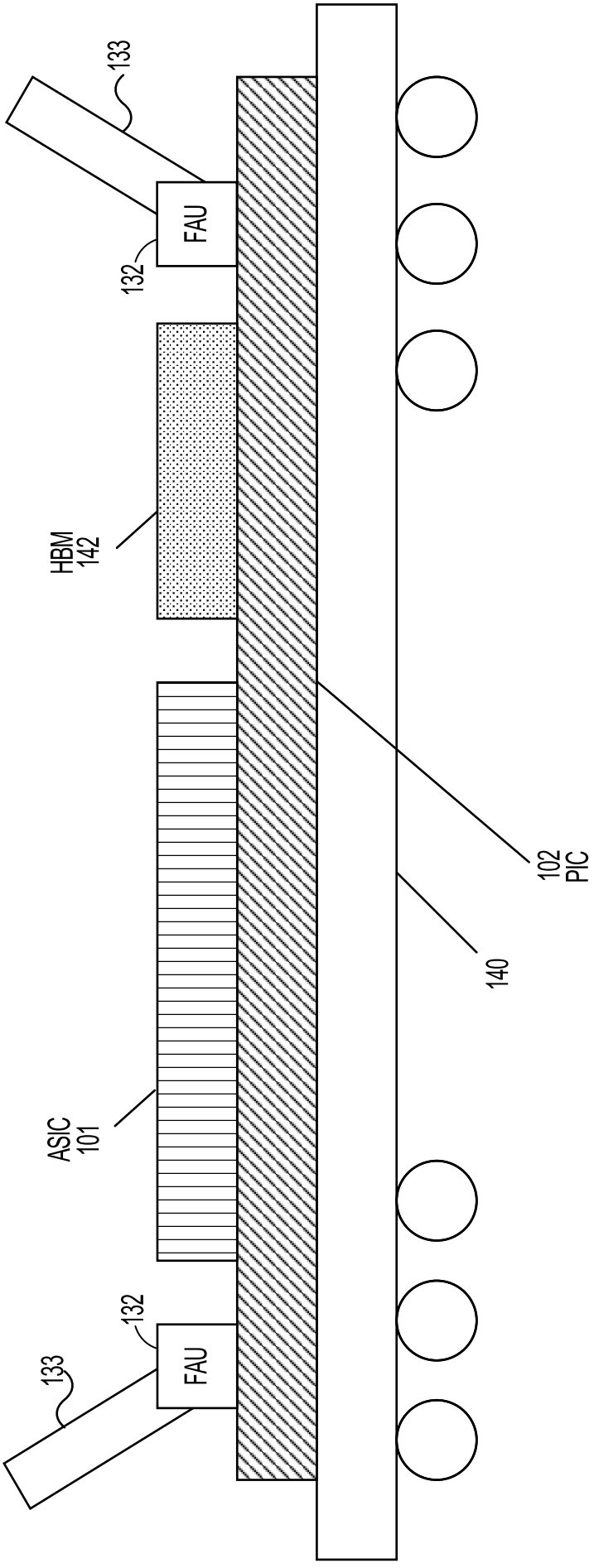


FIG. 1C

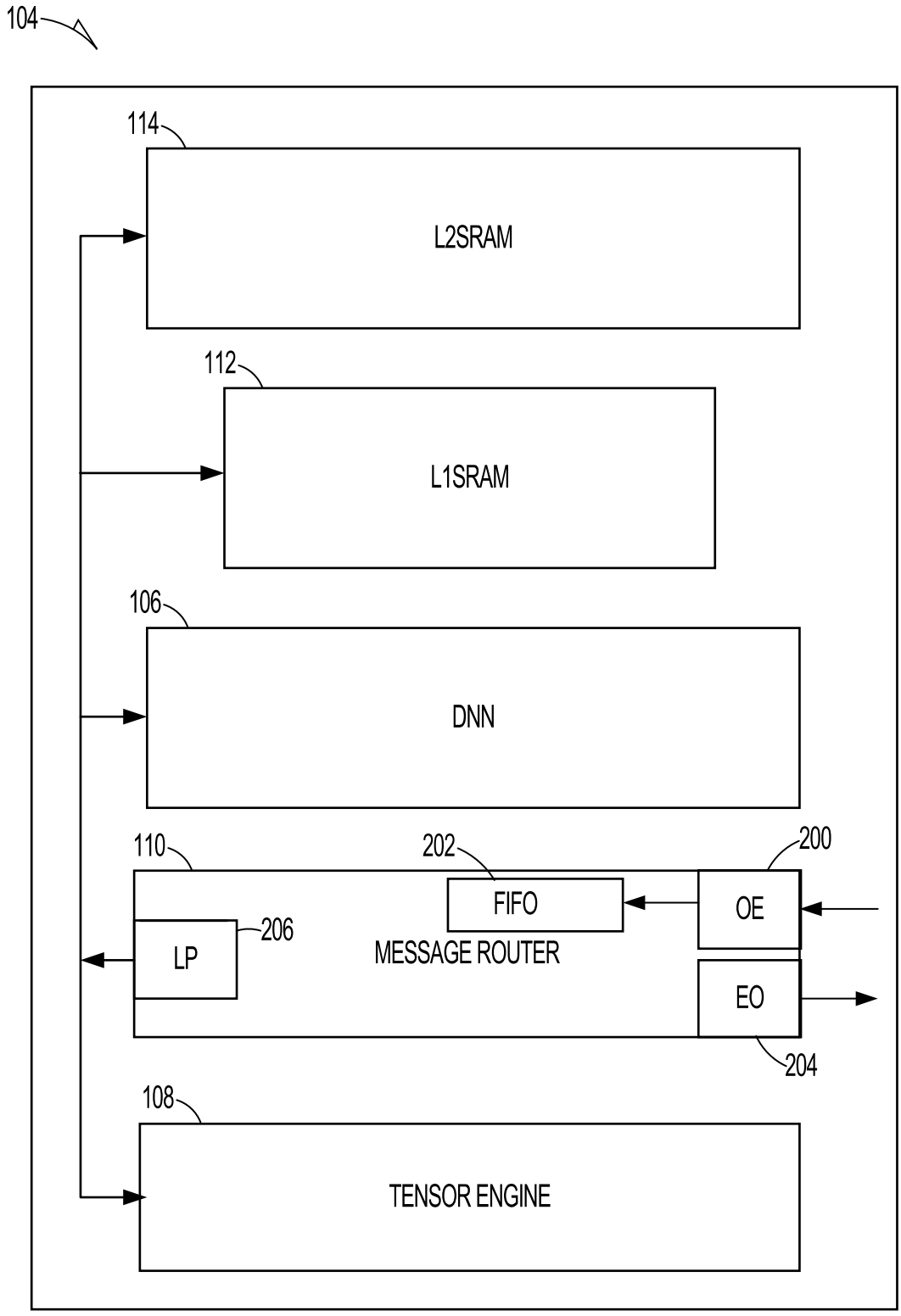

104
114
L2SRAM
112
L1SRAM
106
DNN
110
202
200
FIFO
OE
206
LP
MESSAGE ROUTER
EO
204
108
TENSOR ENGINE

FIG. 2A

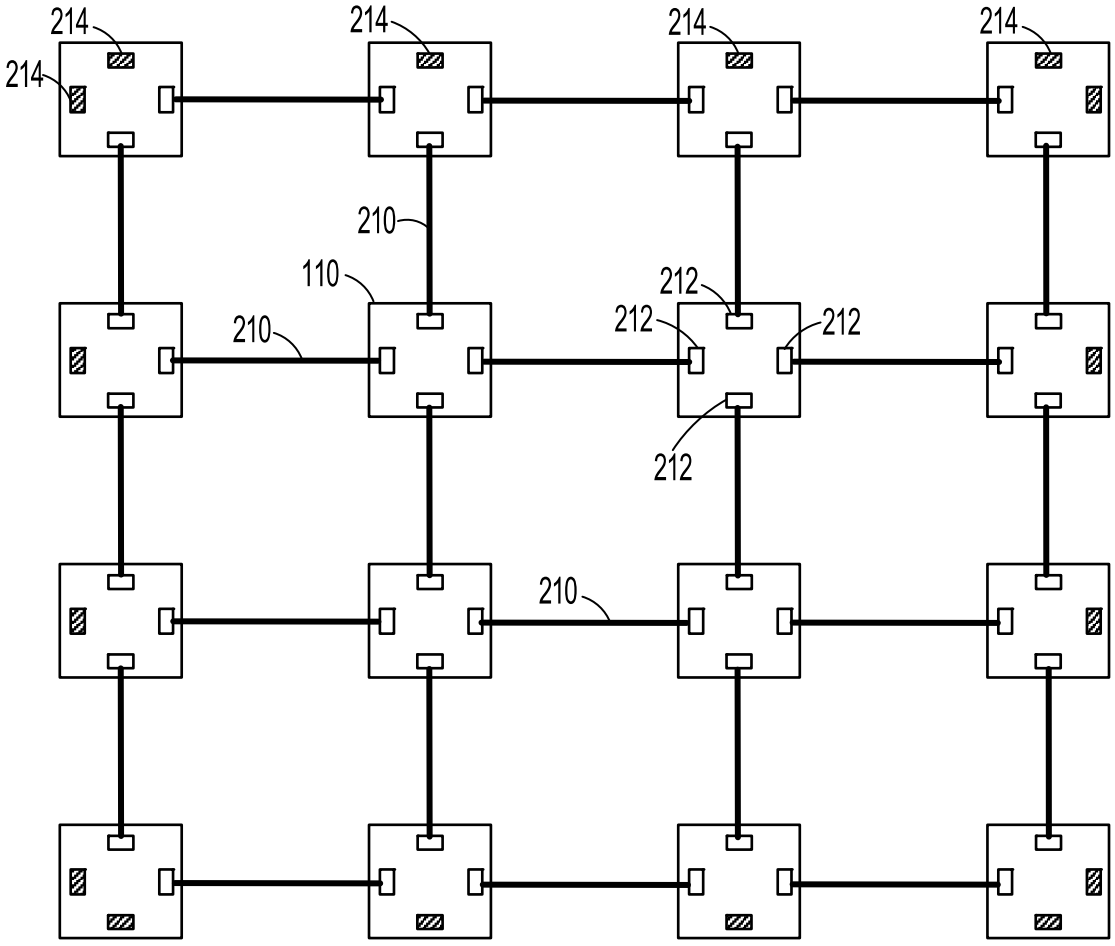


FIG. 2B

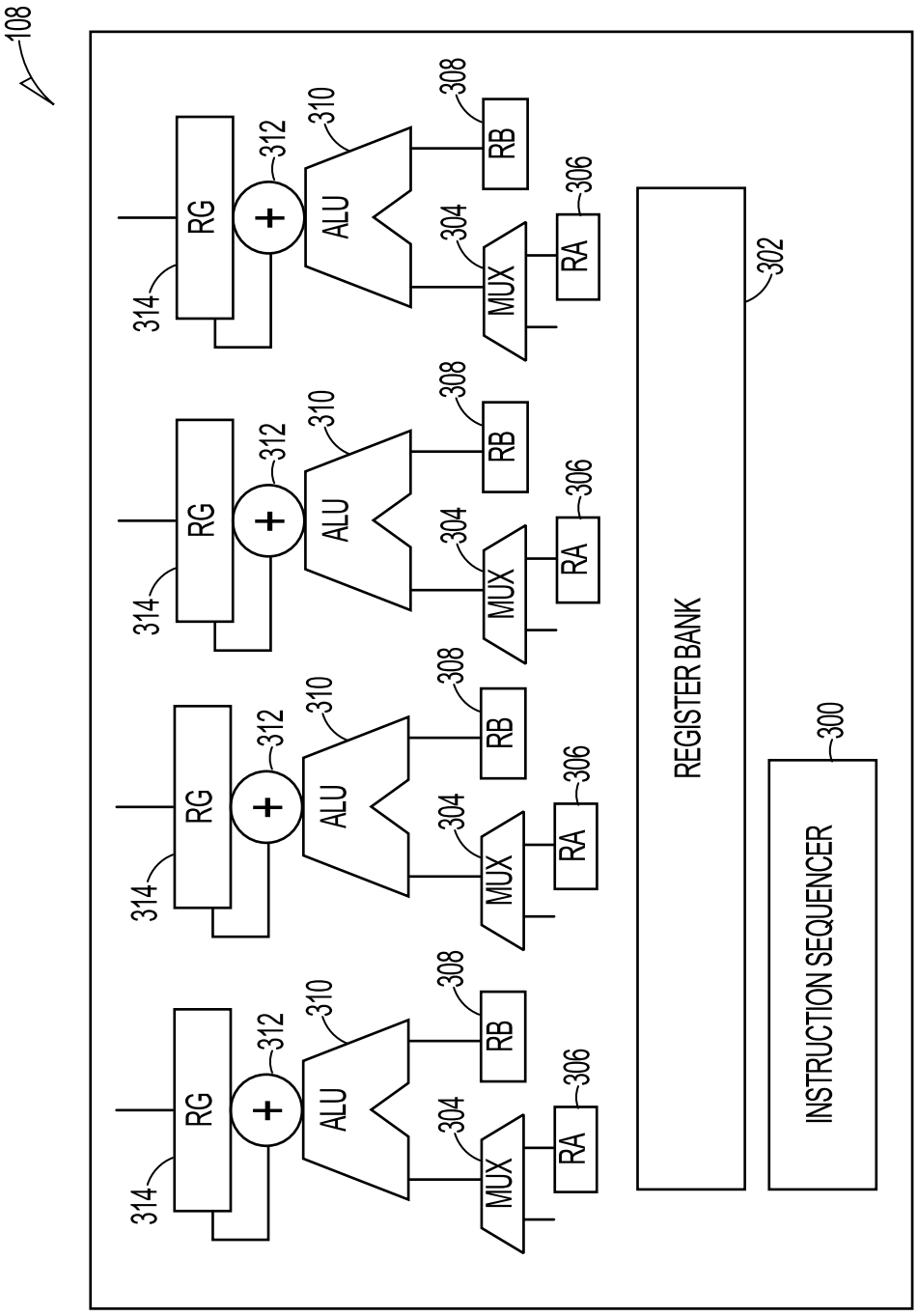

108
RG
+
ALU
MUX
RA
RB
REGISTER BANK
INSTRUCTION SEQUENCER
300
302
304
306
308
310
312
314

FIG. 3

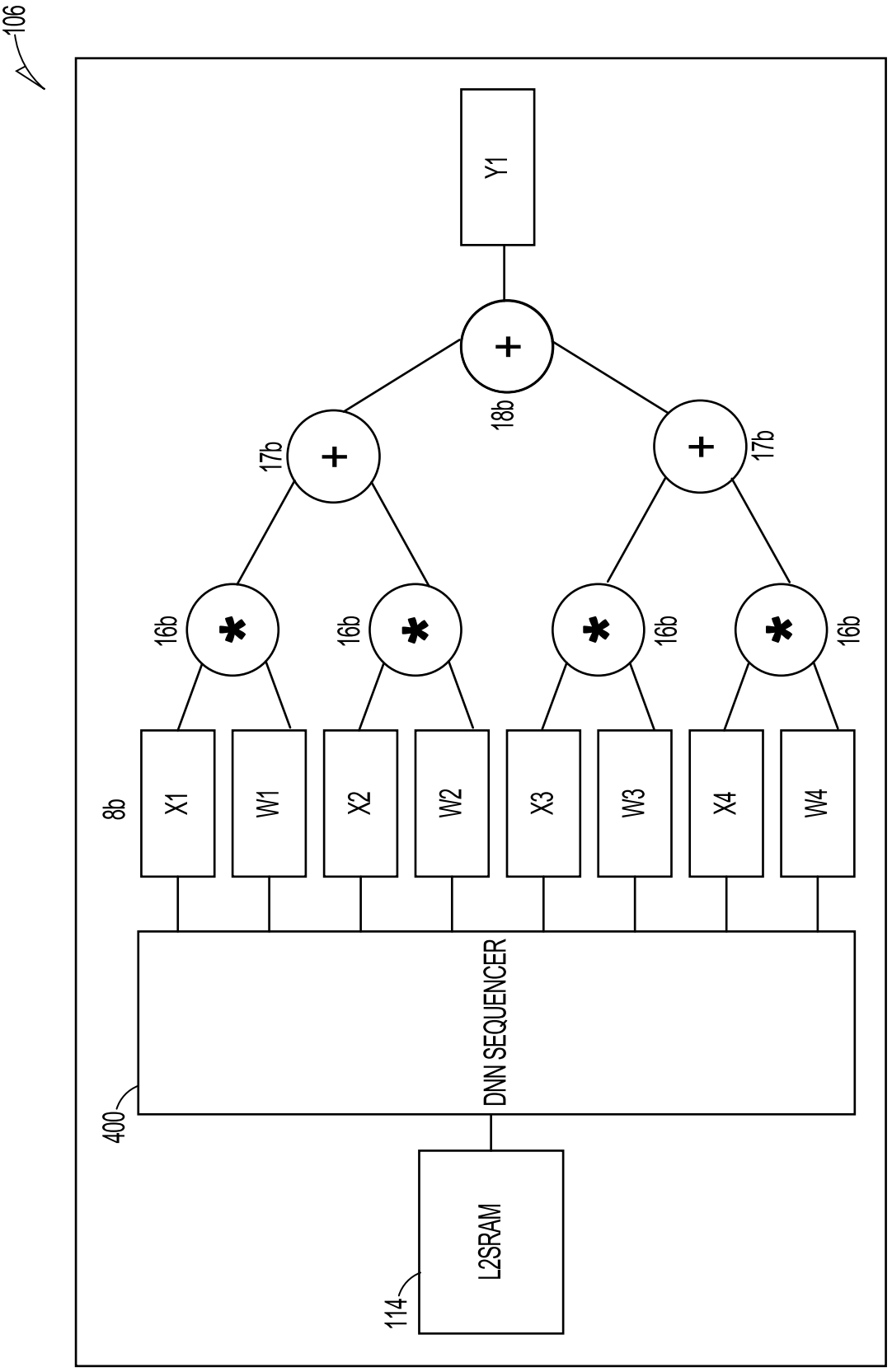

106
Y1
+
18b
17b
+
+
17b
16b
*
16b
*
16b
*
16b
*
8b
X1
W1
X2
W2
X3
W3
X4
W4
DNN SEQUENCER
400
L2SRAM
114

FIG. 4

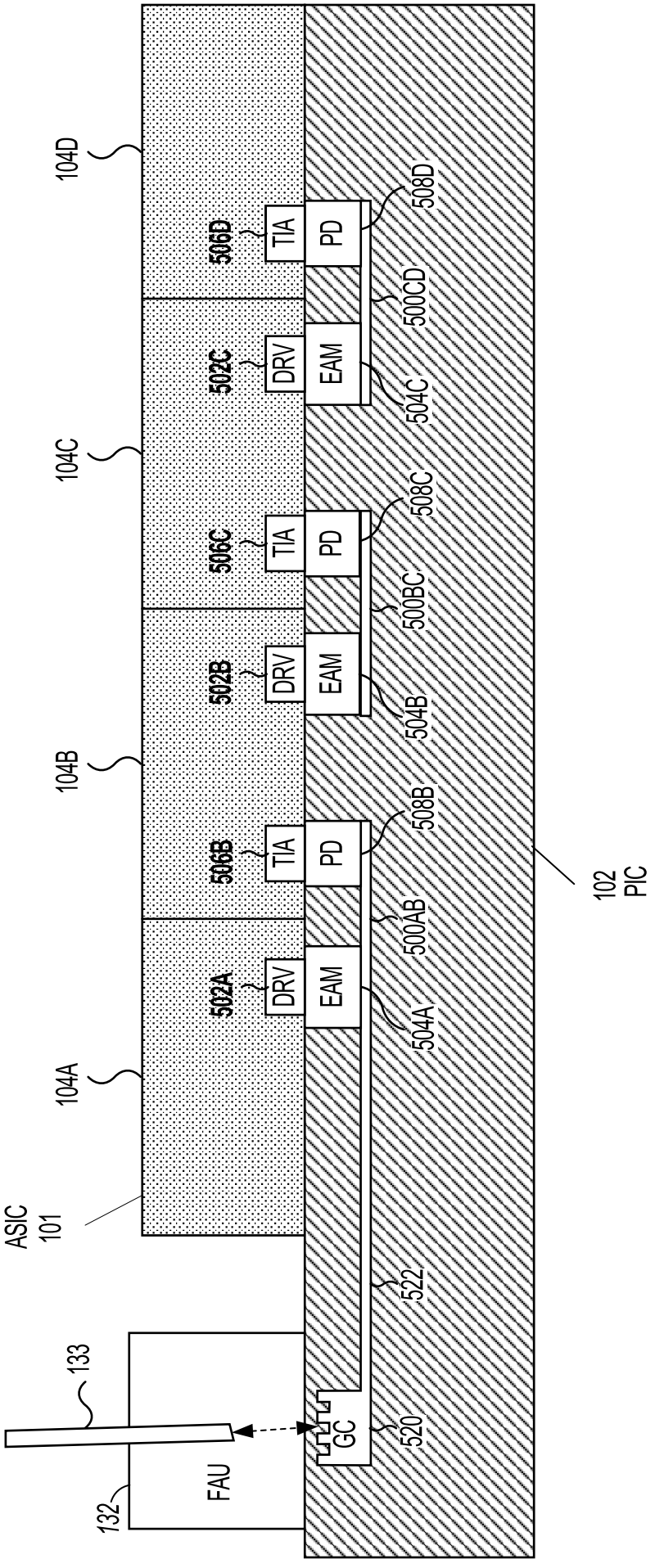

104D
104C
104B
104A
502A
502B
502C
506B
506C
506D
DRV
EAM
TIA
PD
504A
504B
504C
500AB
500BC
500CD
508B
508C
508D
520
522
GC
133
FAU
132
ASIC
101
102
PIC

FIG. 5A

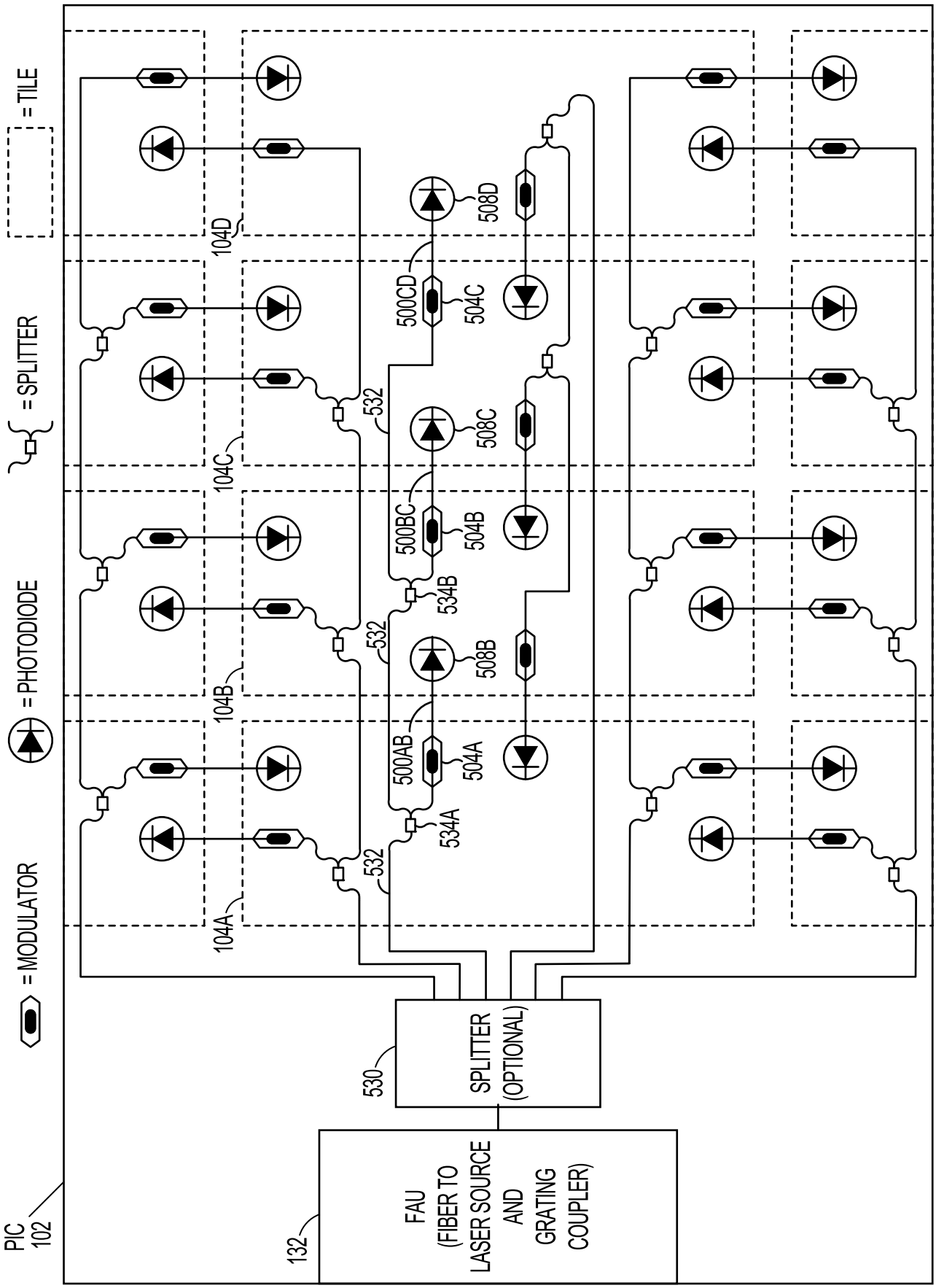

= MODULATOR
= PHOTODIODE
= SPLITTER
= TILE
PIC
102
FAU
(FIBER TO
LASER SOURCE
AND
GRATING
COUPLER)
132
SPLITTER
(OPTIONAL)
530
104A
104B
104C
104D
532
534A
534B
500AB
500BC
500CD
504A
504B
504C
508B
508C
508D

FIG. 5B

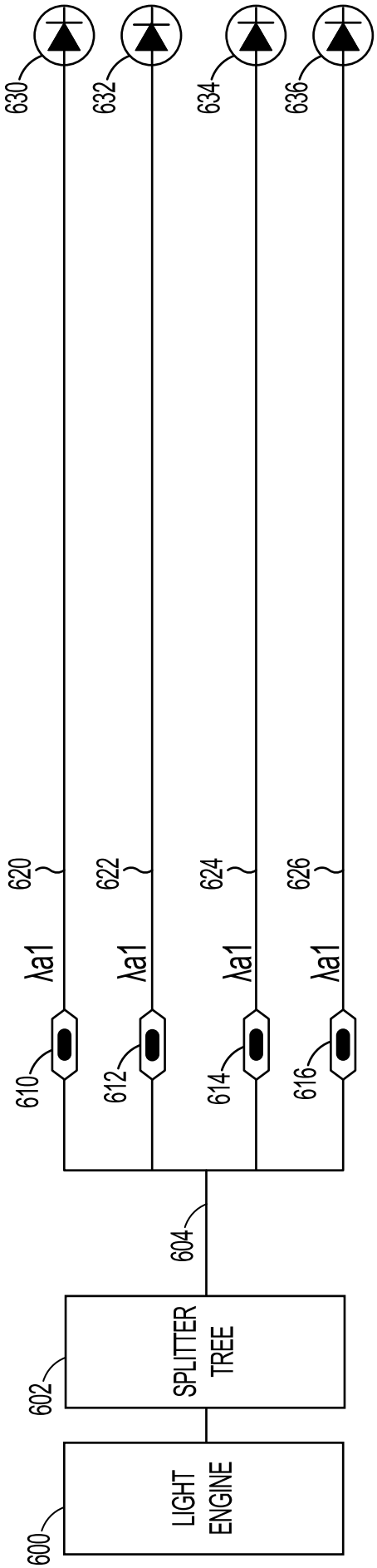


FIG. 6A
(ON-CHIP, NO WDM)

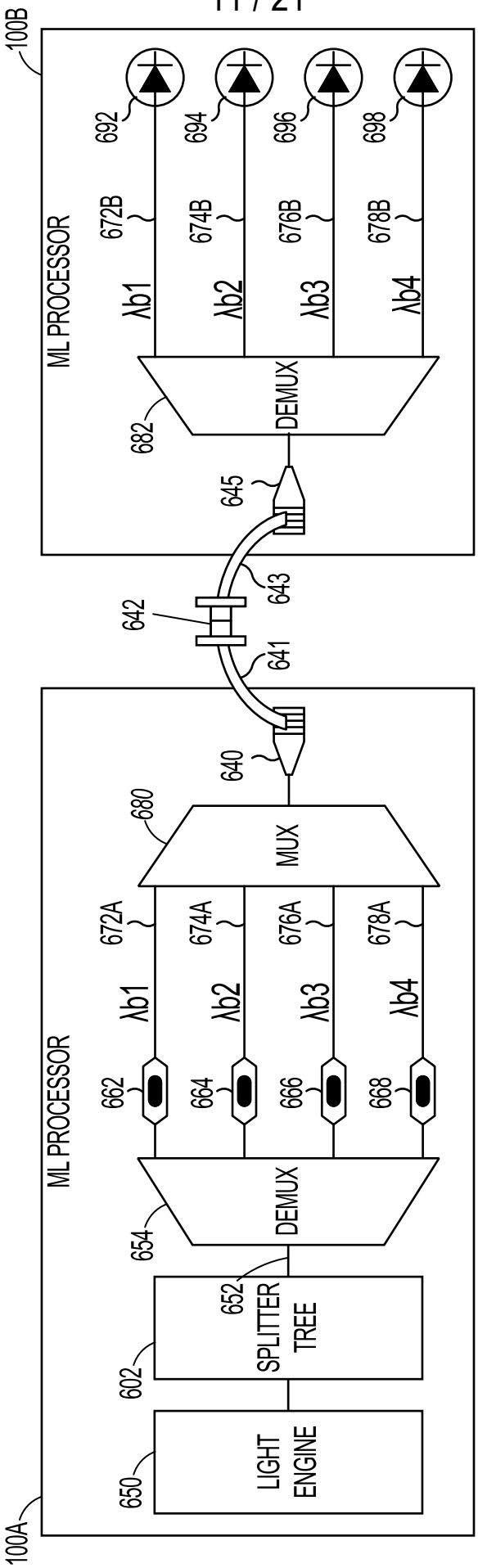


FIG. 6B
(CHIP-TO-CHIP, WDM)

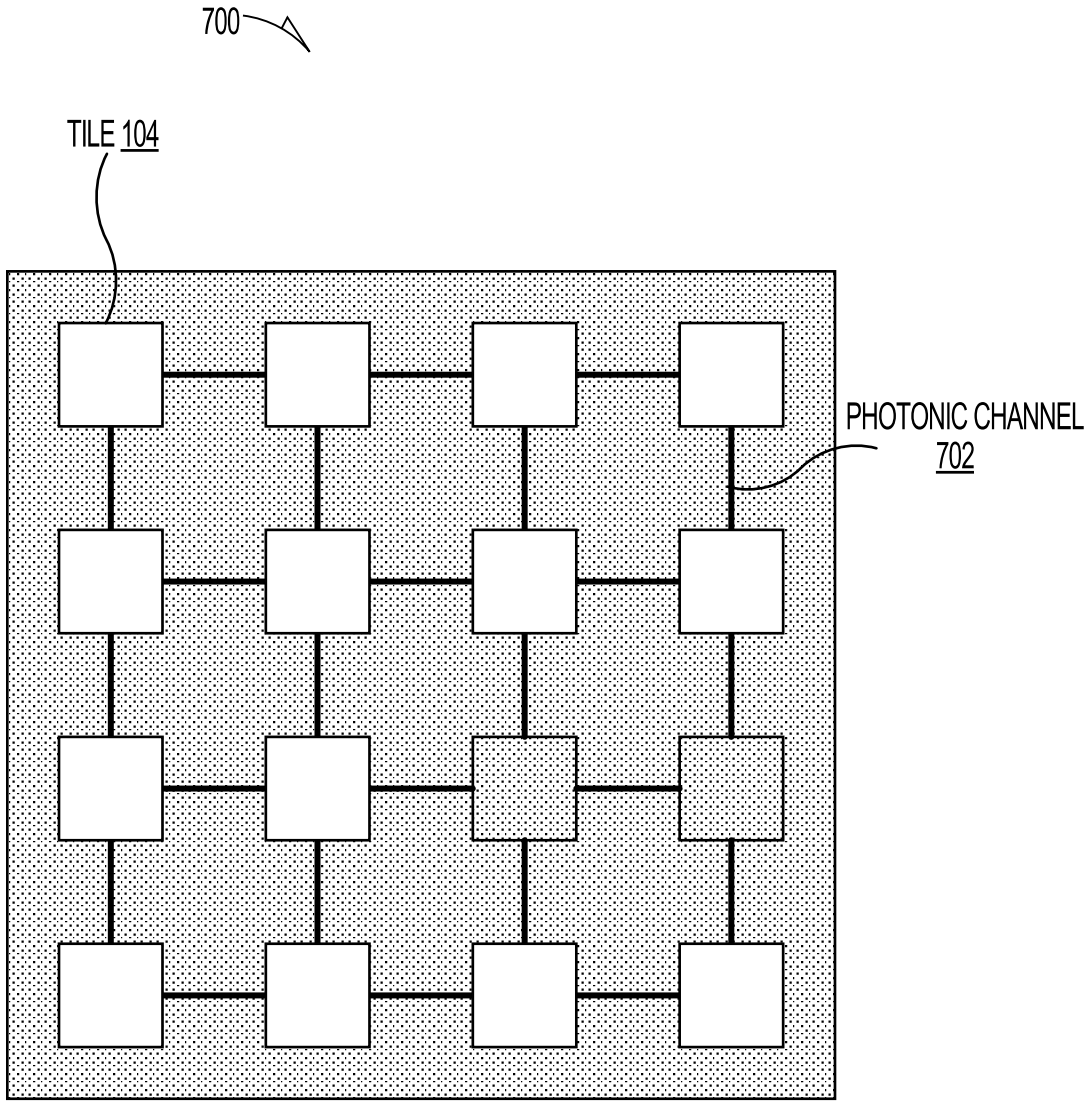


FIG. 7

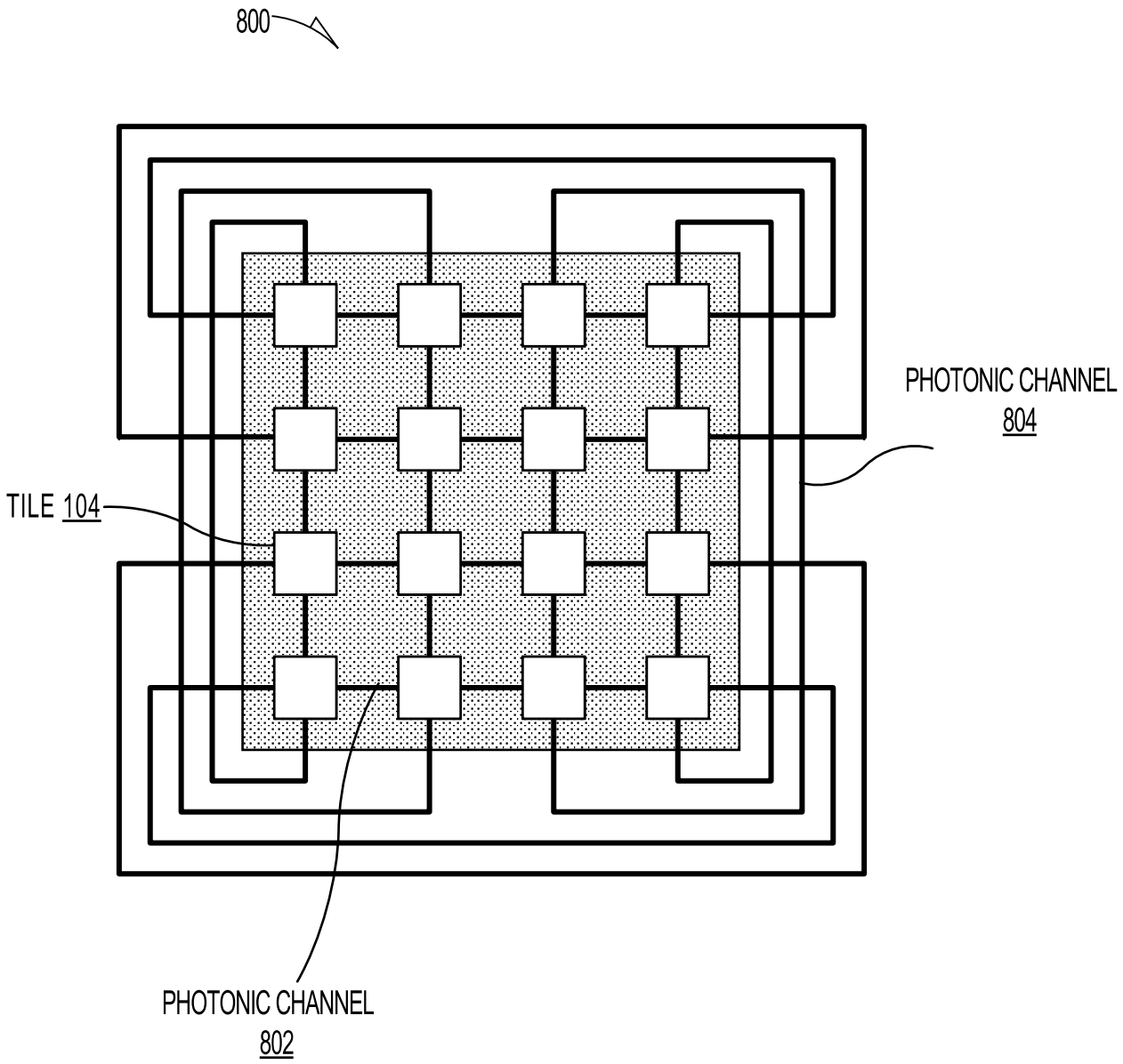


FIG. 8

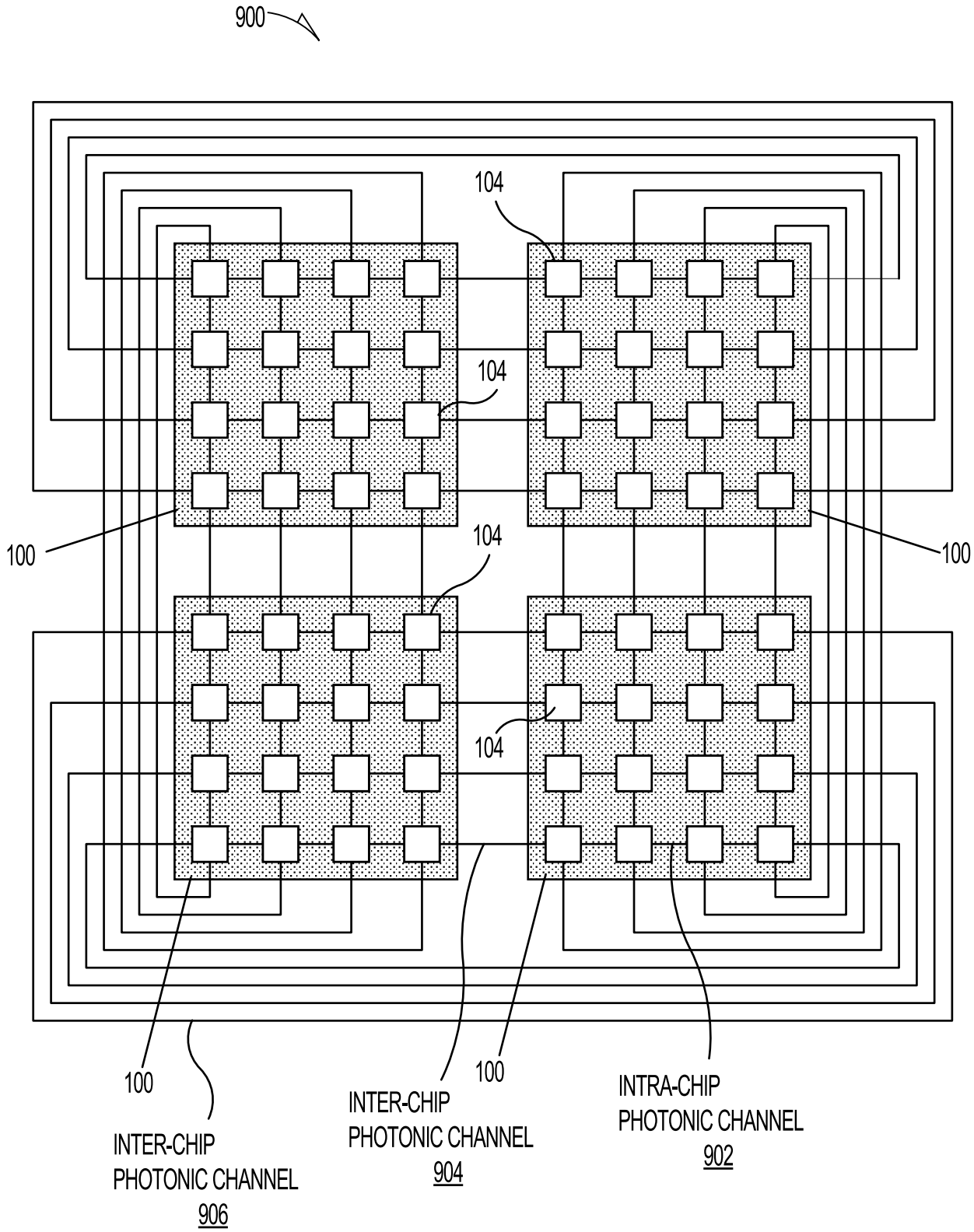

900
104
104
104
104
100
100
100
100
INTER-CHIP
PHOTONIC CHANNEL
906
INTER-CHIP
PHOTONIC CHANNEL
904
INTRA-CHIP
PHOTONIC CHANNEL
902

FIG. 9

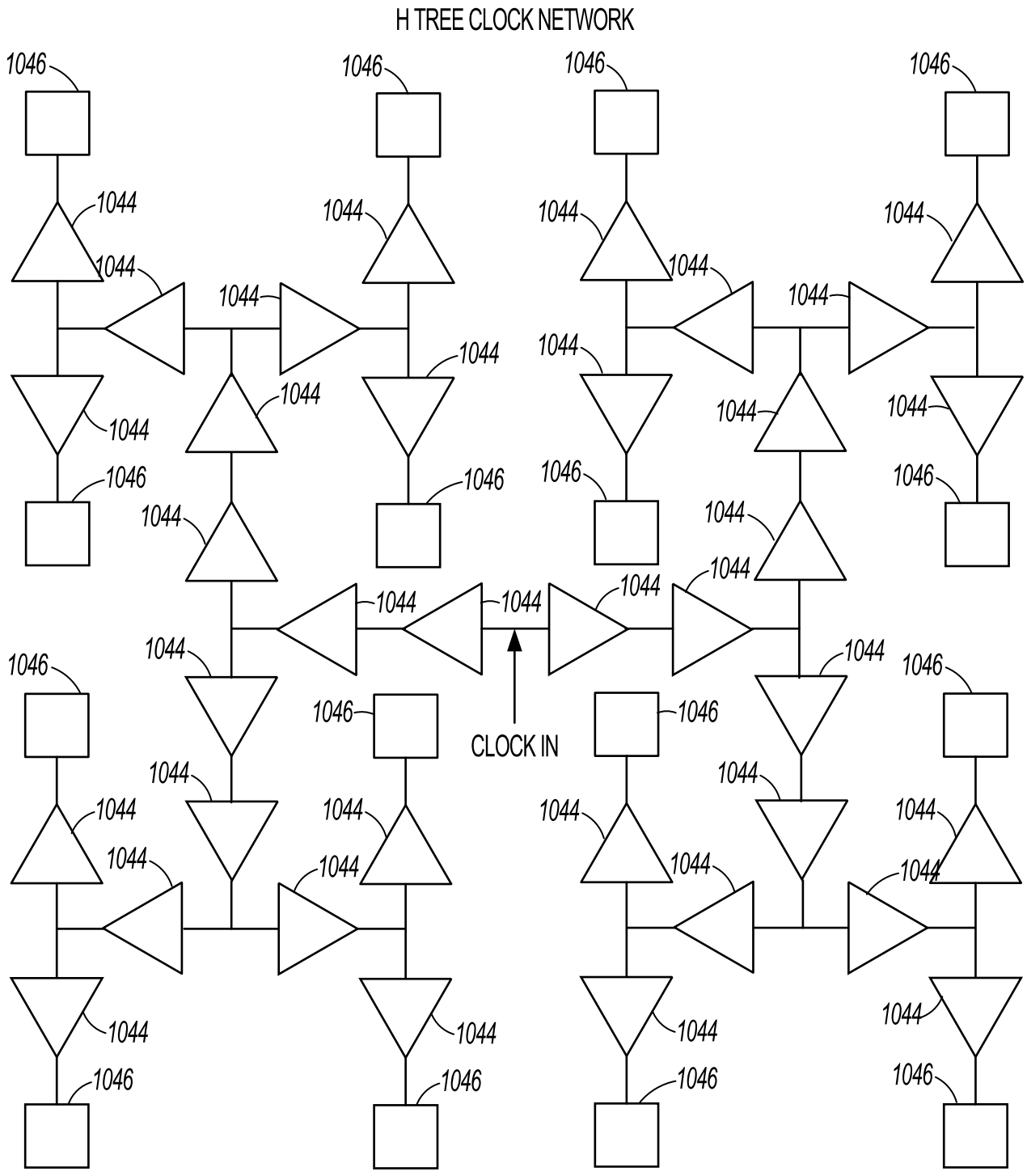


FIG. 10
(PRIOR ART)

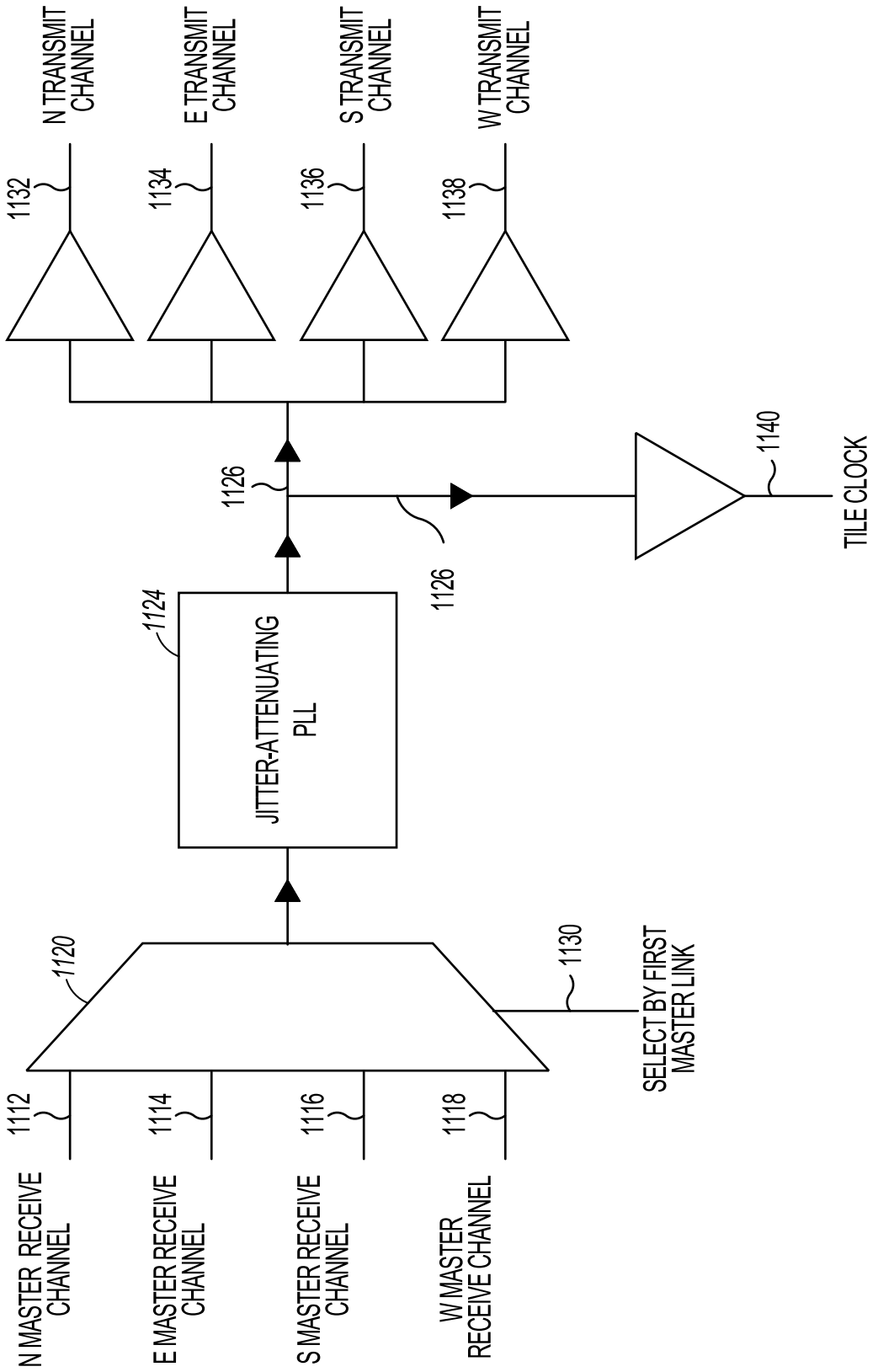

N TRANSMIT CHANNEL
E TRANSMIT CHANNEL
S TRANSMIT CHANNEL
W TRANSMIT CHANNEL
1132
1134
1136
1138
1126
1140
TILE CLOCK
1126
1124
JITTER-ATTENUATING PLL
1120
1130
SELECT BY FIRST MASTER LINK
1112
1114
1116
1118
N MASTER RECEIVE CHANNEL
E MASTER RECEIVE CHANNEL
S MASTER RECEIVE CHANNEL
W MASTER RECEIVE CHANNEL

FIG. 11

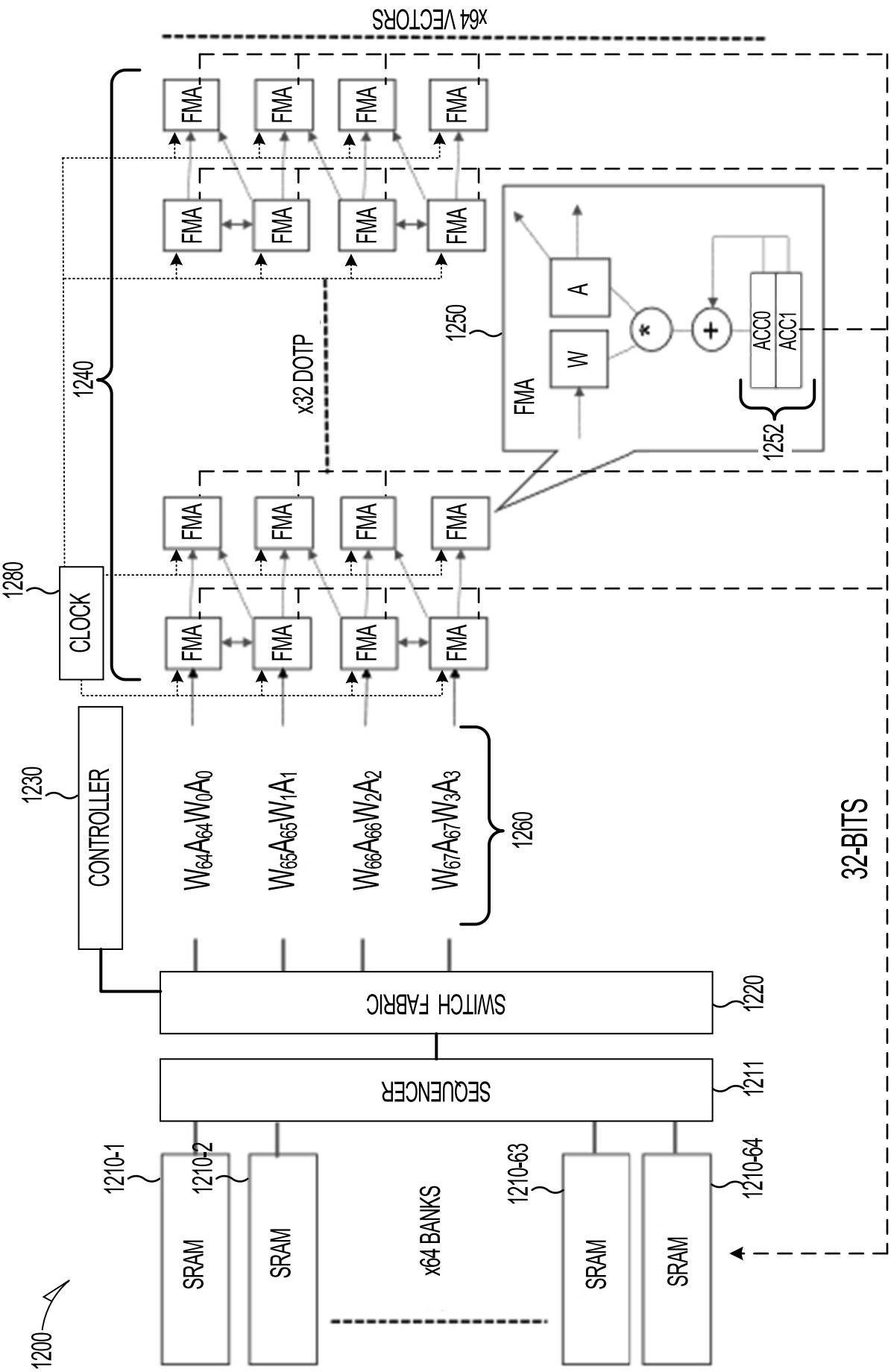

1200
SRAM
SRAM
x64 BANKS
SRAM
SRAM
1210-1
1210-2
1210-63
1210-64
SEQUENCER
1211
SWITCH FABRIC
1220
CONTROLLER
1230
CLOCK
1280
1240
x64 VECTORS
FMA
x32 DOTP
1250
A
W
ACC0
ACC1
1252
1260
$W_{64}A_{64}W_0A_0$
$W_{65}A_{65}W_1A_1$
$W_{66}A_{66}W_2A_2$
$W_{67}A_{67}W_3A_3$
32-BITS

FIG. 12

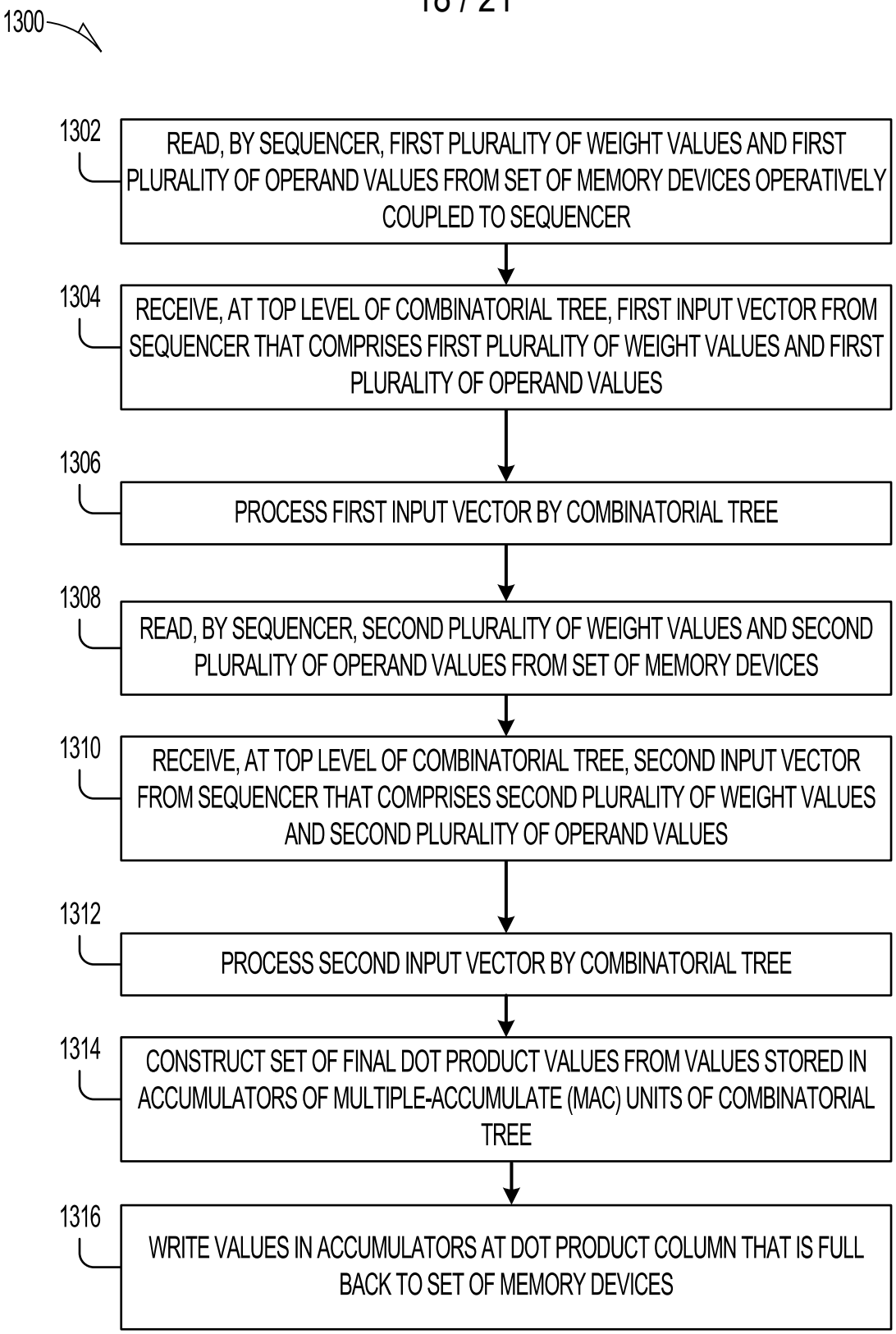

1300
1302
READ, BY SEQUENCER, FIRST PLURALITY OF WEIGHT VALUES AND FIRST PLURALITY OF OPERAND VALUES FROM SET OF MEMORY DEVICES OPERATIVELY COUPLED TO SEQUENCER
1304
RECEIVE, AT TOP LEVEL OF COMBINATORIAL TREE, FIRST INPUT VECTOR FROM SEQUENCER THAT COMPRISES FIRST PLURALITY OF WEIGHT VALUES AND FIRST PLURALITY OF OPERAND VALUES
1306
PROCESS FIRST INPUT VECTOR BY COMBINATORIAL TREE
1308
READ, BY SEQUENCER, SECOND PLURALITY OF WEIGHT VALUES AND SECOND PLURALITY OF OPERAND VALUES FROM SET OF MEMORY DEVICES
1310
RECEIVE, AT TOP LEVEL OF COMBINATORIAL TREE, SECOND INPUT VECTOR FROM SEQUENCER THAT COMPRISES SECOND PLURALITY OF WEIGHT VALUES AND SECOND PLURALITY OF OPERAND VALUES
1312
PROCESS SECOND INPUT VECTOR BY COMBINATORIAL TREE
1314
CONSTRUCT SET OF FINAL DOT PRODUCT VALUES FROM VALUES STORED IN ACCUMULATORS OF MULTIPLE-ACCUMULATE (MAC) UNITS OF COMBINATORIAL TREE
1316
WRITE VALUES IN ACCUMULATORS AT DOT PRODUCT COLUMN THAT IS FULL BACK TO SET OF MEMORY DEVICES

FIG. 13

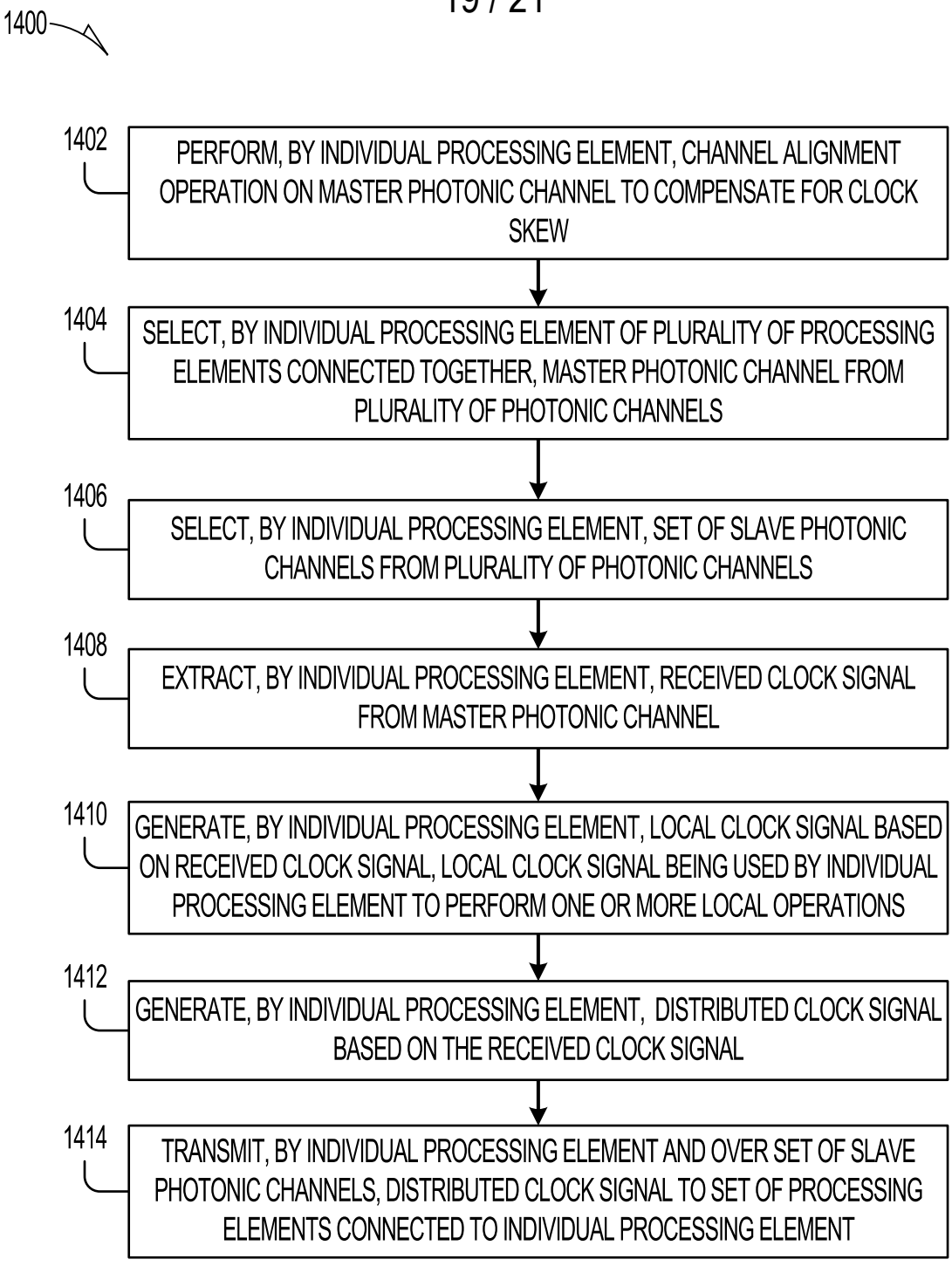

1400
1402
PERFORM, BY INDIVIDUAL PROCESSING ELEMENT, CHANNEL ALIGNMENT OPERATION ON MASTER PHOTONIC CHANNEL TO COMPENSATE FOR CLOCK SKEW
1404
SELECT, BY INDIVIDUAL PROCESSING ELEMENT OF PLURALITY OF PROCESSING ELEMENTS CONNECTED TOGETHER, MASTER PHOTONIC CHANNEL FROM PLURALITY OF PHOTONIC CHANNELS
1406
SELECT, BY INDIVIDUAL PROCESSING ELEMENT, SET OF SLAVE PHOTONIC CHANNELS FROM PLURALITY OF PHOTONIC CHANNELS
1408
EXTRACT, BY INDIVIDUAL PROCESSING ELEMENT, RECEIVED CLOCK SIGNAL FROM MASTER PHOTONIC CHANNEL
1410
GENERATE, BY INDIVIDUAL PROCESSING ELEMENT, LOCAL CLOCK SIGNAL BASED ON RECEIVED CLOCK SIGNAL, LOCAL CLOCK SIGNAL BEING USED BY INDIVIDUAL PROCESSING ELEMENT TO PERFORM ONE OR MORE LOCAL OPERATIONS
1412
GENERATE, BY INDIVIDUAL PROCESSING ELEMENT, DISTRIBUTED CLOCK SIGNAL BASED ON THE RECEIVED CLOCK SIGNAL
1414
TRANSMIT, BY INDIVIDUAL PROCESSING ELEMENT AND OVER SET OF SLAVE PHOTONIC CHANNELS, DISTRIBUTED CLOCK SIGNAL TO SET OF PROCESSING ELEMENTS CONNECTED TO INDIVIDUAL PROCESSING ELEMENT

FIG. 14

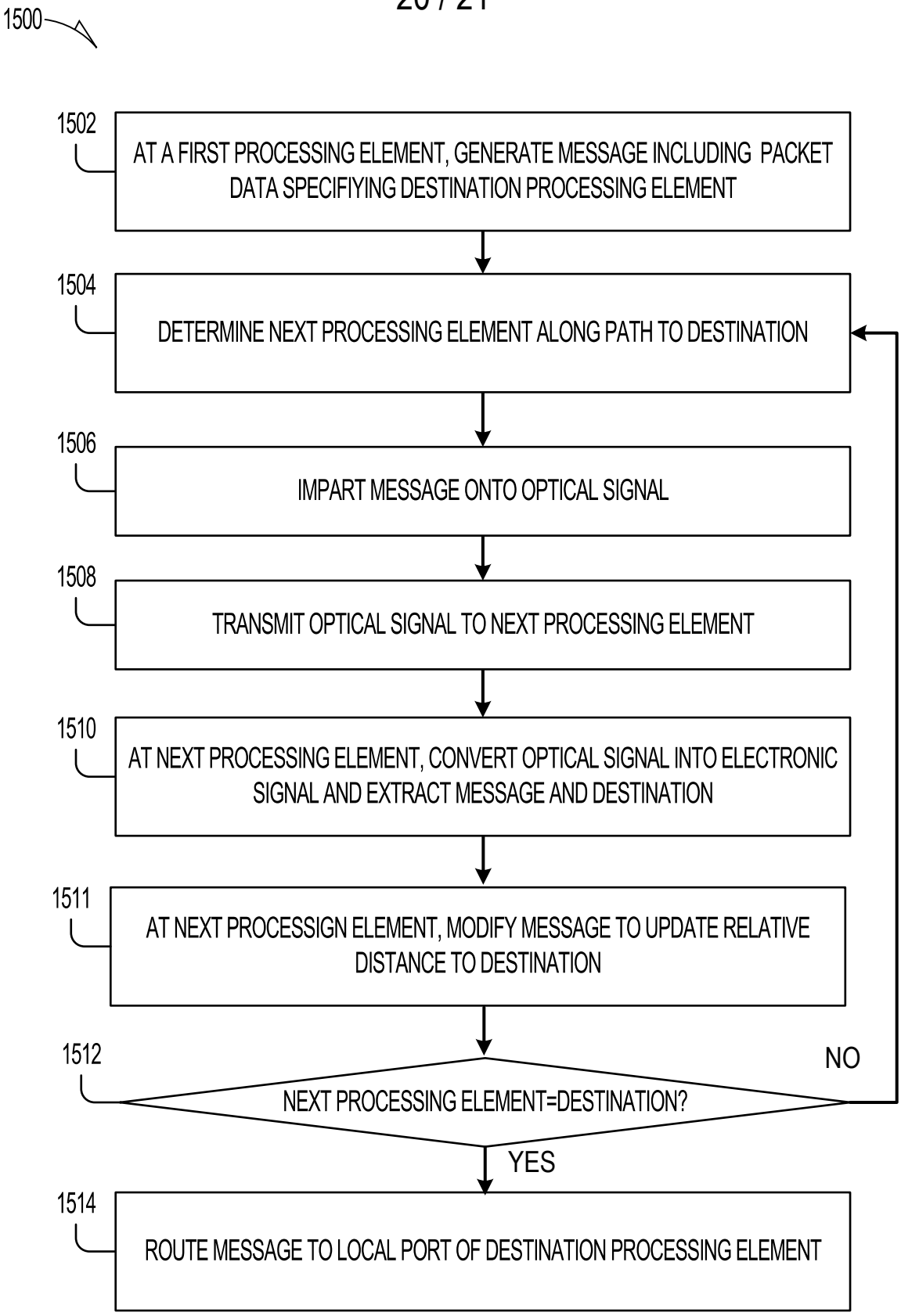

1500
1502
AT A FIRST PROCESSING ELEMENT, GENERATE MESSAGE INCLUDING PACKET DATA SPECIFIYING DESTINATION PROCESSING ELEMENT
1504
DETERMINE NEXT PROCESSING ELEMENT ALONG PATH TO DESTINATION
1506
IMPART MESSAGE ONTO OPTICAL SIGNAL
1508
TRANSMIT OPTICAL SIGNAL TO NEXT PROCESSING ELEMENT
1510
AT NEXT PROCESSING ELEMENT, CONVERT OPTICAL SIGNAL INTO ELECTRONIC SIGNAL AND EXTRACT MESSAGE AND DESTINATION
1511
AT NEXT PROCESSIGN ELEMENT, MODIFY MESSAGE TO UPDATE RELATIVE DISTANCE TO DESTINATION
1512
NEXT PROCESSING ELEMENT=DESTINATION?
NO
YES
1514
ROUTE MESSAGE TO LOCAL PORT OF DESTINATION PROCESSING ELEMENT

FIG. 15

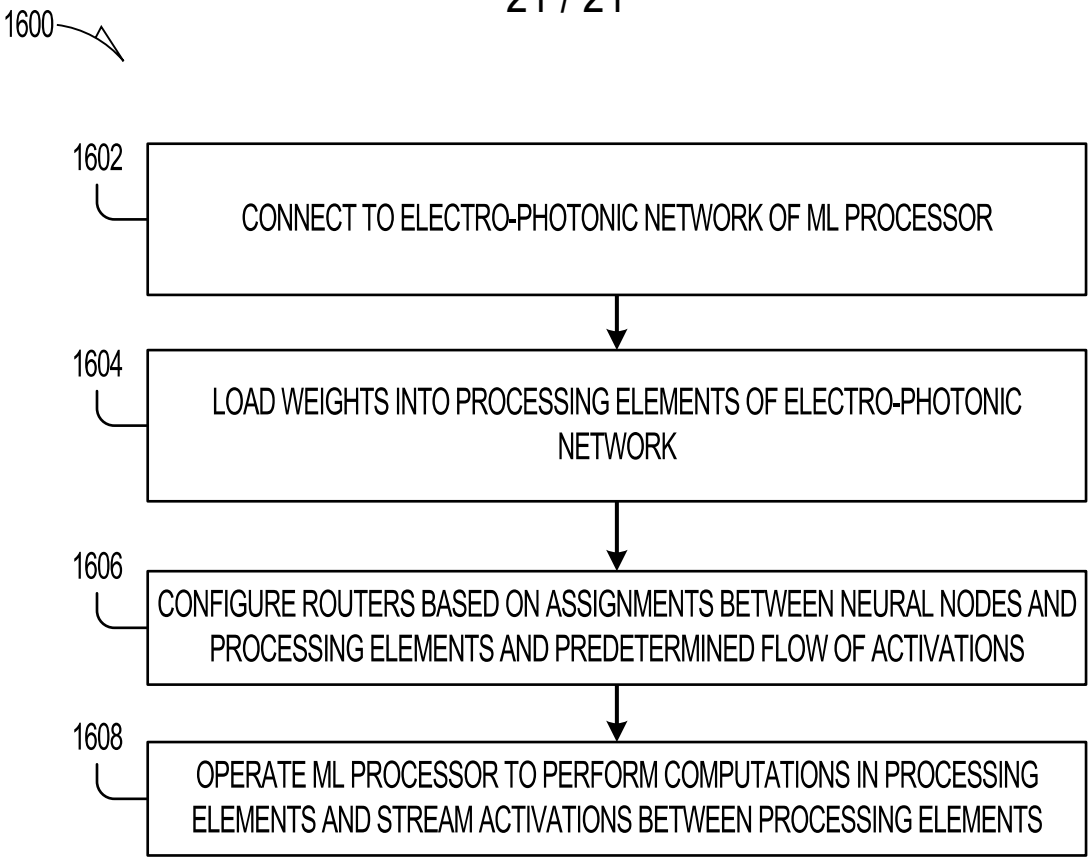

1600
1602
CONNECT TO ELECTRO-PHOTONIC NETWORK OF ML PROCESSOR
1604
LOAD WEIGHTS INTO PROCESSING ELEMENTS OF ELECTRO-PHOTONIC NETWORK
1606
CONFIGURE ROUTERS BASED ON ASSIGNMENTS BETWEEN NEURAL NODES AND PROCESSING ELEMENTS AND PREDETERMINED FLOW OF ACTIVATIONS
1608
OPERATE ML PROCESSOR TO PERFORM COMPUTATIONS IN PROCESSING ELEMENTS AND STREAM ACTIVATIONS BETWEEN PROCESSING ELEMENTS

FIG. 16