WHAT IS CLAIMED IS:

1. A neuromorphic device comprising:

a first memory cell array including first memory cells corresponding to a first address, the first memory cells configured to store first weights, and second memory cells corresponding to a second address, the second memory cells configured to store second weights; and

a first neuron circuit including a first integrator and a first activation circuit, the first integrator configured to sum first read signals from the first memory cells and output a first sum signal to the first activation circuit and to sum second read signals from the second memory cells and output second sum signals to the first activation circuit, and the first activation circuit configured to output a first activation signal based on the first sum signal and output a second activation signal based on the second sum signals of the second read signals output from the first integrator.

2. The neuromorphic device of claim 1, wherein at least one of the second weights indicates a connection strength between the first neuron circuit receiving the first read signals and the neuron circuit receiving the second read signals.

3. The neuromorphic device of claim 1 or claim 2, further comprising:

an address generator configured to generate the second address based on the first activation signal and to generate a third address based on the second activation signal.

4. The neuromorphic device of claim 3, further comprising:

a row decoder configured to decode a first internal row address of the first address and a second internal row address of the second address, respectively; and

a column decoder configured to decode a first internal column address of the first address and a second internal column address of the second address, respectively,

wherein the row decoder and the column decoder sequentially select the first memory cells and the second memory cells.

5. The neuromorphic device of claim 4, wherein the row decoder is configured to decode the first internal row address to simultaneously select first word lines respectively connected to the first memory cells and to decode the second internal row address to simultaneously select second word lines respectively connected to the second memory cells.

6. The neuromorphic device of claim 5, wherein the row decoder is configured to set an upper bit of a row address bit used to select word lines of sub memory blocks to a Don’t Care bit, and

wherein the first word lines and the second word lines are respectively placed in the sub memory blocks.

7. The neuromorphic device of any one of claims 4 to 6, wherein the first activation circuit is configured to reset at least one of the row decoder, the column decoder, and the integrator by using at least one of the first activation signal or the second activation signal.

8. The neuromorphic device of claim 7, wherein the first memory cell array further includes:

third memory cells corresponding to the third address, the third memory cells configured to store third weights; and

fourth memory cells corresponding to a fourth address, the fourth memory cells configured to store fourth weights, and

wherein, in response to at least one of the first activation signal or the second activation signal, the column decoder is configured to disable a first column selection signal selecting first bit lines connected to the first memory cells and to the second memory cells, and configured to disable a second column selection signal selecting second bit lines connected to the third memory cells and the fourth memory cells.

9. The neuromorphic device of claim 1 further comprising:

a programmable router configured to generate a bank address based on at least one of the first activation signal or the second activation signal;

a second memory cell array including third memory cells corresponding to the bank address and configured to store third weights; and

a second neuron circuit including a second integrator and a second activation circuit, the second integrator configured to sum third read signals from the third memory cells and output third sum signals, and the second activation circuit configured to output a third activation signal based on the third sum signals of the third read signals, and

wherein at least one of the third weights indicates a connection strength between the first neuron circuit and the second neuron circuit.

10. The neuromorphic device of any one of claims 1 to 9, wherein the first memory cells and the second memory cells are configured to each store one or more bits.

11. A neuromorphic device comprising:

a memory cell array including memory cells including first memory cells and second memory cells;

an input/output line, configured to access the memory cells and to write weights into the memory cells; and

a neuron circuit including an integrator and an activation circuit,

wherein the integrator is configured to sum first read signals from the first memory cells at the input/output line and output a first sum signal to the activation circuit and to sum second read signals from the second memory cells at the input/output line and output second sum signals to the activation circuit, and the activation circuit is configured to output a first activation signal based on the first sum signal and output a second activation signal based on the second sum signals of the second read signals.

12. The neuromorphic device of claim 11, further comprising:

a write driver configured to write the weights in the memory cells through the input/output line;

a row decoder configured to select a word line connected to one of the memory cells before one of the weights is written in the one of the memory cells by the write driver and to select all word lines respectively connected to the memory cells before the first read signals from the first memory cells are output or the second read signals from the second memory cells are output; and

a column decoder configured to select a column selection line through which a column selection signal selecting bit lines connected to the memory cells is transmitted.

13. The neuromorphic device of claim 12, further comprising:

an address generator configured to generate an internal row address and an internal column address based on the first activation signal or the second activation signal,

wherein the row decoder is configured to decode the internal row address to select all the word lines and to decode an external row address of the neuromorphic device to select the word line connected to the one of the memory cells,

wherein the column decoder is configured to decode the internal column address to select the column selection line and to decode an external column address to select the column selection line, and

wherein the external row address and the external column address correspond to input data of a neural network executed by the memory cell array, the row decoder, the column decoder, and the neuron circuit, and the input data are multiplied with at least a part of the weights.

14. The neuromorphic device of claim 12 or claim 13, wherein

the memory cell array further includes input/output switches configured to transmit the weights through the input/output line to the memory cells, and

wherein the integrator includes local sense amplifiers and a global sense amplifier, the local sense amplifiers configured to simultaneously drive the input/output line based on the first read signals or the second read signals respectively sensed by bit line sense amplifiers connected to the bit lines; and the global sense amplifier connected to the input/output line and simultaneously driven by the local sense amplifiers.

15. The neuromorphic device of any one of claims 12 to 14, further comprising:

a command decoder configured to decode a first command to control the row decoder, the column decoder, and the write driver and to decode a second command to control the row decoder, the column decoder, and the neuron circuit; and

a data input/output circuit configured to receive the weights under control of the command decoder decoding the first command, provide the weights to the write driver, and output read data based on the first activation signal or the second activation signal to an external device under control of the command decoder decoding the second command.

16. The neuromorphic device of any one of claims 12 to 15, wherein bit line sense amplifiers respectively connected to the bit lines are configured to restore the weights stored in the memory cells.

17. A neuromorphic device comprising:

a neuron circuit, the neuron circuit including an integrator and an activation circuit comparing a sum signal of the integrator with a threshold signal to output a pulse signal, the integrator including

a first local sense amplifier configured to output, to a first global input/output line, a first weight stored in a first memory cell and sensed by a first bit line sense amplifier;

a second local sense amplifier configured to output, to the first global input/output line, a second weight stored in a second memory cell and sensed by a second bit line sense amplifier;

a third local sense amplifier configured to output, to a second global input/output line, a third weight stored in a third memory cell and sensed by a third bit line sense amplifier;

a fourth local sense amplifier configured to output, to the second global input/output line, a fourth weight stored in a fourth memory cell and sensed by a fourth bit line sense amplifier;

a first global sense amplifier configured to sense the first and second weights summed at the first global input/output line;

a second global sense amplifier configured to sense the third and fourth weights summed at the second global input/output line; and

a sum circuit configured to sum the first to fourth weights sensed by the first and second global sense amplifiers to output the sum signal.

18. The neuromorphic device of claim 17, further comprising:

a memory cell array, the memory cell array including

first to fourth memory cells;

first to fourth bit line sense amplifiers configured to output the first to fourth weights to first to fourth local input/output lines, respectively;

a first input/output switch electrically connecting the first local input/output line to the first global input/output line;

a second input/output switch electrically connecting the second local input/output line to the first global input/output line;

a third input/output switch electrically connecting the third local input/output line to the second global input/output line; and

a fourth input/output switch electrically connecting the fourth local input/output line to the second global input/output line.

19. The neuromorphic device of claim 18, further comprising:

a row decoder configured to control a first word line connected to the first and third memory cells and a second word line connected to the second and fourth memory cells; and

a column decoder configured to control a column selection line, through which a column selection signal is transmitted, the column selection line electrically connecting a first bit line connected to the first memory cell to the first local input/output line and electrically connecting a second bit line connected to the second memory cell to the second local input/output line or a third bit line connected to the third memory cell to the third local input/output line and electrically connecting a fourth bit line connected to the fourth memory cell to the fourth local input/output line.

20. The neuromorphic device of claim 19, further comprising:

an address generator configured to generate an internal row address and an internal column address based on the pulse signal.