CLAIMS

What is claimed is:

1. An input/output (I/O) interface of a memory device, configured to:

receive a first address of first data to be read;

receive warmup information that indicates a warmup period before reading the first data; and

determine, based on the first address and the warmup information, a second address of second data to be read during the warmup period before reading the first data.

2. The I/O interface of claim 1, wherein the I/O interface comprises an address shifter and a first frequency divider coupled to the address shifter, wherein the address shifter is configured to:

determine the first address less a quantity of warmup cycles as the second address; and

send the second address to the first frequency divider.

3. The I/O interface of claim 2, wherein the address shifter is configured to:

in response to determining that the first address less the quantity of warmup cycles is a negative value, account for the negative value in determining the second address.

4. The I/O interface of claim 3, wherein the I/O interface receives a first clock signal, and wherein the first frequency divider is configured to generate a second clock signal having one-fourth a frequency of the first clock signal.

5. The I/O interface of claim 4, wherein the first data and the second data are read from a first-in-first-out (FIFO) cache of the memory device.

6. The I/O interface of claim 5, wherein the address shifter is configured to account for the negative value in determining the second address by sending a control signal to the first frequency divider, wherein the control signal is configured to instruct an output pointer of the FIFO cache to skip a first rising edge of the second clock signal during the warmup period.

7. The I/O interface of claim 4, comprising:

a second frequency divider configured to generate a third clock signal having half the frequency of the first clock signal; and

a third frequency divider configured to generate a fourth clock signal having one-eighth the frequency of the first clock signal.

8. The I/O interface of claim 1, configured to:

in response to receiving a read command to read the first data:

reset a data path of the I/O interface during a first pulse;

read data based on a fourth least significant bit of the second address during a second pulse;

read data based on a third least significant bit of the second address during a third pulse; and

read data based on a second least significant bit of the second address during a fourth pulse.

9. The I/O interface of claim 1, configured to:

in response to receiving, after a read pause, a read resume command to read the first data:

reset a data path of the I/O interface during a first pulse;

read data based on a fourth least significant bit of the second address during a second pulse;

read data based on a third least significant bit of the second address during a third pulse; and

read data based on a second least significant bit of the second address during a fourth pulse.

10. The I/O interface of claim 1, configured to:

output the second data during the warmup period; and

output the first data after the warmup period.

11. A memory device, comprising:

a memory cell array comprising memory cells; and

peripheral circuits coupled to the memory cell array, wherein the peripheral circuits comprise an input/output (I/O) interface configured to:

receive a first address of first data to be read;

receive warmup information that indicates a warmup period before reading the first data; and

determine, based on the first address and the warmup information, a second address of second data to be read during the warmup period before reading the first data.

12. The memory device of claim 11, wherein the I/O interface comprises an address shifter and a first frequency divider coupled to the address shifter, wherein the address shifter is configured to:

determine the first address less a quantity of warmup cycles as the second address; and

send the second address to the first frequency divider.

13. The memory device of claim 12, wherein the address shifter is configured to:

in response to determining that the first address less the quantity of warmup cycles is a negative value, account for the negative value in determining the second address.

14. The memory device of claim 13, wherein the peripheral circuits comprise a first-in-first-out (FIFO) cache, and wherein the first data and the second data are read from the FIFO cache.

15. The memory device of claim 14, wherein the I/O interface receives a first clock signal,

wherein the first frequency divider is configured to generate a second clock signal having one-fourth a frequency of the first clock signal,

wherein the address shifter is configured to account for the negative value in determining the second address by sending a control signal to the first frequency divider, and

wherein the control signal is configured to instruct an output pointer of the FIFO cache to skip a first rising edge of the second clock signal during the warmup period.

16. The memory device of claim 11, wherein the peripheral circuits are configured to:

read the second data during the warmup period; and

read the first data after the warmup period.

17. The memory device of claim 1, wherein the memory device comprises a NAND memory device.

18. A memory system, comprising:

a memory controller configured to send a read command to read first data, a first address of the first data and warmup information that indicates a warmup period before reading the first data; and

a memory device coupled to the memory controller, the memory device comprising:

a memory cell array comprising memory cells; and

a peripheral circuit comprising an input/output (I/O) interface configured to:

receive the read command, the first address and the warmup information; and

determine, based on the first address and the warmup information, a second address of second data to be read during the warmup period before reading the first data.

19. The memory system of claim 18, wherein determining the second address comprises:

determining the first address less a quantity of warmup cycles as the second address.

20. The memory system of claim 18, wherein the peripheral circuit is configured to:

read the second data during the warmup period; and

read the first data array after the warmup period.