SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application is based on and claims priority to Korean Patent Application No. 10-2022-0030325, filed on 10 March 2022, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] Inventive concepts relate to a semiconductor device, and more particularly, to a semiconductor device with improved device performance.

BACKGROUND

[0003] In line with the miniaturization of semiconductor devices, patterns included in the semiconductor devices have gradually been miniaturized. When manufacturing a semiconductor device, a micro-patterning process for forming micro-patterning becomes increasingly difficult. Accordingly, there may be a need for a method for overcoming difficulties in the micro-patterning process and improving the device performance of miniaturized semiconductor devices.

SUMMARY

[0004] Inventive concepts provide a semiconductor device with improved device performance.

[0005] According to an example embodiment of inventive concepts, a semiconductor device may include a substrate including an active region in a substrate; a first gate line and a second gate line in the active region, the first gate line and the second gate line being spaced apart from each other in a first direction and extending in a second direction, the second direction crossing the first direction; a first source/drain contact pattern in the active region at one side of the first gate line; a second source/drain contact pattern in the active region at one side of the second gate line; and a dummy source/drain contact pattern in the active region between the first gate line and the second gate line. A size of the dummy source/drain contact pattern may be less

than a size of the first source/drain contact pattern and a size of the second source/drain contact pattern.

[0006] According to an example embodiment of inventive concepts, a semiconductor device may include a substrate including an active region having a first region width in a first direction and a first region length in a second direction, the second direction perpendicular to the first direction, the active region including a first active contact region, a second active contact region, and a dummy contact region between the first active contact region and the second active contact region; a first gate line and a second gate line extending in the second direction in the active region, the second gate line spaced apart from the first gate line in the first direction, the first gate line and the second gate line in the active region with the first active contact region at one side of the first gate line, the second active contact region at one side of the second gate line, and the dummy contact region between the first gate line and the second gate line; a first source/drain contact pattern in the first active contact region, the first source/drain contact pattern being spaced apart from the first gate line in the first direction; and a second source/drain contact pattern in the second active contact region, the second source drain/contact pattern being spaced apart from the second gate line in the first direction.

[0007] According to another example embodiment of inventive concepts, a semiconductor device may include a substrate including an active region, the active region including a first active contact region, a second active contact region, and a plurality of dummy contact regions in the active region; a plurality of gate lines spaced apart from each other in a first direction in the active region, the plurality of gate lines extending in a second direction perpendicular to the first direction in the active region, the plurality of gate lines including a first gate line and a second gate line, the plurality of gate lines in the active region with the first active contact region disposed at one side of the first gate line and the second active contact region at one side of the second gate line, and the plurality of dummy contact regions in the active region between the plurality of gate lines; a first source/drain contact pattern in the first active contact region; a second source/drain contact pattern in the second active contact region; and a plurality of dummy source/drain contact patterns in at least one of the plurality of dummy contact regions. Sizes of the plurality of dummy source/drain contact patterns may be less than a size of the first source/drain contact pattern and a size the second source/drain contact pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of inventive concepts will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] FIGS. 1 and 2 are plan views of a semiconductor device according to an embodiment of inventive concepts;

[0010] FIG. 3 is a cross-sectional view of a semiconductor device according to an embodiment of inventive concepts;

[0011] FIG. 4 is a diagram illustrating device resistance of the semiconductor device of FIG. 3;

[0012] FIG. 5 is a cross-sectional view of a semiconductor device according to an embodiment of inventive concepts;

[0013] FIG. 6 is a cross-sectional view of a semiconductor device according to an embodiment of inventive concepts;

[0014] FIG. 7 is a cross-sectional view of a semiconductor device according to an embodiment of inventive concepts;

[0015] FIGS. 8 and 9 are plan views of a semiconductor device according to an embodiment of inventive concepts;

[0016] FIG. 10 is a plan view of a semiconductor device according to an embodiment of inventive concepts;

[0017] FIG. 11 is a diagram illustrating device resistance of the semiconductor device of FIG. 10;

[0018] FIG. 12 is a plan view of a semiconductor device according to an embodiment of inventive concepts;

[0019] FIG. 13 is a plan view of a semiconductor device according to an embodiment of inventive concepts;

[0020] FIG. 14 is a cross-sectional view of a semiconductor device according to an embodiment of inventive concepts;

[0021] FIG. 15 is a cross-sectional view illustrating an active contact structure used in a semiconductor device according to inventive concepts;

[0022] FIG. 16 is a cross-sectional view illustrating an embodiment of a dummy contact structure used in a semiconductor device according to an embodiment of inventive concepts;

[0023] FIG. 17 is a cross-sectional view illustrating an embodiment of a dummy contact structure used in a semiconductor device according to an embodiment of inventive concepts; and

[0024] FIG. 18 is a schematic diagram illustrating an electronic system including a semiconductor device according to an embodiment of inventive concepts.

DETAILED DESCRIPTION

[0025] Hereinafter, example embodiments of inventive concepts are described in detail with reference to the accompanying drawings. The following embodiments of inventive concepts may be implemented by only one or may also be implemented by combining one or more thereof. Accordingly, features and aspects of inventive concepts are not to be construed as being limited to one embodiment.

[0026] FIGS. 1 and 2 are plan views of a semiconductor device according to an embodiment of inventive concepts.

[0027] In an embodiment, a semiconductor device EX1 may include an active region (or active area) 12 in a substrate (sb in FIG. 3), a first gate line 14a, a second gate line 14b, a first source/drain contact pattern 24, a second source/drain contact pattern 26, and a dummy source drain contact pattern 28. A source/drain may refer to a source or a drain.

[0028] The semiconductor device EX1 may be an integrated circuit device. The semiconductor device EX1 may be a metal oxide silicon (MOS) transistor. The semiconductor device EX1 may be a PMOS transistor or an NMOS transistor. The semiconductor device EX1 may be a field effect transistor (FET).

[0029] The active region 12 may be a region in which an active device is formed. The active region 12 may have a first region width ta in a first direction (an X direction) and a first region length tb in a second direction (a Y direction) perpendicular to the first direction (the X direction). Portions other than the active region 12 may be non-active regions (or non-active areas 8 and 10 of FIG. 3). The non-active regions (8 and 10 in FIG. 3) may be referred to as device isolation regions or field regions.

[0030] The first gate line 14a extends in the second direction (the Y direction) in the active region 12. A first gate contact pattern 30 may be disposed on the first gate line 14a. The second gate line 14b is disposed in the active region 12 and spaced apart from the first gate line 14a in the first direction (the X direction).

[0031] A second gate contact pattern 32 may be disposed on the second gate line 14b. The second gate line 14b extends in the second direction (the Y direction). The first gate line 14a and the second gate line 14b may also be disposed outside the active region 12, that is, in the non-active region.

[0032] According to the arrangement of the first gate line 14a and the second gate line 14b, the active region 12 may be classified as a first active contact region 18, a second active contact region 20, and a dummy contact region 22. The first active contact region 18 may be disposed in the active region 12 at one side of the first gate line 14a. The second active contact region 20 may be disposed in the active region 12 at one side of the second gate line 14b. The dummy contact region 22 may be disposed in the active region 12 between the first gate line 14a and the second gate line 14b.

[0033] The first active contact region 18 may be a first source/drain region. The second active contact region 20 may be a second source/drain region. The dummy contact region 22 may be a dummy source/drain region.

[0034] The first source/drain contact pattern 24 is disposed in the active region 12 at one side of the first gate line 14a. The first source/drain contact pattern 24 may be disposed in the first active contact region 18. The first source/drain contact pattern 24 is apart from the first gate line 14a in the first direction (the X direction). The first source/drain contact pattern 24 is apart from one edge 12c of the active region 12 in the first direction (the X direction).

[0035] The second source/drain contact pattern 26 is disposed in the active region 12 at one side of the second gate line 14b. The second source/drain contact pattern 26 may be disposed in the second active contact region 20. The second source/drain contact pattern 26 is apart from the second gate line 14b in the first direction (the X direction). The second source/drain contact pattern 26 is apart from one edge 12d of the active region 12 in the first direction (-X direction).

[0036] The dummy source/drain contact pattern 28 is disposed in the active region 12 between the first gate line 14a and the second gate line 14b. The semiconductor device EX1 may have a symmetrical structure in the first direction (the X direction) with respect to the dummy source/drain contact pattern 28. The dummy source/drain contact pattern 28 may be disposed in the dummy contact region 22.

[0037] The dummy source/drain contact pattern 28 is apart from one edge 12a of the active region 12 by a first spacing distance g in the second direction (-Y direction). The dummy source/drain contact pattern 28 is apart from the other edge 12b of the active region 12 by a second spacing distance h in the second direction (the Y direction).

[0038] The dummy source/drain contact pattern 28 may have a smaller size than the first source/drain contact pattern 24 and the second source/drain contact pattern 26. The size may refer to the width, length, or area of a pattern. Here, the sizes of the first source/drain contact pattern 24, the second source/drain contact pattern 26, and the dummy source/drain contact pattern 28 are described in detail.

[0039] The dummy source/drain contact pattern 28 may have a first pattern width a in the first direction (the X direction) and a first pattern length b in the second direction (the Y direction). The first source/drain contact pattern 24 may have a second pattern width c in the first direction (the X direction) and a second pattern length d in the second direction (the Y direction). The second source/drain contact pattern 26 may have a third pattern width e in the first direction (the X direction) and a third pattern length f in the second direction (the Y direction). The second pattern length d of the first source/drain contact pattern 24 and the third pattern length f of the second source/drain contact pattern 26 may be equal to the first region length tb of the active region 12.

[0040] In some embodiments, the first pattern width a, the first pattern length b, the second pattern width c, the second pattern length d, the third pattern width e, and the third pattern length f may have a size of a few nanometers (nm) to tens of nanometers (nm).

[0041] The first pattern width a of the dummy source/drain contact pattern 28 may be equal to the second pattern width c of the first source/drain contact pattern 24 in the first direction (the X direction) and the third pattern width e of the second source/drain contact pattern 26 in the first direction (the X direction).

[0042] The first pattern length b of the dummy source/drain contact pattern 28 may be less than the second pattern length d of the first source/drain contact pattern 24 in the second direction (the Y direction) and the third pattern length f of the second source/drain contact pattern 26 in the second direction (the Y direction). The first pattern length b of the dummy source/drain contact pattern 28 may be less than the first region length tb of the active region 12.

[0043] As described above, in the semiconductor device EX1, the first pattern length b of the dummy source/drain contact pattern 28 is configured to be less than the second pattern length d of the first source/drain contact pattern 24 and the third pattern length f of the second source/drain contact pattern 26.

[0044] Accordingly, in the semiconductor device EX1, damage to the active region 12 below the dummy source/drain contact pattern 28, for example, the dummy source/drain region, may be limited and/or suppressed. As a result, in the semiconductor device EX1, device resistance between the first source/drain contact pattern 24 and the second source/drain contact pattern 26 may be reduced during a device operation, thereby improving device performance.

[0045] FIG. 3 is a cross-sectional view of the semiconductor device EX1 according to an embodiment of inventive concepts, and FIG. 4 is a diagram illustrating device resistance of the semiconductor device EX1 of FIG. 3.

[0046] In an embodiment, the semiconductor device EX1 may be a cross-sectional view taken along line X1-X1' of FIG. 1. In FIGS. 3 and 4, the same reference numerals as those of FIGS. 1 and 2 denote the same members. In FIGS. 3 and 4, the same description as that of FIGS. 1 and 2 is briefly given or omitted.

[0047] The semiconductor device EX1 may be a planar transistor and may be formed by a gate first process. Accordingly, in the semiconductor device EX1, a first gate insulating layer 13 and a second gate insulating layer 15 may be formed below the first gate line 14a and the second gate line 14b, respectively.

[0048] In more detail, the semiconductor device EX1 may include the active region 12 and the non-active regions 8 and 10 formed in the substrate sb. The non-active regions 8 and 10 may include a first non-active region 8 and a second non-active region 10. A substrate sb may include one or more semiconductor materials selected from the group consisting of Si, Ge, SiGe, GaP, GaAs, SiC, SiGeC, InAs, and InP. The active region 12 may include the same material as that of the substrate sb. The active region 12 may be defined by forming the first and second non-active regions 8 and 10 on the substrate sb. The first and second non-active regions 8 and 10 may be insulating regions. The first and second non-active regions 8 and 10 may be trench isolation regions.

[0049] The first gate line 14a and the second gate line 14b may be formed in the active region 12 of the substrate sb. The first gate line 14a and the second gate line 14b may be referred to as planar gate lines formed on the substrate Sb. The first gate line 14a and the second gate line 14b may include a metal, such as W or TiN. The second gate line 14b is apart from the first gate line 14a in the first direction (the X direction). The first gate insulating layer 13 may be formed below the first gate line 14a. The second gate insulating layer 15 may be formed below the second gate line 14b.

[0050] The first active contact region 18 may be formed in the active region 12 of the substrate sb at one side of the first gate line 14a. The first active contact region 18 may be a first source/drain region. The first source/drain region may be an impurity-doped region in which the substrate sb is doped with impurities.

[0051] The second active contact region 20 may be formed in the active region 12 of the substrate sb at one side of the second gate line 14b. The second active contact region 20 may be a second source/drain region. The second source/drain region may be an impurity-doped region in which the substrate sb is doped with impurities.

[0052] The dummy contact region 22 may be formed in the active region 12 of the substrate sb between the first gate line 14a and the second gate line 14b. The dummy contact region 22

may be a dummy source/drain region. The dummy source/drain region may be an impurity-doped region in which the substrate sb is doped with impurities.

[0053] The first source/drain contact pattern 24 may be formed in the first active contact region 18. In other words, the first source/drain contact pattern 24 may be formed in the first active contact region 18 to be apart from the first gate line 14a.

[0054] The second source/drain contact pattern 26 may be formed on the second active contact region 20. In other words, the second source/drain contact pattern 26 may be formed in the second active contact region 20 to be apart from the second gate line 14b. The dummy source/drain contact pattern 28 may be formed in the dummy contact region 22.

[0055] When the dummy source/drain contact pattern 28 is formed to manufacture the semiconductor device EX1, the dummy contact region 22 may be damaged to form a dummy source/drain loss region 34. The dummy source/drain loss region 34 may have a depth de1 from a surface 6 of the substrate sb, as shown in FIG. 4.

[0056] As described above, the dummy source/drain contact pattern 28 of the semiconductor device EX1 of inventive concepts may have a smaller size than the first source/drain contact pattern 24 and the second source/drain contact pattern 26. Accordingly, as shown in FIG. 4, in the semiconductor device EX1 of inventive concepts, the size of the dummy source/drain loss region 34 may be reduced to reduce resistance Rsd of the dummy contact region 22. The resistance Rsd of the dummy contact region 22 may be connected to channel resistance Rch.

[0057] As a result, in the semiconductor device EX1 according to embodiments of inventive concepts, device resistance between the first active contact region 18 (or the first source/drain region) and the second active contact region 20 (or the second source/drain region) may be reduced during a device operation.

[0058] FIG. 5 is a cross-sectional view of a semiconductor device EX2 according to an embodiment of inventive concepts.

[0059] In an embodiment, the semiconductor device EX2 may be the same as the semiconductor device EX1 of FIG. 3, except that structures of a first gate line 14a-1 and a second gate line 14b-1 are different from those in the semiconductor device EX1 of FIG. 3. The semiconductor device EX2 of FIG. 5 may be a cross-sectional view taken along line X-X' of FIG. 1. In FIG. 5, the same reference numerals as those of FIG. 3 denote the same members. In FIG. 5, the descriptions given above with reference to FIG. 3 are briefly given or omitted.

[0060] The semiconductor device EX2 of FIG. 5 may be a planar transistor and may be formed by a gate last process. The semiconductor device EX2 may have a symmetric structure in the first direction (the X direction) with respect to the dummy source/drain contact pattern 28. The

first gate line 14a-1 and the second gate line 14b-1 of the semiconductor device EX2 may be manufactured during the same process. The first gate line 14a-1 and the second gate line 14b-1 may be referred to as trench-type gate lines formed in a gate trench in the substrate Sb.

[0061] In an embodiment, in the semiconductor device EX2, a first gate insulating layer 13-1 may be formed in a first gate trench TE1 in the substrate Sb. The first gate line 14a-1 may be formed on the first gate insulating layer 13-1 in the first gate trench TE1. The first gate line 14a-1 may include a first metal layer mg1 and a second metal layer mg2. Although the first gate line 14a-1 includes two metal layers, the first gate line 14a-1 may also include three or more metal layers.

[0062] In the semiconductor device EX2, a second gate insulating layer 15-1 may be formed in the second gate trench TE2 in the substrate Sb. The second gate line 14b-1 may be formed on the second gate insulating layer 15-1 in the second gate trench TE2. The second gate line 14b-1 may include a third metal layer mg3 and a fourth metal layer mg4.

[0063] Although the second gate line 14b-1 includes two metal layers, the second gate line 14b-1 may also include three or more metal layers. The first metal layer mg1 and the third metal layer mg3 may include at least one of TiN, TaN, TiC, and TaC. The second metal layer mg2 and the fourth metal layer mg4 may include W or Al.

[0064] FIG. 6 is a cross-sectional view of a semiconductor device according to an embodiment of inventive concepts.

[0065] In an embodiment, a semiconductor device EX3 may be the same as the semiconductor device EX1 of FIG. 3, except that the semiconductor device EX3 includes a fin-type active region 12-1. The semiconductor device EX3 may be a cross-sectional view taken along line X-X' of FIG. 1. In FIG. 6, the same reference numerals as those in FIG. 3 denote the same members. In FIG. 6, the descriptions given above with reference to FIG. 3 are briefly given or omitted.

[0066] The semiconductor device EX3 may be a fin-type field effect transistor (FinFET) and may be formed by a gate first process. The semiconductor device EX3 may have a symmetrical structure in the first direction (the X direction) with respect to the dummy source/drain contact pattern 28. The semiconductor device EX3 may include the fin-type active region 12-1 protruding from surfaces 8a and 10a of the first and second non-active regions 8 and 10.

[0067] The surface 8a of the first non-active region 8 may be lower than the surface 6 of the substrate sb. The surface 10a of the second non-active region 10 may be lower than the surface 6 of the substrate sb. The first active contact region 18 may protrude relative to the surface 8a

of the first non-active region 8. The second active contact region 20 may protrude relative to the surface 10a of the second non-active region 10.

[0068] FIG. 7 is a cross-sectional view of a semiconductor device EX4 according to an embodiment of inventive concepts.

[0069] In an embodiment, the semiconductor device EX4 may be the same as that of the semiconductor device EX2 of FIG. 5, except that the semiconductor device EX4 includes the fin-type active region 12-1. The semiconductor device EX4 may be a cross-sectional view taken along line X-X' of FIG. 1. In FIG. 7, the same reference numerals as in those of FIG. 5 denote the same members. In FIG. 7, the descriptions given above with reference to FIG. 5 are briefly given or omitted.

[0070] The semiconductor device EX4 may be a FinFET and may be formed by a gate last process. The semiconductor device EX4 may have a symmetrical structure in the first direction (the X direction) with respect to the dummy source/drain contact pattern 28. The semiconductor device EX4 may include a first gate line 14a-1 and a second gate line 14b-1.

[0071] The semiconductor device EX4 may include the fin-type active region 12-1 protruding from the surfaces 8a and 10a of the first and second non-active regions 8 and 10. The first active contact region 18 may protrude relative to the surface 8a of the first non-active region 8. The second active contact region 20 may protrude relative to the surface 10a of the second non-active region 10.

[0072] FIGS. 8 and 9 are plan views of a semiconductor device EX5 according to an embodiment of inventive concepts.

[0073] In an embodiment, the semiconductor device EX5 may be the same as the semiconductor device EX1 of FIGS. 1 and 2, except for a different arrangement and shape of a dummy source/drain contact pattern 28-1. In FIGS. 8 and 9, the same reference numerals as those of FIGS. 1 and 2 denote the same members. In FIGS. 8 and 9, the descriptions given above with reference to FIGS. 1 and 2 are briefly given or omitted.

[0074] The semiconductor device EX5 may include the active region 12, the first gate line 14a, the second gate line 14b, the first source/drain contact pattern 24, the second source/drain contact pattern 26, and the dummy source/drain contact pattern 28-1. The semiconductor device EX5 may have a symmetric structure in the first direction (the X direction) with respect to the dummy source/drain contact pattern 28-1.

[0075] The active region 12 may have the first region width ta in the first direction (the X direction) and the first region length tb in the second direction (the Y direction) perpendicular to the first direction (the X direction). According to the arrangement of the first gate line 14a

and the second gate line 14b, the active region 12 may be classified as a first active contact region 18, a second active contact region 20, and a dummy contact region 22.

[0076] The dummy source/drain contact pattern 28-1 may be in contact with one edge 12a and the other edge 12b of the active region 12 in the second direction (the Y direction), rather than being apart therefrom. The dummy source/drain contact pattern 28-1 may have a smaller size than that of the first source/drain contact pattern 24 and the second source/drain contact pattern 26.

[0077] The dummy source/drain contact pattern 28-1 may have a first pattern width a-1 in the first direction (the X direction) and a first pattern length b-1 in the second direction (the Y direction). The first pattern width a-1 of the dummy source/drain contact pattern 28-1 in the first direction (the X direction) may be less than the second pattern width c of the first source/drain contact pattern 24 in the first direction (the X direction) and the third pattern width e of the second source/drain contact pattern 26 in the first direction (the X direction).

[0078] The first pattern length b-1 of the dummy source/drain contact pattern 28-1 in the second direction (the Y direction) may be equal to the second pattern length d of the first source/drain contact pattern 24 in the second direction (the Y direction) and the third pattern length f of the second source/drain contact pattern 26 in the third direction (the Y direction). The second pattern length d of the first source/drain contact pattern 24 and the third pattern length f of the second source/drain contact pattern 26 may be equal to the first region length tb of the active region 12.

[0079] In some embodiments, the first pattern width a-1, the first pattern length b-1, the second pattern width c, the second pattern length d, the third pattern width e, and the third pattern length f may have a size of a few nanometers (nm) to tens of nanometers (nm).

[0080] As described above, in the semiconductor device EX5, the first pattern width a-1 of the dummy source/drain contact pattern 28-1 is configured to be less than the second pattern width c of the first source/drain contact pattern 24 and the third pattern width e of the second source/drain contact pattern 26.

[0081] Accordingly, in the semiconductor device EX5, damage to the active region 12 below the dummy source/drain contact pattern 28-1, for example, the dummy source/drain region, may be suppressed. As a result, in the semiconductor device EX5, device resistance between the first source/drain contact pattern 24 and the second source/drain contact pattern 26 may be reduced during a device operation, thereby improving device performance.

[0082] FIG. 10 is a plan view of a semiconductor device EX6 according to an embodiment of inventive concepts, and FIG. 11 is a diagram illustrating device resistance of the semiconductor device EX6 of FIG. 10.

[0083] In an embodiment, the semiconductor device EX6 may be the same as the semiconductor device EX1 of FIGS. 1 and 2, except that a dummy source/drain contact pattern is not disposed in the dummy contact region 22. In FIGS. 10 and 11, the same reference numerals as those of FIGS. 1 and 2 denote the same members. In FIGS. 10 and 11, the descriptions given above with reference to FIGS. 1 and 2 are briefly given or omitted.

[0084] The semiconductor device EX6 may include the active region 12, the first gate line 14a, the second gate line 14b, the first source/drain contact pattern 24, and the second source/drain contact pattern 26. According to the arrangement of the first gate line 14a and the second gate line 14b, the active region 12 may be classified as a first active contact region 18, a second active contact region 20, and a dummy contact region 22. A dummy source/drain contact pattern is not disposed in the dummy contact region 22.

[0085] As described above, in the semiconductor device EX6, a dummy source/drain contact pattern is not disposed in the dummy contact region 22. Accordingly, in the semiconductor device EX6, there is no damage to the dummy contact region 22, that is, the dummy source/drain region, so that resistance Rsd-1 of the dummy contact region 22 may be reduced. The resistance Rsd-1 of the dummy contact region 22 may be connected to a channel resistance Rch.

[0086] As a result, in the semiconductor device EX6 of inventive concepts, device resistance between the first active contact region 18 (or the first source/drain region) and the second active contact region 20 (or the second source/drain region) may be reduced during a device operation.

[0087] FIG. 12 is a plan view of a semiconductor device EX7 according to an embodiment of inventive concepts.

[0088] In an embodiment, the semiconductor device EX7 may be the same as the semiconductor device EX1 of FIGS. 1 and 2, except that the semiconductor device EX7 includes a plurality of gate lines 14c to14f and an arrangement form of a dummy source/drain contact pattern 28-2 is different from that in the semiconductor device EX1 of FIGS. 1 and 2. In FIG. 12, the same reference numerals as those of FIGS. 1 and 2 denote the same members. In FIG. 12, the descriptions given above with reference to FIGS. 1 and 2 are briefly given or omitted.

[0089] The semiconductor device EX7 may include an active region 12 disposed on a substrate (sb of FIG. 3), a plurality of gate lines 14c to 14f, a first source/drain contact pattern 24, a second source/drain contact pattern 26, and a dummy source/drain contact pattern 28-2.

[0090] The gate lines 14c to 14f are apart from each other in the first direction (the X direction) in the active region 12 and extend in the second direction (the Y direction) perpendicular to the first direction (the X direction). The gate lines 14c to 14f may include a first gate line 14c on the left side in the first direction (the X direction) and a second gate line 14f on the right side.

[0091] The active region 12 may be classified as a first active contact region 18, a second active contact region 20, and a dummy contact region 22-1 according to the arrangement of the gate lines 14c to 14f. The first active contact region 18 may be disposed in the active region 12 at one side of the first gate line 14c. The second active contact region 20 may be disposed in the active region 12 at one side of the second gate line 14f.

[0092] The dummy contact region 22-1 may be disposed in the active region 12 between the gate lines 14c to 14f. The dummy contact region 22-1 may include first to third dummy contact regions 22a to 22c. A dummy source/drain contact pattern 28-2 may be disposed in the dummy contact region 22-1.

[0093] The dummy source/drain contact pattern 28-2 may include first to third dummy source/drain contact patterns 28a to 28c. The first to third dummy source/drain contact patterns 28a to 28c may be disposed in the first to third dummy contact regions 22a to 22c, respectively.

[0094] The first dummy source/drain contact pattern 28a is apart from one edge 12a of the active region 12 by a first spacing distance g1 in the second direction (-Y direction). The first dummy source/drain contact pattern 28a may be the same as the dummy source/drain contact pattern 28 of FIGS. 1 and 2. The first dummy source/drain contact pattern 28a is apart from the other edge 12b of the active region 12 by a second spacing distance h1 in the second direction (the Y direction).

[0095] The second dummy source/drain contact pattern 28b is in contact with one edge 12a of the active region 12 in the second direction (-Y direction). The second dummy source/drain contact pattern 28b may have the same size as the first dummy source/drain contact pattern 28a. The second dummy source/drain contact pattern 28b is apart from the other edge 12b of the active region 12 by a third spacing distance h2 in the second direction (the Y direction).

[0096] The third dummy source/drain contact pattern 28c is in contact with the other edge 12b of the active region 12 in the second direction (the Y direction). The third dummy source/drain contact pattern 28c is apart from one edge 12a of the active region 12 by a fourth spacing

distance g2 in the second direction (-Y direction). The third dummy source/drain contact pattern 28c may have the same size as the first dummy source/drain contact pattern 28a.

[0097] As described above, the dummy source/drain contact pattern 28-2 of the semiconductor device EX7 may have a size less than the first source/drain contact pattern 24 and the second source/drain contact pattern 26. Accordingly, in the semiconductor device EX7 of inventive concepts, resistance of the dummy contact region 22-1 may be reduced by reducing the size of a dummy source/drain loss region below the dummy source/drain contact pattern 28-2.

[0098] As a result, in the semiconductor device EX7 of inventive concepts, device resistance between the first active contact region 18 (or the first source/drain region) and the second active contact region 20 (or the second source/drain region) may be reduced during a device operation.

[0099] FIG. 13 is a plan view of a semiconductor device EX8 according to an embodiment of inventive concepts.

[0100] In detail, the semiconductor device EX8 may be the same as the semiconductor device EX7 of FIG. 12, except that an arrangement form or arranged shape of a dummy source/drain contact pattern 28-3 is different. In FIG. 13, the same reference numerals as those of FIG. 12 denote the same members. In FIG. 13, the descriptions given above with reference to FIG. 12 are briefly given or omitted.

[0101] The semiconductor device EX8 may include the active region 12 disposed on the substrate (sb of FIG. 3), a plurality of gate lines 14g to 14k, a first source/drain contact pattern 24, a second source/drain contact pattern 26, and a dummy source/drain contact pattern 28-3.

[0102] The gate lines 14g to 14k are apart from each other in the first direction (the X direction) in the active region 12 and extend in the second direction (the Y direction) perpendicular to the first direction (the X direction). The gate lines 14g to 14k may include a first gate line 14g on the left side in the first direction (the X direction) and a second gate line 14k on the right side.

[0103] The active region 12 may be classified as a first active contact region 18, a second active contact region 20, and a dummy contact region 22-2 according to the arrangement of the gate lines 14g to 14k. The first active contact region 18 may be disposed in the active region 12 at one side of the first gate line 14c. The second active contact region 20 may be disposed in the active region 12 at one side of the second gate line 14g.

[0104] The dummy contact region 22-2 may be disposed in the active region 12 between the gate lines 14g to 14k. The dummy contact area 22-2 may include first to fourth dummy contact areas 22d to 22f. The dummy source/drain contact pattern 28-3 may be disposed in the dummy contact region 22-2.

[0105] The dummy source/drain contact pattern 28-3 may include first to third dummy source/drain contact patterns 28e to 28g. The first to third dummy source/drain contact patterns 28e to 28g may be disposed in the first to third dummy contact regions 22d to 22f, respectively. A dummy source/drain contact pattern may not be formed in the fourth dummy contact region 22g.

[0106] The first dummy source/drain contact pattern 28e is in contact with one edge 12a and the other edge 12b of the active region 12 in the second direction (the Y direction). The first dummy source/drain contact pattern 28e may be the same as the first dummy source/drain contact pattern 28-1 of FIGS. 8 and 9. The first dummy source/drain contact pattern 28f is in contact with one edge 12a and the other edge 12b of the active region 12 in the second direction (the Y direction).

[0107] The second dummy source/drain contact pattern 28f may include a plurality of sub-dummy source/drain contact patterns 28f1 and 28f2. In FIG. 13, two sub-dummy source/drain contact patterns 28f1 and 28f2 are included, but a greater number of sub-dummy source/drain contact patterns may be included.

[0108] The third dummy source/drain contact pattern 28g is apart from one edge 12a of the active region 12 by a fifth spacing distance h3 in the second direction (-Y direction). The third dummy source/drain contact pattern 28g is apart from the other edge 12b of the active region 12 by a sixth spacing distance g3 in the second direction (the Y direction). The third dummy source/drain contact pattern 28g may have the same pattern width as that of the first dummy source/drain contact pattern 28e in the first direction (the X direction). The third dummy source/drain contact pattern 28g may have a length less than that of the first dummy source/drain contact pattern 28e in the second direction (the Y direction).

[0109] As described above, the dummy source/drain contact pattern 28-3 of the semiconductor device EX8 may have a size less than that of the first source/drain contact pattern 24 and the second source/drain contact pattern 26. Accordingly, in the semiconductor device EX8 of an embodiment of inventive concepts, resistance of the dummy contact region 22-2 may be reduced by reducing the size of a dummy source/drain loss region below the dummy source/drain contact pattern 28-3.

[0110] As a result, in the semiconductor device EX8 of an embodiment inventive concepts, device resistance between the first active contact region 18 (or the first source/drain region) and the second active contact region 20 (or the second source/drain region) may be reduced during a device operation.

[0111] FIG. 14 is a cross-sectional view of a semiconductor device EX9 according to an embodiment of inventive concepts.

[0112] In an embodiment, the semiconductor device EX9 may be the same as the semiconductor device EX1 of FIGS. 1 to 3, except that a structure of a dummy source/drain contact pattern 28-4 and a dummy contact region 22-3 are different. In FIG. 14, the same reference numerals as those of FIGS. 1 to 3 denote the same members. In FIG. 14, the descriptions given above with reference to FIGS. 1 to 3 are briefly given or omitted.

[0113] The semiconductor device EX9 may include the active region 12, the first and second gate lines 14a and 14b, the first source/drain contact pattern 24, the second source/drain contact pattern 26, the dummy contact region 22-3, and the dummy source/drain contact pattern 28-4.

[0114] The first gate line 14a is formed on the active region 12 of the substrate sb in the Y direction. The first gate contact pattern 30 may be formed on the first gate line 14a. The second gate line 14b is formed in the active region 12 of the substrate sb to be apart from the first gate line 14a in the first direction (the X direction).

[0115] The first source/drain contact pattern 24 is disposed in the active region 12 at one side of the first gate line 14a. The first source/drain contact pattern 24 may be disposed in the first active contact region 18. When the first source/drain contact pattern 24 is formed, a source/drain loss region 19 may occur in the first active contact region 18. The first source/drain contact pattern 24 may have a second pattern width c in the first direction (the X direction).

[0116] The second source/drain contact pattern 26 is disposed in the active region 12 at one side of the second gate line 14b. The second source/drain contact pattern 26 may be disposed in the second active contact region 20. When the second source/drain contact pattern 26 is formed, a source/drain loss region 21 may occur in the second active contact region 20. The second source/drain contact pattern 26 may have a third pattern width e in the first direction (the X direction).

[0117] The dummy contact region 22-3 may be formed between the first gate line 14a and the second gate line 14b. The dummy contact region 22-3 may include first to third dummy contact regions 22h to 22i apart from each other in the first direction (the X direction).

[0118] A dummy source/drain contact pattern 28-4 is disposed in the active region 12 between the first gate line 14a and the second gate line 14b. The dummy source/drain contact pattern 28-4 may be disposed in the dummy contact region 22-3.

[0119] The dummy source/drain contact pattern 28-4 may include first and second dummy source/drain contact patterns 28i and 28j. The first dummy source/drain contact pattern 28i may be formed on the first dummy contact region 22h. When the first dummy source/drain

contact pattern 28i is formed, a dummy source/drain loss region 34-1 may occur in the first dummy contact region 22h.

[0120] The first dummy source/drain contact pattern 28i may have a first sub-pattern width a' in the first direction (the X direction). The first sub-pattern width a' may be less than the third pattern width c.

[0121] The second dummy source/drain contact pattern 28j may be formed on the second dummy contact region 22i. The second dummy source/drain contact pattern 28j may not be in contact with the second dummy contact region 22i. The second dummy source/drain contact pattern 28j may have a second sub-pattern width a'' in the first direction (the X direction). The second sub-pattern width a'' may be less than the first sub-pattern width a' and the third pattern width c. A dummy source/drain contact pattern may not be formed on the second dummy contact region 22j.

[0122] As described above, the dummy source/drain contact pattern 28-4 of the semiconductor device EX8 may have a width less than the first source/drain contact pattern 24 and the second source/drain contact pattern 26. Accordingly, in the semiconductor device EX8 of inventive concepts, resistance of the dummy contact region 22-3 may be reduced by reducing the size of the dummy source/drain loss region 34-1 located below the dummy source/drain contact pattern 28-4.

[0123] As a result, in the semiconductor device EX8 of an embodiment inventive concepts, device resistance between the first active contact region 18 (or the first source/drain region) and the second active contact region 20 (or the second source/drain region) may be reduced during a device operation.

[0124] FIG. 15 is a cross-sectional view illustrating an active contact structure ACA used in a semiconductor device according to inventive concepts.

[0125] In an embodiment, the active contact structure ACA may be used in the semiconductor devices (e.g., EX1 to EX9 described above) according to inventive concepts. The active contact structure ACA may include a first active contact structure ACA-1, a second active contact structure ACA-2, and a third active contact structure ACA-3. At least one of a first active contact structure ACA-1, a second active contact structure ACA-2, and a third active contact structure ACA-3 may be used in the semiconductor devices (e.g., EX1 to EX9 described above) of inventive concepts.

[0126] The first active contact structure ACA-1 may include a source/drain contact pattern 24-1, a first via 40a, a first wiring layer 42a, a third via 44a, and a second wiring layer 46a. The first active contact structure ACA-1 includes the source/drain contact pattern 24-1 formed on

a source/drain region (e.g., 18 of FIG. 3) formed in the substrate sb. The source/drain contact pattern 24-1 may be connected to the second wiring layer 46a through the first via 40a, the first wiring layer 42a, and the third via 44a.

[0127] The second active contact structure ACA-2 may include a source/drain contact pattern 24-2, a first via 40b, a first wiring layer 42b, a second via 40c, and a gate line 14-2. The first active contact structure ACA-2 includes the source/drain contact pattern 24-2 formed on a source/drain region (e.g., 18 of FIG. 3) formed in the substrate sb. The source/drain contact pattern 24-2 may be connected to the gate line 14-2 through the first via 40b, the first wiring layer 42b, and the second via 40c.

[0128] The third active contact structure ACA-3 may include a first source/drain contact pattern 24-3, a first via 40d, a first wiring layer 42c, a second via 40e, a gate line 14-3, and a second source/drain contact pattern 26-1. The third active contact structure ACA-3 includes the first source/drain contact pattern 24-3 formed on the source/drain region (e.g., 18 of FIG. 3) formed on the substrate sb and the second source/drain contact pattern 26-1 formed on the source/drain region (e.g., 20 of FIG. 3) formed on the substrate sb. The first source/drain contact pattern 24-3 may be connected to the second source/drain contact pattern 26-1 through the first via 40d, the first wiring layer 42c, and the second via 40e.

[0129] FIG. 16 is a cross-sectional view illustrating an embodiment of a dummy contact structure DCA1 used in a semiconductor device according to an embodiment of inventive concepts.

[0130] In an embodiment, the dummy contact structure DCA1 may be used in the semiconductor devices (e.g., EX1 to EX9 described above) according to inventive concepts. The dummy contact structure DCA1 may include a first dummy contact structure DCA-1 and a second dummy contact structure DCA-2. At least one of the first dummy contact structure DCA-1 and the second dummy contact structure DCA-2 may be used in the semiconductor devices (e.g., EX1 to EX9 described above) according to inventive concepts.

[0131] The first dummy contact structure DCA-1 may include a dummy source/drain contact pattern 28-5a, a first via 48a, a second via 48b, and a first wiring layer 50a. The first dummy contact structure DCA-1 includes the dummy source/drain contact pattern 28-5a formed on the dummy source/drain region (e.g., 22 of FIG. 3) formed in the substrate sb. In a first portion PO1 of the first dummy contact structure DCA-1, the dummy source/drain contact patterns 28-5a may not be connected to the first via 48a, and the first via 48a may be connected to the first wiring layer 50a.

[0132] In a second portion PO2 of the first dummy contact structure DCA-1, the dummy source/drain contact patterns 28-5a may be connected to the second via 48b, and the second via 48b may not be connected to the first wiring layer 50a. In a third portion PO3 of the first dummy contact structure DCA-1, the dummy source/drain contact pattern 28-5a may not include a via and may not be connected to the first wiring layer 50a.

[0133] The second dummy contact structure DCA-2 may include a dummy source/drain contact patterns 28-5b, a first via 48c, a first wiring layer 50b, a second via 52a, a third via 52b, and a second wiring layer 54. The second dummy contact structure DCA-2 includes the dummy source/drain contact pattern 28-5b formed on the dummy source/drain region (e.g., 22 of FIG. 3) formed in the substrate sb. In a fourth portion PO4 of the second dummy contact structure DCA-2, the dummy source/drain contact pattern 28-5b may be connected to the first wiring layer 50b through the first via 48c, and the first wiring layer 50b may not be connected to the second via 52a.

[0134] In a fifth portion PO5 of the second dummy contact structure DCA-1, the dummy source/drain contact pattern 28-5b may be connected to the first wiring layer 50b through the first via 48c, and the first wiring layer 50b may be connected to the third via 52b.

[0135] In a sixth portion PO6 of the second dummy contact structure DCA-2, the dummy source/drain contact pattern 28-5b may be connected to the first wiring layer 50b through the first via 48c, and the first wiring layer 50b may not be connected to the second wiring layer 54.

[0136] FIG. 17 is a cross-sectional view illustrating an embodiment of a dummy contact structure DCA2 used in a semiconductor device according to inventive concepts.

[0137] In an embodiment, the dummy contact structure DCA2 may be used in the semiconductor devices (e.g., EX1 to EX9 described above) according to inventive concepts. The dummy contact structure DCA2 may include a third dummy contact structure DCA-3 and a fourth dummy contact structure DCA-4. At least one of the third dummy contact structure DCA-3 and the fourth dummy contact structure DCA-4 may be used in the semiconductor devices (e.g., EX1 to EX9 described above) according to inventive concepts.

[0138] The third dummy contact structure DCA-3 may include a dummy source/drain contact pattern 28-6a, a first via 56a, a second via 56b, a third via 56c, a first wiring layer 58a, and a gate line 14-4. The third dummy contact structure DCA-3 includes the dummy source/drain contact pattern 28-6a formed on the dummy source/drain region (e.g., 22 of FIG. 3) formed in the substrate sb.

[0139] In a seventh portion PO7 of the third dummy contact structure DCA-3, the dummy source/drain contact patterns 28-6a may be connected to the first wiring layer 58a through the

first via 56a, and the second via 56b located below the first wiring layer 58a may not be connected to the gate line 14-4.

[0140] In an eighth portion PO8 of the third dummy contact structure DCA-3, the dummy source/drain contact patterns 28-may be connected to the first wiring layer 58a through the first vias 56a, and the first wiring layer 58a may not be connected to the third via 56c on the gate line 14-4.

[0141] In a ninth portion PO9 of the third dummy contact structure DCA-3, the dummy source/drain contact pattern 28-6a may be connected to the first wiring layer 58a through the first vias 56a, and the first wiring layer 58a may not be connected to the gate line 14-4.

[0142] The fourth dummy contact structure DCA-4 may include a first dummy source/drain contact pattern 28-6b, a first via 56d, a second via 56e, a third via 56f, a first wiring layer 58b, and a second dummy source/drain contact pattern 28-6c. The fourth dummy contact structure DCA-4 includes the first dummy source/drain contact pattern 28-6b formed on the dummy source/drain region (e.g., 22 of FIG. 3) formed in the substrate sb.

[0143] In a tenth portion PO10 of the fourth dummy contact structure DCA-4, the first dummy source/drain contact patterns 28-6b may be connected to the first wiring layer 58b through the first vias 56d, and the second via 56e located below the first wiring layer 58b may not be connected to the second dummy source/drain contact pattern 28-6c.

[0144] In an eleventh portion PO11 of the fourth dummy contact structure DCA-4, the first dummy source/drain contact patterns 28-6b may be connected to the first wiring layer 58b through the first via 56d, and the first wiring layer 58b may not be connected to the third via 58f on the second dummy source/drain contact pattern 28-6c.

[0145] In a twelfth portion PO12 of the fourth dummy contact structure DCA-4, the first dummy source/drain contact patterns 28-6b may be connected to the first wiring layer 58b through the first via 56d, and the first wiring layer 58b may not be connected to the second dummy source/drain contact pattern 28-6c.

[0146] FIG. 18 is a schematic diagram illustrating an electronic system 100 including a semiconductor device according to an embodiment of inventive concepts.

[0147] In an embodiment, the electronic system 100 may include a controller 110, an input/output (I/O) device 120, a memory 130, and an interface 140. The electronic system 100 may be a mobile system or a system for transmitting or receiving information. The mobile system may be a personal digital assistant (PDA), a portable computer, a web tablet, a wireless phone, a mobile phone, a digital music player, or a memory card.

[0148] The controller 110 may serve to execute a program and control the system 100. The controller 110 may include a semiconductor device according to an embodiment of inventive concepts. The controller 110 may be, for example, a microprocessor, a digital signal processor, a microcontroller, or a similar device.

[0149] The I/O device 120 may be used to input or output data of the electronic system 100. The electronic system 100 may be connected to an external device such as a personal computer or a network using the I/O device 120 to exchange data with the external device. The I/O device 120 may be, for example, a keypad, a keyboard, or a display.

[0150] The memory 130 may store codes and/or data for an operation of the controller 110, and/or store data processed by the controller 110. The memory 130 may include the semiconductor devices EX1 to EX9 according to an embodiment of inventive concepts. The interface 140 may be a data transmission path between the electronic system 100 and another external device. The controller 110, the I/O device 120, the memory 130, and the interface 140 may communicate with each other through a bus 150.

[0151] For example, the electronic system 100 may be used in mobile phones, MP3 players, navigation systems, portable multimedia players (PMPs), solid state disks (SSDs), or household appliances.

[0152] One or more of the elements disclosed above may include or be implemented in processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the processing circuitry more specifically may include, but is not limited to, a central processing unit (CPU) , an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), a System-on-Chip (SoC), a programmable logic unit, a microprocessor, application-specific integrated circuit (ASIC), etc.

[0153] It should be understood that embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each embodiment should typically be considered as available for other similar features or aspects in other embodiments. While some embodiments of inventive concepts have been particularly shown and described, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate including an active region;

a first gate line and a second gate line in the active region,

the first gate line and the second gate line being spaced apart from each other in a first direction and extending in a second direction, the second direction crossing the first direction;

a first source/drain contact pattern in the active region at one side of the first gate line;

a second source/drain contact pattern in the active region at one side of the second gate line; and

a dummy source/drain contact pattern in the active region between the first gate line and the second gate line, wherein

a size of the dummy source/drain contact pattern is less than a size of the first source/drain contact pattern and a size of the second source/drain contact pattern.

2. The semiconductor device of claim 1, wherein the dummy source/drain contact pattern is spaced apart in the second direction from a first edge of the active region, a second edge of the active region, or both the first edge of the active region and the second edge of the active region.

3. The semiconductor device of claim 1 or claim 2, wherein

the dummy source/drain contact pattern includes a plurality of dummy source/drain contact patterns, and

sizes of the plurality of dummy source/drain contact patterns are less than a size of the first source/drain contact pattern and a size of the second source/drain contact pattern.

4. The semiconductor device of any one of claims 1 to 3, wherein

the active region includes a dummy contact region between the first gate line and the second gate line,

the dummy contact region includes a dummy source/drain region in the substrate, and

the active region includes a dummy source/drain loss region in the dummy source/drain region below the dummy source/drain contact pattern.

5. The semiconductor device of any one of claims 1 to 4, wherein

the dummy source/drain contact pattern has a first pattern width in the first direction and a first pattern length in the second direction,

the first source/drain contact pattern has a second pattern width in the first direction and a second pattern length in the second direction,

the second source/drain contact pattern has a third pattern width in the first direction and a third pattern length in the second direction,

the first pattern width is equal to the second pattern width and the third pattern width, and

the first pattern length is less than the second pattern length and the third pattern length.

6. The semiconductor device of any one of claims 1 to 5, wherein the dummy source/drain contact pattern includes a plurality of sub-dummy source/drain contact patterns spaced apart from each other.

7. A semiconductor device comprising:

a substrate including an active region having a first region width in a first direction and a first region length in a second direction, the second direction perpendicular to the first direction,

the active region including a first active contact region, a second active contact region, and a dummy contact region between the first active contact region and the second active contact region;

a first gate line and a second gate line extending in the second direction in the active region, the second gate line spaced apart from the first gate line in the first direction,

the first gate line and the second gate line in the active region with the first active contact region at one side of the first gate line, the second active contact region at one side of the second gate line, and the dummy contact region between the first gate line and the second gate line;

a first source/drain contact pattern in the first active contact region, the first source/drain contact pattern being spaced apart from the first gate line in the first direction; and

a second source/drain contact pattern in the second active contact region, the second source drain/contact pattern being spaced apart from the second gate line in the first direction.

8. The semiconductor device of claim 7, wherein

the first source/drain contact pattern has a second pattern width in the first direction and a second pattern length in the second direction,

the second source/drain contact pattern has a third pattern width in the first direction and a third pattern length in the second direction,

the first region length is equal to the second pattern length and the third pattern length, and

the first region width is greater than the second pattern width and the third pattern width.

9. A semiconductor device comprising:

a substrate including an active region, the active region including a first active contact region, a second active contact region, and a plurality of dummy contact regions in the active region;

a plurality of gate lines spaced apart from each other in a first direction in the active region, the plurality of gate lines extending in a second direction perpendicular to the first direction in the active region, the plurality of gate lines including a first gate line and a second gate line,

the plurality of gate lines in the active region with the first active contact region at one side of the first gate line and the second active contact region at one side of the second gate line, and the plurality of dummy contact regions in the active region between the plurality of gate lines;

a first source/drain contact pattern in the first active contact region;

a second source/drain contact pattern in the second active contact region; and

a plurality of dummy source/drain contact patterns in at least one of the plurality of dummy contact regions,

wherein sizes of the plurality of dummy source/drain contact patterns are less than a size of the first source/drain contact pattern and a size the second source/drain contact pattern.

10. The semiconductor device of claim 9, wherein the plurality of dummy source/drain contact patterns have different pattern widths in the first direction.