

DIGITAL ENCODER

5 The present invention relates to a digital encoder, and is concerned particularly although not exclusively with a digital encoder for use in a digital camera.

10 Recently, cameras have tended to be converted from analog systems to digital systems. As a result, a digital encoder for processing digital chrominance and luminance signals and generating a suitable burst signal is demanded for use in a digital camera, and such a digital encoder may be applicable to a surveillance camera, a camera for use in industry or home, etc.

15 Preferred embodiments of the present invention aim to provide a digital encoder for modulating the levels and phases of colour difference signals.

20 It is an another aim to provide a compatible digital encoder for use in both NTSC (National Television System Committee) and PAL (Phase Alternation by Line) systems by variegating the levels and phases of colour difference and burst signals.

25 According to an aspect of the present invention, a digital encoder includes a frequency converting circuit for converting a colour difference signal into a sub-carrier frequency. A digital modulator determines a level and phase of a converted colour difference signal in response to first control signals, and a burst generator determines a level and phase of the burst signal in response to second control signals. A chroma encoder receives outputs of

the digital modulator and the burst generator, and generates a chrominance signal in response to third control signals.

5 The digital modulator of the digital encoder may invert colour difference signals R-Y every other horizontal synchronizing signal in response to a line alternate signal.

10 A burst generating unit of the digital encoder may control, in response to the line alternate signal, a switching operation of data supplied from registers, so as to determine a level and phase of the burst signal.

According to another aspect of the present invention, there is provided a digital encoder means comprising:

15 a frequency converting means for converting a colour difference signal into a sub-carrier frequency;

20 a modulating means for receiving a converted colour difference signal and determining a level and phase of said converted colour difference signal in response to first control signals;

a register means having phase information of a burst signal;

25 a burst generating means for receiving data of said register means, and determining a level and phase of said burst signal in response to second control signals; and

a chroma encoder means for receiving outputs of said modulating means and said burst generating means, and generating a chrominance signal in response to third control signals.

5 Preferably, said first control signals comprise a line alternate signal, a sub-carrier frequency and a twice sub-carrier frequency.

10 Preferably, said second control signals comprise a line alternate signal, a sub-carrier frequency, a twice sub-carrier frequency, a four times sub-carrier frequency, a burst flag signal and a mode select signal.

Preferably, said line alternate signal is set to a given logic state when the said digital encoder means is used in the NTSC system.

15 Preferably, said line alternate signal alternates between logic "low" state and logic "high" state when the said digital encoder means is used in the PAL system.

Preferably, said modulating means comprise:

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a first exclusive OR gate for receiving a first signal of said converted colour difference signal and a line alternate signal, and determining a level and phase of said first signal of said converted colour difference signal;

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a first multiplexer means for receiving and multiplexing a second signal of said converted colour difference signal transmitted from said frequency converting means and an output of said first exclusive OR gate, in response to a sub-carrier frequency;

a second exclusive OR gate for receiving an output of said first multiplexer means and said sub-carrier frequency, and determining a level and phase of said output of said first multiplexer means, in response to said sub-carrier frequency.

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Preferably, said first exclusive OR gate operates only as a buffer, or operates alternately as a buffer and an inverter, in response to said line alternate signal.

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Preferably, said second exclusive OR gate operates only as a buffer, or operates alternately as a buffer and an inverter, in response to said sub-carrier frequency.

Preferably, said burst generating means comprises:

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a switching means for switching data transmitted from said register means, in response to said line alternate signal;

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a second multiplexer means for multiplexing a signal transmitted from said switching means, in response to said twice sub-carrier frequency;

a third exclusive OR gate for exclusive-ORing an output of said second multiplexer and said sub-carrier frequency;

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a burst generator means for receiving an output of said third exclusive OR gate and generating said burst signal in response to said line alternate signal, said four times sub-carrier frequency, said burst flag signal and said mode select signal.

Preferably, said third exclusive OR gate operates only as a buffer, or operates alternately as a buffer and an inverter, in response to said sub-carrier frequency.

- 5 Preferably, said third control signals comprises a fade signal, a composite blank signal and a gain signal.

Preferably, said chroma encoder means comprises:

- 10 a combinational means for combining said fade signal, said composite blank signal and said gain signal;

a fifth multiplexer means for receiving and multiplexing outputs of said combinational means and said modulating means; and

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a first mixer means for combining an output of said fifth multiplexer means with said burst signal of said burst generating means, so as to generate a digital chrominance signal.

- 20 A digital encoder means as above may further comprise at least one frequency divider for dividing a sub-carrier frequency by a given number.

Preferably, said given number is two.

- 25 Said burst generating means may comprise:

a fourth exclusive OR gate for receiving and exclusive-ORing data of a first register means of said register means and said line alternate signal;

a second multiplexer means for receiving and multiplexing an output of said fourth exclusive OR gate and data of a second register means of said register means, in response to said twice sub-carrier frequency;

5 a second inverter means for inverting said sub-carrier frequency;

a fifth exclusive OR gate for receiving and exclusive-ORing an output of said second inverter and said mode select signal;

10 a third exclusive OR gate for receiving and exclusive-ORing outputs of said fifth exclusive OR gate and said second multiplexer means; and

a burst generator means for receiving an output of said third exclusive OR gate and generating said burst signal in response to said line alternate signal, said four times sub-carrier frequency and said burst flag signal.

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Preferably, said burst generator means comprises:

a first inverter means for inverting said output of said third exclusive OR gate;

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a third multiplexer means for receiving and multiplexing outputs of said first inverter means and said third exclusive OR gate, in response to said line alternate signal;

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a second mixer means for combining an output of said third multiplexer with said four times sub-carrier frequency;

a fourth multiplexer means for receiving and multiplexing outputs of said second mixer means and said first inverter means, in response to said mode select signal;

5 a synchronizing means for synchronizing said burst flag signal with said four times sub-carrier frequency; and

an AND gate for receiving and ANDing an outputs of said synchronizing means and said fourth multiplexer.

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The invention extends to a camera provided with a digital encoder according to any of the preceding aspects of the invention.

15 For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example only, to the accompanying diagrammatic drawings, in which:

Figure 1 is a schematic block diagram of one example of a digital encoder according to the present invention;

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Figure 2 is a block diagram showing a preferred embodiment of Figure 1;

25 Figure 3 is a detailed block diagram of a burst generator shown in Figure 2;

Figures 4A to 4H are waveforms appearing at each portion of Figures 1 and 2;

Figures 5A to 5C are vector diagrams showing phases of a burst signal;
and

Figure 6 is a block diagram showing another preferred embodiment of
5 Figure 1.

In the figures, like reference numerals denote like or corresponding
parts.

10 Referring to Figure 1, a time-division digital colour difference signal
R-Y/B-Y is applied to a demultiplexer 1 and separated into two colour
difference signals B-Y and R-Y. In this case, a frequency of a clock signal
CLK is at least twice the frequency of the signals R-Y and B-Y, in order to
separate the colour difference signals B-Y and R-Y without distortion. The
15 two signals R-Y and B-Y transmitted from the demultiplexer 1 are supplied
to a sub-carrier frequency converter 3 through a low-pass filter 2, and
converted into a sub-carrier frequency. The frequency converted signals are
supplied to a digital modulator 4 to be modulated and compressed in response
to a line alternate signal LALT, a sub-carrier frequency FSC and a twice sub-
20 carrier frequency 2FSC. A modulated and compressed signal is provided to
a chroma encoder 5.

A burst generating circuit 8 receives, from registers 6 and 7, data
having phase information with respect to NTSC and PAL systems
25 respectively, and generates a burst signal under control of the line alternate
signal LALT, the sub-carrier frequency FSC, the twice sub-carrier frequency
2FSC, a four times sub-carrier frequency 4FSC, a burst flag signal BF and
a mode select signal MODE for selecting either NTSC or PAL system. The

burst signal BURST, generated by the burst generating circuit 8, is provided to the chroma encoder 5. The chroma encoder 5, receiving output of the digital modulator 4 and the burst signal BURST, produces a digital chrominance signal C_{out} in response to a fade signal FADE, a composite blank signal C-BLK and a gain signal GAIN. Moreover, a luminance signal Y_H is sent to a luminance encoder 10 through a low-pass filter 9, and the luminance encoder 10 generates a digital luminance signal Y_{out} in response to the fade signal FADE, the gain signal GAIN, a composite synchronizing signal C-SYNC, the composite blank signal C-BLK and a luminance control signal YC.

Referring to Figure 2, there is shown one example of a preferred embodiment of Figure 1. Signals B-Y and R-Y separated from the demultiplexer 1 are supplied to low-pass filters 21 and 22 for filtering frequency of separated signals B-Y and R-Y. If a frequency (clock frequency) of the input signal of a digital modulator 4 and a sub-carrier frequency are not identical to each other, a signal to be modulated can not be modulated. Therefore, the frequencies of separated signals R-Y and B-Y are respectively converted into sub-carrier frequency through sub-carrier frequency converters 31 and 32, and then, the converted signals are supplied to the digital modulator 4. In this case, while the output signal from the sub-carrier frequency converter 31 is directly supplied to a multiplexer 41 of the digital modulator 4, the output signal from the sub-carrier frequency converter 32 is applied to the multiplexer 41 via an exclusive OR gate 42 together with a line alternate signal LALT.

If the digital encoder is used in the NTSC system, the line alternate signal LALT is at the logic "low" state, and the exclusive OR gate 42

operates as a buffer. However, if the digital encoder is used in the PAL system, the line alternate signal LALT is alternately at the logic "high" and "low" states every horizontal synchronizing signal. Accordingly, the exclusive OR gate 42 operates as a buffer and an inverter alternately, so that
5 the level and phase of the signal R-Y are alternately inverted and not inverted every horizontal synchronizing signal.

The multiplexer 41 receives the output signal of the sub-carrier frequency converter 31 and the output of the exclusive OR gate 41, and
10 operates in response to the signal 2FSC produced from a frequency divider 11 for dividing the signal 4FSC by two. An exclusive OR gate 43, receiving the output signal of the multiplexer 41, supplies the output thereof to a multiplexer 51 of the chroma encoder 5, in response to the signal FSC produced from a frequency divider 12 for dividing the signal 2FSC by two.
15 That is, the exclusive OR gate 43 operates as an inverter or a buffer when the signal FSC is at the logic "high" or logic "low" state, so that the level and phase of the output of the multiplexer 41 are alternately inverted and not inverted. As a result, colour difference signals B-Y and R-Y are digitally modulated in the digital encoder. The multiplexer 51 of the chroma encoder
20 5 supplies the output thereof to a mixer 53 of the chroma encoder 5 in response to the fade signal FADE, the composite blank signal C-BLK and the gain signal GAIN.

On the other hand, the registers 6 and 7 having phase information of
25 the burst signal are connected to a multiplexer 82 of the burst generating circuit 8 through a switch 81 which operates in response to the line alternate signal LALT. If the digital encoder is used in the NTSC system, the line alternate signal LALT is at the logic "low" state and output terminals X1, X2

of the switch 81 are coupled to the input terminals L1, L2 so as to transmit data of the registers 6 and 7 to the multiplexer 82. However, in the PAL system, the line alternate signal LALT is alternately at the logic "high" and the logic "low" states every horizontal synchronizing signal, and output terminals X1, X2 of the switch 81 are alternately coupled to input terminals H1, H2 and input terminals L1, L2, so that the level and phase of the outputs of the registers 6 and 7 supplied to the multiplexer 82 are inverted every other horizontal synchronizing signal. The output of the multiplexer 82 is supplied to an exclusive OR gate 83 together with the sub-carrier frequency FSC. In this case, if the signal FSC is at the logic "high" state, the exclusive OR gate 83 operates as an inverter, and if it is at the logic "low" state, the exclusive OR gate 83 operates as a buffer. Therefore, since the output of the exclusive OR gate 83 is changed in its phase and level every horizontal synchronizing signal, the phase and level of the burst signal are adjusted.

A signal BURST' generated by the exclusive OR gate 83 is provided to a burst generator 84 for generating a burst signal BURST suitable for NTSC and PAL systems, in response to the line alternate signal LALT, the signal 4FSC, a burst flag signal BF and the signal MODE. Thus, the burst signal selected for either NTSC or PAL system in the burst generator 84 is supplied to the mixer 53 of the chroma encoder 5 and mixed with the output signal of the multiplexer 51 of the chroma encoder 5, to generate the digital chrominance signal C_{out} .

A detailed example of the burst generator 84 is illustrated in Figure 3. The signal BURST' is fed to multiplexers 842 and 843 through an inverter 841. Output of the multiplexer 843 is supplied to a mixer 844 in response to the line alternate signal LALT. The mixer 844 combines the output of the

5 multiplexer 843 with the signal 4FSC, and the output thereof is applied to the multiplexer 842. The multiplexer 842 receives the outputs of the inverter 841 and the mixer 844, and generates the output of the inverter 841 to an AND gate 845 in response to the signal MODE. Meanwhile, the burst flag signal
10 BF in an active state during a burst period is synchronized with the signal 4FSC through a synchronizing circuit 846 and supplied to one input terminal of an AND gate 845. If the digital encoder is used in the NTSC system, since the signal LALT is at the logic "low" state, the AND gate 845 receives the output of the multiplexer 842 and the signal BF, and generates the burst
15 signal BURST. However, if the digital encoder is used in the PAL system, the signal LALT alternates between the logic "high" and the logic "low" states every horizontal synchronizing signal, so that the burst signal BURST is produced by ANDing with the signal BF and the output of the multiplexer 842 which is inverted every other horizontal synchronizing signal.

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Referring to Figure 4A, there is shown the signal 4FSC to be supplied to the frequency divider 11. Figure 4B and Figure 4C show respectively 2FSC and FSC signals produced by the frequency dividers 11, 12. Figure 4D and 4E show the signal R-Y and B-Y respectively, to be applied into the
20 digital modulator 4 shown in Figure 2. Figure 4F shows output of the multiplexer 4. Figure 4G is a converted analog output of the exclusive OR gate 43, for better understanding, when the digital output of the exclusive OR gate 43 is converted into an analog waveform. Figure 4H illustrates a waveform obtained when the analog waveform of Figure 4G is passed through
25 a low-pass filter.

Figure 5A illustrates data of registers 6 and 7 respectively, when the digital encoder is used in the NTSC system. The registers 6 and 7 hold the

R-Y component and B-Y component of the burst signal, respectively. Further, since the line alternate signal LALT is set to the logic "low" state, the phase of the burst signal can be adjusted simply. However, in the case that the digital encoder is used in the PAL system, since the line alternate signal LALT is varied every horizontal synchronizing signal, the R-Y component of the burst signal is inverted as shown in Figure 5B. In the PAL system, since the phase difference between burst signals BURST+ and BURST- must be maintained at 90°, outputs of registers 6 and 7 should be altered in response to the signal LALT. Figure 5C shows that the burst signal maintains a phase difference of 90° when the digital encoder is used in the PAL system. Burst signals P and Q have a phase difference of 90° to each other for use in the PAL system, and if it is desired to have burst signals of P' and Q' while maintaining the phase difference of 90°, P(P_x, P_y) and Q(Q_x, Q_y) should be changed to P'(P'_x, P'_y) and Q'(Q'_x, Q'_y), respectively. In this case, the following relationships are satisfied:

$$Q'_x = P'_y \text{ and } P'_x = Q'_y.$$

That is, this result coincides with that obtained when the outputs of the registers 6 and 7 are altered in the switch 81 in response to the line alternate signal LALT.

In Figure 6, another example of a preferred embodiment of the digital encoder is shown. An exclusive OR gate 201 is used instead of the switch 81 of Figure 2, and operates as a buffer or an inverter in response to the line alternate signal LALT. Moreover, instead of a mode select signal MODE directly applied to the burst generating circuit 8, an exclusive OR gate 202 is

As described above, the illustrated digital encoder is compatibly used in both NTSC and PAL systems and widely applicable to a digital supervisory camera, a camera for use in industry or home, and the like.

5. While preferred embodiments of the invention have been particularly shown and described, it will be understood by those skilled in the art that modifications in detail may be made without departing from the scope of the invention.



CLAIMS

1. A digital encoder means comprising:

5 a frequency converting means for converting a colour difference signal into a sub-carrier frequency;

a modulating means for receiving a converted colour difference signal and determining a level and phase of said converted colour difference signal
10 in response to first control signals;

a register means having phase information of a burst signal;

a burst generating means for receiving data of said register means, and
15 determining a level and phase of said burst signal in response to second control signals; and

a chroma encoder means for receiving outputs of said modulating means and said burst generating means, and generating a chrominance signal
20 in response to third control signals.

2. A digital encoder means as claimed in claim 1, wherein said first control signals comprise a line alternate signal, a sub-carrier frequency and a twice sub-carrier frequency.

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3. A digital encoder means as claimed in claim 1 or 2, wherein said second control signals comprise a line alternate signal, a sub-carrier frequency, a twice sub-carrier frequency, a four times sub-carrier frequency, a burst flag signal and a mode select signal.



4. A digital encoder means as claimed in claim 2 or 3, wherein said line alternate signal is set to a given logic state when the said digital encoder means is used in the NTSC system.

5 5. A digital encoder means as claimed in claim 2 or 3, wherein said line alternate signal alternates between logic "low" state and logic "high" state when the said digital encoder means is used in the PAL system.

6. A digital encoder means as claimed in any of the preceding claims,
10 wherein said modulating means comprise:

15 a first exclusive OR gate for receiving a first signal of said converted colour difference signal and a line alternate signal, and determining a level and phase of said first signal of said converted colour difference signal;

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a first multiplexer means for receiving and multiplexing a second signal of said converted colour difference signal transmitted from said frequency converting means and an output of said first exclusive OR gate, in response to a sub-carrier frequency;

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a second exclusive OR gate for receiving an output of said first multiplexer means and said sub-carrier frequency, and determining a level and phase of said output of said first multiplexer means, in response to said sub-carrier frequency.

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7. A digital encoder as claimed in claim 6, wherein said first exclusive OR gate operates only as a buffer, or operates alternately as a buffer and an inverter, in response to said line alternate signal.



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8. A digital encoder as claimed in claim 7, wherein said second exclusive OR gate operates only as a buffer, or operates alternately as a buffer and an inverter, in response to said sub-carrier frequency.

5 9. A digital encoder means as claimed in claim 3 or any of claims 4 to 8 as appendant thereto, wherein said burst generating means comprises:

a switching means for switching data transmitted from said register means, in response to said line alternate signal;

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a second multiplexer means for multiplexing a signal transmitted from said switching means, in response to said twice sub-carrier frequency;

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a third exclusive OR gate for exclusive-ORing an output of said second multiplexer and said sub-carrier frequency;

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a burst generator means for receiving an output of said third exclusive OR gate and generating said burst signal in response to said line alternate signal, said four times sub-carrier frequency, said burst flag signal and said mode select signal.

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10. A digital encoder means as claimed in claim 9, wherein said third exclusive OR gate operates only as a buffer, or operates alternately as a buffer and an inverter, in response to said sub-carrier frequency.

11. A digital encoder means as claimed in any of the preceding claims, wherein said third control signals comprises a fade signal, a composite blank signal and a gain signal.



12. A digital encoder means as claimed in claim 11, wherein said chroma encoder means comprises:

5 a combinational means for combining said fade signal, said composite blank signal and said gain signal;

a fifth multiplexer means for receiving and multiplexing outputs of said combinational means and said modulating means; and

10 a first mixer means for combining an output of said fifth multiplexer means with said burst signal of said burst generating means, so as to generate a digital chrominance signal.

13. A digital encoder means as claimed in claim 12, further comprising at
15 least one frequency divider for dividing a sub-carrier frequency by a given number.

14. A digital encoder means as claimed in claim 13, wherein said given
20 number is two.

15. A digital encoder means as claimed in claim 3 and claim 6, 7 or 8, wherein said burst generating means comprises:

25 a fourth exclusive OR gate for receiving and exclusive-ORing data of a first register means of said register means and said line alternate signal;

a second multiplexer means for receiving and multiplexing an output of said fourth exclusive OR gate and data of a second register means of said register means, in response to said twice sub-carrier frequency;



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a second inverter means for inverting said sub-carrier frequency;

a fifth exclusive OR gate for receiving and exclusive-ORing an output of said second inverter and said mode select signal;

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a third exclusive OR gate for receiving and exclusive-ORing outputs of said fifth exclusive OR gate and said second multiplexer means; and

10 a burst generator means for receiving an output of said third exclusive OR gate and generating said burst signal in response to said line alternate signal, said four times sub-carrier frequency and said burst flag signal.

16. A digital encoder means as claimed in claim 9 or 15, wherein said burst generator means comprises:

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a first inverter means for inverting said output of said third exclusive OR gate;

20 a third multiplexer means for receiving and multiplexing outputs of said first inverter means and said third exclusive OR gate, in response to said line alternate signal;

a second mixer means for combining an output of said third multiplexer with said four times sub-carrier frequency;

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a fourth multiplexer means for receiving and multiplexing outputs of said second mixer means and said first inverter means, in response to said mode select signal;



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a synchronizing means for synchronizing said burst flag signal with said four times sub-carrier frequency; and

an AND gate for receiving and ANDing an outputs of said
5 synchronizing means and said fourth multiplexer.

17. A digital encoder substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.

10 18. A digital encoder substantially as hereinbefore described with reference to Figures 1 to 3 or Figures 1, 3 and 6 of the accompanying drawings.

19. A digital encoder substantially as hereinbefore described with reference to Figures 1 to 5 or Figures 1, 3, 4, 5 and 6 of the accompanying drawings.

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20. A camera provided with a digital encoder according to any of the preceding claims.