D E S C R I P T I O N

A METHOD FOR DEPOSITING A METAL LAYER ON A SEMICONDUCTOR INTERCONNECT STRUCTURE HAVING A CAPPING LAYER

RELATED APPLICATION

This Application is related to U.S. Patent Application Serial No. 10/318,605, entitled "A Method for Depositing a Metal Layer on a Semiconductor Interconnect Structure", filed even date herewith.

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor processing and more particularly relates to the processing of semiconductor wafers incorporating advanced interconnect structures using copper metallurgy.

Advanced interconnect structures using copper metallurgy present a number of technical challenges with regard to functional performance. Foremost among these is achieving a low contact resistance that is stable under thermal cycling, as well as good reliability under electromigration and stress migration.

Electromigration is the movement of the ions in a conductor such as copper in response to the passage of current through it and can ultimately lead to an open-circuit failure of the conductor.

Various prior art approaches have been developed to prevent or limit electromigration, particularly in copper

metal lines and interconnects. Thus, Hsiao et al. U.S. Patent 6,191,029, the disclosure of which is incorporated by reference herein, discloses a method for fabricating a metal interconnect including depositing a barrier metal layer in a trench, depositing a conductive metal such as copper to fill the trench, etching away part of the copper to form a concavity in the trench, and filling the concavity with a top barrier layer and then dielectric material. The conformal top barrier layer over the copper improves electromigration resistance.

Chen U.S. Patent 6,200,890, the disclosure of which is incorporated by reference herein, discloses a method for fabricating a metal interconnect including etching away part of the dielectric layer after copper wire formation so that the copper wires project from the surface of the dielectric layer, and then forming a top barrier layer over the projecting copper wires to prevent electromigration and current leakage.

Nogami et al. U.S. Patent 6,214,731, the disclosure of which is incorporated by reference herein, discloses a process for fabricating a metal interconnect including depositing a barrier metal layer in a trench, treating the barrier metal layer with a silane to form a silicon layer, and depositing copper on the silicon layer to fill the trench, whereby the copper and silicon react to form a copper silicide layer between the barrier metal layer and the deposited copper. The copper silicide layer improves interface defect density and electromigration resistance.

Despite the existence of various prior art methods for addressing the known problems of electromigration, the prior art does not appear to appreciate the contribution made by conventionally-employed metal layer deposition steps to the

problem of electromigration. The failure to realize these challenges has become particularly acute with the employment of organic dielectric films. Thus, the side wall and undercut profiles observed with interconnect structures such as trenches and vias in organic dielectrics present unprecedented difficulties in and of themselves in achieving high-integrity liner and seed layer coverage of such trenches and vias prior to metal filling. Another problem with the organic dielectric films is so-called time dependent dielectric breakdown (TDDB) in which copper, for example, penetrates incomplete side wal layers and poisons the dielectric material. Accordingly, the need continues to exist for methods for fabricating metal interconnects, and particularly copper interconnects, having improved electromigtration resistance and reduced stress migration and which avoid TDDB.

Currently known metal barrier schemes include, among other things, argon sputter cleaning of the patterned dielectric. Conversely, all existing solutions to the problems of electromigration and TDDB known to the present inventors involve depositions of metal layers, or sequences of metal layers, without any contemplation of sputtering steps in between sequential metal layer depositions. In practice, deposition tool vendors specifically recommend against argon sputtering on metal layers, owing to concerns relating to shorting of the shielding.

BRIEF SUMMARY OF THE INVENTION

According to the present invention, there is provided a method for depositing a metal layer on an interconnect structure for a semiconductor wafer, the method comprising the steps of:

(a) providing an interconnect structure comprising a metallic conductor covered by a capping layer and a dielectric layer;

(b) patterning the dielectric layer to form an opening that exposes the capping layer over the metal conductor;

(c) sputter-etching the capping layer to expose the metal conductor and at least partially redepositing the capping layer on a sidewall of the opening; and

(d) depositing at least one metal layer on the wall of the opening and covering the redeposited capping layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The Figures are for illustration purposes only and are not drawn to scale. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows taken in conjunction with the accompanying drawings in which:

Figures 1A to 1E are cross-sectional side views of a semiconductor wafer illustrating a first embodiment of a process according to the present invention for depositing a metal layer.

Figures 2A to 2E are cross-sectional side views of a semiconductor wafer illustrating a second embodiment of a process according to the present invention for depositing a metal layer.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the Figures in more detail, and particularly referring to Figures 1A to 1E, there is illustrated a first embodiment of a process according to the present invention. Referring first to Figure 1A, two levels of semiconductor wafer 10 are shown. A first level includes interlevel dielectric (ILD) layer 12, metal conductive line 14 and capping layer 16. For the sake of clarity, the underlying silicon is not shown. Capping layer 16 protects the metal conductive line 14 from oxidation, humidity and contamination during processing of the next level of semiconductor wafer 10. Additionally, capping layer 16 serves to prevent undesirable diffusion of conductive line 14 into ILD 18. In the next level, ILD 18 is deposited on cap layer 16 using conventional techniques.

Any dielectric material can be used for ILDs 12, 18. However, the demands of current sub-micron high-density integrated circuits require that ILDs 12, 18 preferably constitute organic dielectric layers, and more preferably a low-k organic dielectric layer, i.e., organic dielectric materials having a low dielectric constant generally defined as about 3.0 or less. One preferred example of such a low-k organic dielectric material is SiLK (a poly (arylene ether) available from Dow Chemical). The composition of ILDs 12, 18 are not limited to organic low-k dielectrics. Rather, they may be composed of any low-k dielectric known to one skilled in the art to be useful. Capping layer 16 can be made of any suitable capping material, such as silicon nitride, silicon carbide, silicon oxycarbide, hydrogenated silicon carbide, silicon dioxide, organosilicate glass, and other low-k dielectrics. The metal conductive line 14 may comprise copper, tungsten or aluminum. If the metal conductive line 14 is the

first metal level, then tungsten is preferred while copper is preferred for subsequent levels.

Referring now to Figure 1B, a circuitry pattern 20 is then patterned on and through ILD 18, preferably using conventional lithographic and etch techniques (e.g., reactive ion etching (RIE)). The circuitry pattern includes, for example, an interconnect structure such as trench 20a and via 20b for forming a metal conductive interconnect to metal conductive line 14. The interconnect structure shown is a double damascene structure but this particular structure is not necessary to the present invention. The circuitry pattern can include any desired pattern of lines (trench structures), vias (interconnects) and other structures such as pads and devices such as FETs, conventionally designed into such semiconductor wafers, depending on the predetermined design requirements of the fabricated multi-level semiconductor integrated circuit. Very Large Scale Integration (VLSI) technology may include five or six (or possibly more) levels of patterns of integrated and interconnected circuitry elements having individual features of sub-micron dimension.

As also shown in Figure 1B, the circuitry pattern 20 has now exposed capping layer 16. In the use of copper wiring in semiconductor devices, the metal wiring has to be protected from oxidation, humidity and other environmental contaminants during the processing of ILD 18. This is most particularly true of copper wiring. Hence, the protective capping layer 16. The capping layer 16 may also be used as an etch stop during the patterning of ILD 18.

In the prior art processing method, the capping layer 16 would be removed by reactive ion etching or similar process, the wafer removed from the etching chamber and then transferred to a deposition chamber. During this transfer

process, the metal conductive line 14 would be subjected to the atmosphere, and hence exposure to oxidation and humidity, and possible contamination. After transferring to the deposition chamber, the metal conductive wiring line would be lightly etched to remove any oxidation or contamination.

According to the present invention, a sputter etch is utilized to remove the capping layer 16 over the metal conductive line 14. While argon is shown for purposes of illustration and not limitation, any pure gas such as Ar, He, Ne, Xe, N_2, H_2, NH_3, N_2H_2, or mixtures thereof can be used for the sputter etch process. If desired, the metal conductive line 14 may also be sputter etched so as to etch back the metal conductive line 14 as shown in Figure 1C. Etching back the metal conductive line is an optional step. The present inventors have found that when the capping layer 16 is sputter etched, part of the capping layer 16 is redeposited 22 onto the sidewall of the circuitry pattern 20, more particularly via 20b, as shown in Figure 1C. Such redeposition provides some extra material (particularly useful as extra Cu diffusion barrier material when Cu is the via/trench metal) near the bottom of the circuitry pattern 20, particularly via 20b, and alleviates electromigration and TDDB problems that may arise later.

Sputter etching is a process whereby a wafer is held between two electrically biased electrodes in a vaccum chamber and then a gas is fed into the vacuum chamber to create a plasma which bombards the surface of the wafer. The ionized particles cause etching of the surface of the wafer. Using Ar gas during the sputter etching, the present inventors have found that the preferred operation conditions of the argon sputter etching are as follows: gas flow of 20 sccm argon, temperature of 20 °C, bias of top electrode of 400KHz and 750

W, table bias of 13.56 MHz and 400W, and a process pressure of approximately 0.6 mTorr.

Referring now to Figure 1D, while the wafer is still in the deposition chamber, a liner layer or layers are deposited in the circuitry opening 20. Preferably, a first layer 24 of TaN, Ta, Ti, Ti(Si)N or W is conventionally deposited (e.g., by chemical vapor deposition (CVD), plasma vapor deposition (PVD) or other process) followed by a second conventionally deposited layer 26 of TaN, Ta, Ti, Ti(Si)N, W or Cu. The metal conductive line 14 is now sealed in and may be moved to another chamber if desired. If copper is to be the material for the metal conductive line 14, then a copper seed layer (not shown) may be deposited on top of the second layer 26. In a preferred embodiment, first layer 24 is TaN, second layer 26 is Ta followed by the copper seed layer.

Fill metallurgy 28 is then conventionally deposited followed by a planarization process such as chemical-mechanical polishing or the like to result in the structure shown in Figure 1F. If the fill metallurgy 28 is copper, the wafer is removed from the deposition chamber and copper fill metallurgy 28 is plated conventionally. If the fill metallurgy 28 is W or Al, the W or Al could be deposited in the same deposition chamber or, more in keeping with conventional practice, would be moved to a chamber specially set up to handle the W or Al fill metallurgy 28.

Referring now to Figures 2A to 2E, a second embodiment of a process according to the present invention is described. Figure 2A is identical to Figure 1A previously described including the materials that may be used for the various layers. Similarly, Figure 2B is identical to Figure 1B except that sputter etching does not take place yet.

Referring now to Figure 2C, a first metal layer 24 of TaN, Ta, Ti, Ti(Si)N, or W is conventionally deposited. The semiconductor wafer 10' is now subjected to sputter etching. The operating parameters are similar to those discussed earlier. In this embodiment of the present invention, metal layer 24 and capping layer 16 are sputter etched at the same time to result in the structure shown in Figure 2D. Again, if desired, sputter etching may be continued past the capping layer 16 so as to etch back the metal conductive line 14. The metal layer 24 first, and then capping layer 16 are redeposited 30 onto the sidewall of the via 20b. If the metal conductive line 14 is also sputter etched, then the metal conductive line 14 is redeposited 30 onto the redeposited capping layer.

The horizontal portions of first metal layer 24 on the top of ILD 18 and in trench 20a are usually much thicker than the horizontal portion of first metal layer 24 at the bottom of via 20b as a normal consequence of the deposition process. Accordingly, after sputter etching, the horizontal portions of first metal layer 24 on the top of ILD 18 and in trench 20a remain, although thinned somewhat.

Thereafter, as shown in Figure 2E, a second metal layer 26 of TaN, Ta, Ti, Ti(Si)N, W or Cu is conventionally deposited. The wafer is then removed from the deposition chamber followed by deposition of fill metallurgy 28, preferably plated copper. If copper is used as the fill metallurgy 28, there will usually be deposited a prior copper seed layer. The semiconductor wafer 10' is then planarized by chemical-mechanical polishing or other similar process to result in the structure shown in Figure 2E.

It will be apparent to those skilled in the art having regard to this disclosure that other modifications of this

invention beyond those embodiments specifically described here may be made without departing from the spirit of the invention. Accordingly, such modifications are considered within the scope of the invention as limited solely by the appended claims.

Claims

1. A method for depositing a metal layer on an interconnect structure for a semiconductor wafer, the method comprising the steps of:

(a) providing an interconnect structure comprising a metallic conductor covered by a capping layer and a dielectric layer;

(b) patterning the dielectric layer to form an opening that exposes the capping layer over the metal conductor;

(c) sputter-etching the capping layer to expose the metal conductor and at least partially redepositing the capping layer on a sidewall of the opening; and

(d) depositing at least one layer on the wall of the opening and covering the redeposited capping layer.

2. The method of claim 1 wherein prior to step (c), further comprising the step of depositing a liner layer on a wall and bottom of the opening, and wherein in step (c), the liner layer is also sputter-etched to expose the capping layer and at least partially redeposited on a sidewall of the opening.

3. The method of claim 1 wherein the capping layer is selected from the group consisting of silicon nitride, silicon carbide, silicon oxycarbide, hydrogenated silicon carbide, silicon dioxide and organosilicate glass.

4. The method of claim 1 wherein the capping layer is thinner in thickness than the dielectric layer.

5. The method of claim 1 wherein the at least one layer is selected from the group consisting of TaN, Ta, Ti, Ti(Si)N and W.

6. The method of claim 5 wherein the thickness of the metal is 10 to 500 angstroms.

7. The method of claim 2 wherein the liner layer is selected from the group consisting of TaN, Ta, Ti, Ti(Si)N,and W and the metal layer is selected from the group consisting of TaN, Ta, Ti, Ti(Si)N, W and Cu.

8. The method of claim 7 wherein the liner layer is TaN and the at least one layer is Ta.

9. The method of claim 1 further comprising the step of filling the opening with copper.

10. The method of claim 2 further comprising the step of filling the opening with copper.

11. The method of claim 1 wherein the opening is a via or a trench.

12. The method of claim 1 wherein the metal conductor is selected from the group consisting of copper, tungsten and aluminum.

13. The method of claim 1 wherein a gas for sputter etching is selected from the group consisting of Ar, He, Ne, Xe, N_2, H_2, NH_3, N_2H_2 and mixtures thereof.

14. The method of claim 1 wherein in the step of sputter etching, the sputter etching stops after at least partially sputter etching the metal conductor.

15. The method of claim 1 wherein in the step of sputter etching, the sputter etching stops on a top surface of the metal conductor.