

ABSTRACT

Apparatus is disclosed for asynchronously controlling a pipeline. The control circuitry includes an alternating chain of control circuits and detection circuits. When a full control circuit precedes an empty control circuit in the chain, indicating that the data storage element corresponding to the full control circuit should transfer its data to the next storage element corresponding to the empty control circuit, the detection circuit generates a "move" signal. The "move" signal sets the preceding control circuit to empty and the following control circuit to full, thereby enabling movement of a data element from the preceding to the following stage. Because the control circuits are relatively simple and have predictable signal propagation times, the relative reactions of two adjacent control circuits to the common move signal can be tightly controlled. The control circuitry may control a counterflow pipeline, a forking pipeline, or a merging pipeline.

Figure 4