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## (54) IMPROVEMENTS IN OR RELATING TO LOGIC CIRCUITS

(71) We, TELETYPE CORPORATION, of 5555 Touhy Avenue, Skokie, Cook County, State of Illinois, United States of America, a Corporation organised under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to logic circuits useful in building up code translating circuits suitable for economic fabrication by integrated circuit techniques.

Digital circuitry has played an important role in the growth of electronic industries. As the cost of equipment for performing digital operations is reduced, digital circuits replace more and more analog circuits and find new applications previously not contemplated.

Developments enabling the fabrication of large scale integrated logic circuit arrays have reduced the potential cost of digital equipment. Thousands of devices can be created on a semiconductor substrate which previously was employed for one device. As the size of semiconductor devices is reduced and their packing density is thereby increased, the electrical and thermal parameters which affect the design of such circuitry are altered. For example, as the size of a MOSFET is reduced, the minimum obtainable source-to-drain impedance is increased. As components are placed more closely together, stray capacity is reduced and average allowable power dissipation for each device is reduced. Further, because of the compact arrangement, bringing access leads to the circuitry increases the complexity thereof.

Existing code translating circuits built from discrete components often employ combinations of standard logic gates. These gates, including diodes, resistors and transistors require a bias current from a power supply. If an integrated circuit were built using these existing circuit configurations, the energy supplied from the power supply

would be dissipated on the circuit chip, limiting the packing density obtainable. The logic gate approach suffers from the further disadvantage that more than the minimum number of devices is employed. Further, power supply leads would be required increasing layout complexity.

In some approaches to the design of integrated circuits, field effect transistors are employed. The yields attainable with such circuits are often low because proper circuit operation is dependent upon a narrow range of field effect transistor parameters. Optimum circuit layout is not achieved with conventional field effect transistor circuits because different size devices are required, some of which cannot be minimum size devices.

To overcome some of the above problems, dynamic logic circuits have been developed in which field effect transistors are employed to charge and discharge distributed capacities. These dynamic logic circuits are suitable for many circuit applications. One major drawback, however, is that the logic signals are present for only a predetermined time period therefore requiring synchronizing clock signals. These clock signals require signal routing leads which hamper layout efficiency. Redundant devices for performing some logical functions are still required in various positions of the layout and waste silicon.

According to one aspect of the invention there is provided a logic circuit comprising a first gate connected to be enabled by a signal of predetermined value on a first conductor to connect an input terminal with a first load impedance, a second gate connected to be enabled by a signal of said predetermined value on a second conductor to connect said input terminal with a second load impedance, a third gate connected to be enabled by a signal of said predetermined value on said second conductor to complete an electric path from said first load impedance, and a fourth gate connected to be enabled by a signal of said predetermined value on said first conductor to complete an electric path from said second load im-

pedance, said first and second conductors being energisable such that only one of the load impedances will receive current from said input terminal depending on the energisation of the first and second conductors.

Preferably, each said load impedance comprises respective capacitive means.

Such logic circuits are useful in building up more complex circuits, particularly decoding circuits.

A binary decoding circuit may comprise first and second logic circuits each associated (a) with the same first and second conductors (b) with a different pair of load impedances, and (c) with a different one of first and second input terminals, said first and second input terminals being energisable depending on the value of a first binary digit and said energisation of said second and first conductors depending on the value of a second binary digit, so that a unique one of the load impedances of the two logic circuits will be energised for each combination of said first and second binary digit values.

Preferably, each said gate comprises a field effect transistor having a gate electrode and two controlled electrodes between which the impedance presented is low when a said predetermined signal is applied to the corresponding gate electrode.

There is another way of viewing a decoder as embodied herein in which an "N" bit binary coded word is decoded to provide a one out of  $2^N$  logic signal. Thus, the first and second bits of the binary word are passed through circuits which provide the first and second bits and their complements respectively. One of a pair of controlled terminals of two field effect transistors are driven by the first data bits while one of a pair of controlled terminals of two additional field effect transistors are driven by the complement of the first data bit. The gates of one of the first field effect transistors and one of the additional field effect transistors are driven by the second data bit while the gates of the remaining two field effect transistors are driven by the complement of the second data bit, thereby decoding the first two binary data bits by providing a one out of four logic signal at the second controlled terminals of the four field effect transistors.

By providing four additional field effect transistors, each having one of its controlled terminals connected to the second controlled terminal of a different one of the first four field effect transistors, a low impedance output signal for all states of the binary coded word is ensured. The second controlled terminals of the four additional field effect transistors are connected to the respective gates of the associated first four field effect transistors. The gates of the additional four field effect transistors are driven by the

second bit if their associated field effect transistor is driven by the complement of the second bit. The gates of the remaining additional field effect transistors are driven by the complement of the second bit.

An embodiment of the invention will now be described by way of example, with reference to the accompanying drawing, in which:

Fig. 1 is a schematic diagram showing a circuit embodying the principles of this invention.

Fig. 2 is a truth table describing the logic performed by the circuit of Fig. 1.

When processing information with electronic circuits, it is often necessary to transform data available in one code format to data in another code format before performing specific functions. Most digital data is handled and processed as binary coded words. This format is convenient since a maximum of information can be expressed with a minimum of bits. An "N" bit binary word, for example, contains  $2^N$  information indicative combinations.

To retrieve information stored in a memory, however, it is more convenient to use a different code format. Typically, information is stored in a memory at locations arranged in a matrix array. The number of leads required to access the memory is related to the number of memory locations. Normally, two unique access leads are energized for each memory location. When a binary coded word is provided to indicate which access leads of a matrix are to be energized, a code format translation circuit is required.

A circuit shown in Fig. 1 converts a two bit binary coded data word into a "one out of four" logical signal. The two data bits are applied to input terminals A and B respectively. The "one out of four" output signal appears across output capacitors  $X_1$  to  $X_4$ , respectively in accordance with the truth table in Fig. 2.

The circuit shown in Fig. 1 contains two identical circuits 10 and 11, each enclosed in dashed lines, which serve as basic circuit building blocks. Each circuit, such as circuit 10, includes for enhancement mode, P-channel MOS field effect transistors such as field effect transistors 12, 13, 14, and 16. The field effect transistors 12 and 13 serve as logic devices while the field effect transistors 14 and 16 serve as ground return devices. The circuit 11 includes logic field effect transistors 17 and 18 and ground return field effect transistors 19 and 21. Each field effect transistor employed therein is characterized in that a negative voltage applied to its gate will induce a low impedance between a pair of controlled terminals, while a ground potential applied to its gate will induce a high impedance between the pair of controlled terminals. The term

controlled terminals is used herein to describe the source and drain electrodes because the terms source and drain refer to directions of current flow in the field effect transistor. Since, as will become apparent, the current flowing in the field effect transistors of Fig. 1 changed direction during circuit operation, the terms source and drain are not used.

The input terminals A and B are connected to the circuits 10 and 11 by phase splitters 22 and 23. Each phase splitter 22 and 23 has a single input terminal, input terminals A and B respectively,

and a pair of output terminals A and  $\bar{A}$ ,

and B and  $\bar{B}$ , respectively. A signal will appear on output terminal A which is identical to the signal applied to input terminal A while the complement of the signal applied to input terminal A will appear on

output terminal  $\bar{A}$ . In a like manner the signal applied to the input terminal B will appear on output terminal B while the complement

thereof will appear on output terminal  $\bar{B}$ . It should be apparent that a simple inverter circuit would enable achievement of the function of the phase splitter 22 or 23. When an inverter is employed the input terminals A and B would also serve as output terminals  $\bar{A}$  and  $\bar{B}$  respectively.

The output terminals of phase splitter 22, A and  $\bar{A}$ , are connected to first controlled terminals 24 and 26 (for A), and 27 and 28

(for  $\bar{A}$ ) of logic field effect transistors 12 and 13, and 17 and 18, respectively. The output

terminals of phase splitter 23, B and  $\bar{B}$ , are connected to the gates 29 and 31 (for B),

and 32 and 33 (for  $\bar{B}$ ) of the logic field effect transistors 12 and 17, and 13 and 18, respectively.

In operation a two-bit data signal in which a "1" is represented by a  $-V$  potential and "0" is represented by a ground potential is applied to input terminals A and B. When the two-bit data word is "10" as shown in the first row of the truth table in Fig. 2, a  $-V$  potential appears on output terminal A of the phase splitter 22 while a ground

potential appears on the  $\bar{A}$  output terminal of phase splitter 22. In a like manner a ground potential appears upon output terminal B and a  $-V$  potential appears on out-

put terminal  $\bar{B}$  of the phase splitter 23. The

$-V$  potential on the output terminal  $\bar{B}$

turns ON the logic field effect transistors 18 and 13 while the ground potential on output terminal B maintains the field effect transistors 17 and 12 in an OFF condition. The  $-V$  potential on the output terminal A is passed by the ON field effect transistor 13 to the output capacitor  $X_1$ .

The other three output capacitors  $X_2$ — $X_4$  do not respond in this example (10). Specifically, (1) the OFF field effect transistor 12 blocks the  $-V$  potential on the output terminal A from the output capacitor  $X_2$ ; (2) the ON field effect transistor 18 passes

the ground potential on output  $\bar{A}$  to the output capacitor  $X_3$ ; and (3) the OFF field effect transistor 17 inhibits the ground

signal on the output terminal  $\bar{A}$  from reaching output capacitor  $X_4$ .

Therefore, it is seen that, with the field effect transistors 12, 13, 17 and 18 driven by an input signal of "10" a  $-V$  potential indicating a "1" appears across the output capacitor  $X_1$  while a ground potential is impressed across output capacitor  $X_3$ . A  $-V$  potential is not impressed across the output capacitors  $X_2$  and  $X_4$ . Therefore, if one were to sense the output capacitors  $X_1$  to  $X_4$  looking for a  $-V$  potential, one would find the  $-V$  potential only across the output capacitor  $X_1$  provided that capacitors  $X_2$  and  $X_4$  were previously at ground or not storing charge.

It is more convenient in sensing the output conditions of the capacitors  $X_1$  to  $X_4$ , however, to have a potential applied through a relatively low impedance source to each of the output capacitors  $X_1$  to  $X_4$ . Therefore, field effect transistors 14 and 21 have

their gates 34 and 36 connected to the B output terminal of phase splitter 23. First controlled terminals 37 and 38 of the field effect transistors 14 and 21 are connected to the B output terminals of phase splitter 23. The second controlled terminals 39 and 41 of the field effect transistors 14 and 21 are connected to the output capacitors  $X_2$  and  $X_4$ , respectively. In this way, each time the output B exhibits a ground potential, ground return field effect transistors 14 and 21 are turned on by the  $-V$  potential on

output  $\bar{B}$ . The ground potential on output B is therefore passed to output capacitors  $X_2$  and  $X_4$ .

If the signals on input terminals A and B switch from their present condition of "10" to "11" as shown in the second row of the truth table in Fig. 2, the field effect transistors 13 and 18 are turned OFF by the ground potential now appearing on output

terminal  $\bar{B}$  of phase splitter 23 while logic

transistors 12 and 17 are turned ON by the  $-V$  potential appearing on output terminal B. The logic field effect transistor 12 applies the  $-V$  potential still appearing on output terminal A of phase splitter 22 to output capacitor  $X_2$ . It should be noted at this point that the first controlled terminal 24 is now negative with respect to the second controlled terminal of logic field effect transistor 12 while the capacitor  $X_2$  is charging. Logic field effect transistor 17 applies the

ground potential still on output terminal A of phase splitter 22 to output capacitor  $X_4$ . It should be noted that since output capacitor  $X_4$  had a ground potential thereacross, no current flows through logic field effect transistor 17.

The ground return field effect transistors 14 and 21 are now OFF due to the ground

potential on output terminal B of phase splitter 23. The ground return field effect transistors 16 and 19 on the other hand are now in the ON condition due to the  $-V$  potential on output terminal B of phase splitter 23. The ground return field effect transistor 19 merely maintains the potential across capacitor  $X_3$  in its previous ground condition as did logic transistor 17 maintain output capacitor  $X_4$  in its prior condition. Ground return transistor 16 on the other hand, now in its ON condition, discharges capacitor  $X_1$  to the ground supplied

on output terminal B of the phase splitter. It can be seen, therefore, that the output potentials on capacitors  $X_1$  to  $X_4$  are arranged in accordance with the truth table in Fig. 2.

It should be noted, see Fig. 2 that the A output applied to the circuit 10 was a "1" or  $-V$  potential in both of the examples noted above. When the B output switched from "0" to "1", the  $-V$  signal switched from the capacitor  $X_1$  to the capacitor  $X_2$ . It

should be further noted that the A output applied to the circuit 11 was "0" or ground potential in both of the examples cited above. Upon examination of the first two rows of the truth table in Fig. 2, columns  $X_3$  and  $X_4$ , it is seen that the outputs  $X_3$  and  $X_4$  were "0" without regard to the condition of the signal at the B output. Therefore, it can be seen that each of the identical circuits 10 and 11 serve as digital steering devices for the "1" output.

It can be appreciated also that additional circuits similar to 10 and 11 may be combined to convert "N" bit binary coded words, when N is greater than 2, into one-out-of- $2^N$  logic. For example, a one-out-of-eight logic circuit, driven by three binary bits, can be constructed by adding four more

circuits such as circuits 10 and 11. Each one of the added circuits would have its input (in circuits 10 and 11 the inputs are

those leads connected to outputs or A or A of phase splitter 22) connected to a different output lead of circuits 10 and 11 (output leads are those connected to the output capacitors  $X_1$  to  $X_4$ ). The third binary bit and its complement bit would be employed to drive the gates of all the transistors in the four additional circuits in the same way that

outputs B and B of phase splitter 23 drive all the gates of the circuits 10 and 11. Thus, the circuits 10 and 11 would sum the 4 combinations of A and B, as intermediate stages, feeding 8 output FET's to provide one output for each distinctive combination of the three input bits.

In general, to convert an N bit word,  $2^N$  output FETs are provided to similar FETs 12, 13, 17 and 18, as well as as many intermediate stages as are necessary in various possible arrays, such that each output FET turns ON for only one of the  $2^N$  possible combinations of the coded words.

One further point of circuit operation not brought out in the prior discussion is noted when the signals on input terminals A and B switch from their prior condition of "1" "1" to the condition "0" "1". In this case,

since the B and B inputs remain at the same values, all the transistors previously ON remain ON and all the transistors previously OFF remain OFF. The negative voltage previously on transistor  $X_2$  is discharged through logic field effect transistor 12 to ground potential now appearing on output A of phase splitter 22. The first controlled terminal 24 is now positive with respect to the second controlled terminal during the discharging procedure. Therefore it is seen that, while the first controlled terminal 24 served as a drain in the prior example, it serves as a source in this example.

The output capacitor  $X_4$  is charged to  $-V$  potential from output A of phase splitter 22 through logic field effect transistor 17. The ground potential previously on output capacitors  $X_1$  and  $X_3$  remains unchanged. Therefore, from looking at the truth table in Fig. 2 one can see that the outputs  $X_1$  to  $X_4$  again conform thereto.

Although the invention has been described with reference to a particular embodiment, it is to be understood that this embodiment is only illustrative of the application of the principles of the invention. While the code-translating circuits shown herein may be used in the performance of various logic functions, one particular circuit in which they may

advantageously be used is described in U.S. Patent No. 3,618,050.

WHAT WE CLAIM IS:—

1. A logic circuit comprising a first gate  
5 connected to be enabled by a signal of pre-  
determined value on a first conductor to connect an input terminal with a first load  
impedance, a second gate connected to be  
10 enabled by a signal of said predetermined  
value on a second conductor to connect said  
input terminal with a second load impedance,  
a third gate connected to be enabled by a  
15 signal of said predetermined value on said  
second conductor to complete an electric  
path from said first load impedance, and a  
fourth gate connected to be enabled by a  
signal of said predetermined value on said  
20 first conductor to complete an electric path  
from said second load impedance, said first  
and second conductors being energisable such  
that only one of the load impedances will  
receive current from said input terminal  
25 depending on the energisation of the first and  
second conductors.
2. A binary decoding circuit comprising  
first and second logic circuits each according  
to claim 1, each of said first and second logic  
circuits being associated (a) with the same  
30 first and second conductors (b) with a  
different pair of load impedances, and (c)  
with a different one of first and second input  
terminals, said first and second input  
terminals being energisable depending on the  
value of a first binary digit and said ener-  
35 gisation of said second and first conductors  
depending on the value of a second binary

digit, so that a unique one of the load im-  
pedances of the two logic circuits will be  
energised for each combination of said first  
and second binary digit values.

3. A circuit according to Claim 1, or 2,  
wherein each said load impedance comprises  
a respective capacitive means.

4. A circuit according to claim 2, where-  
in said first and second input terminals and  
said first and second conductors comprise  
the outputs of first and second phase split-  
ting circuits respectively, each of said first  
and second phase splitting circuits providing  
complementary energisation of its outputs  
50 according to the value of a bit representative  
signal at its input.

5. A circuit according to claim 1 or  
claim 2, wherein each said gate comprises a  
field effect transistor having a gate electrode  
and two controlled electrodes between which  
the impedance presented is low when a signal  
of said predetermined value is applied to  
the corresponding gate electrode.

6. A logic circuit arranged and adapted  
to operate substantially as herein described,  
with reference to and as shown in block 10  
of Fig. 1 of the drawing.

7. A binary decoding circuit arranged  
and adapted to operate substantially as here-  
in described with reference to and as shown  
in Figs. 1 and 2 of the drawing.

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advantageously be used is described in U.S. Patent No. 3,618,050.

WHAT WE CLAIM IS:—

1. A logic circuit comprising a first gate  
5 connected to be enabled by a signal of predetermined value on a first conductor to connect an input terminal with a first load impedance, a second gate connected to be enabled by a signal of said predetermined  
10 value on a second conductor to connect said input terminal with a second load impedance, a third gate connected to be enabled by a signal of said predetermined value on said second conductor to complete an electric  
15 path from said first load impedance, and a fourth gate connected to be enabled by a signal of said predetermined value on said first conductor to complete an electric path from said second load impedance, said first  
20 and second conductors being energisable such that only one of the load impedances will receive current from said input terminal depending on the energisation of the first and second conductors.
2. A binary decoding circuit comprising  
25 first and second logic circuits each according to claim 1, each of said first and second logic circuits being associated (a) with the same first and second conductors (b) with a different pair of load impedances, and (c)  
30 with a different one of first and second input terminals, said first and second input terminals being energisable depending on the value of a first binary digit and said energisation of said second and first conductors  
35 depending on the value of a second binary

digit, so that a unique one of the load impedances of the two logic circuits will be energised for each combination of said first and second binary digit values.

3. A circuit according to Claim 1, or 2, wherein each said load impedance comprises a respective capacitive means.

4. A circuit according to claim 2, wherein said first and second input terminals and said first and second conductors comprise the outputs of first and second phase splitting circuits respectively, each of said first and second phase splitting circuits providing complementary energisation of its outputs according to the value of a bit representative signal at its input.

5. A circuit according to claim 1 or claim 2, wherein each said gate comprises a field effect transistor having a gate electrode and two controlled electrodes between which the impedance presented is low when a signal of said predetermined value is applied to the corresponding gate electrode.

6. A logic circuit arranged and adapted to operate substantially as herein described, with reference to and as shown in block 10 of Fig. 1 of the drawing.

7. A binary decoding circuit arranged and adapted to operate substantially as herein described with reference to and as shown in Figs. 1 and 2 of the drawing.

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