METHOD AND STRUCTURE TO PREVENT SILICIDE STRAPPING OF SOURCE/DRAIN TO BODY IN SEMICONDUCTOR DEVICES WITH SOURCE/DRAIN STRESSOR

Abstract

The example embodiments disclose devices and methods to prevent silicide strapping of the Source/Drain to Body in semiconductor devices with S/D stressor. We provide isolation regions in the substrate and a gate structure over the substrate. We form recesses in the substrate adjacent to the gate structure with disposable spacers and adjacent to the isolation regions. We provide stressor regions filling the recesses. The stress region can have a pit adjacent the isolation regions. We form stressor spacers at least partially in the pit on the sidewalls of the stressor regions. We form silicide regions over the stressor regions. The spacer on the stressor regions sidewalls inhibit the formation of silicide at the stressor region edge during the silicide process, thus preventing silicide strapping of the Source/Drain to Body.

Figure 6