ABSTRACT

HIGH PERFORMANCE LDMOS DEVICE HAVING ENHANCED DIELECTRIC STRAIN LAYER

An LDMOS device includes a substrate having a surface and a gate electrode overlying the surface and defining a channel region in the substrate below the gate electrode. A drain region is spaced apart from the channel region by an isolation region. The isolation region includes a region of high tensile stress and is configured to induce localized stress in the substrate in close proximity to the drain region. The region of high tensile stress in the isolation region can be formed by high-stress silicon oxide or high-stress silicon nitride. In a preferred embodiment, the isolation region is a shallow trench isolation region formed in the substrate intermediate to the gate electrode and the drain region.

Fig. 1