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(54) "IMPROVEMENTS IN AND RELATING TO INTEGRATED SEMICONDUCTOR DEVICES"

(71) We N.V. PHILIPS' GLOEILAMPENFABRIEKEN, a limited liability Company, organised and established under the laws of the Kingdom of the Netherlands, of Emmasingel 29, Eindhoven, the Netherlands do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to an integrated semiconductor device comprising a semiconductor body having a portion in which a plurality of vertically arranged inversely operable transistors are present together with one or more multi-layer current injector structures for supply of bias currents to said transistors, one of said transistors constituting a driver transistor which is coupled to a transistor having a higher bias current, and to an arrangement comprising such a device.

In the integrated circuit art there are in existence comprehensive articles on I^2L (integrated injection logic), the substance of this technology being that the current supply of the transistors of an integrated circuit is effected *via* one or more multi-layer current injector structures formed at least partly in the semiconductor body of the integrated circuit, the or each current injector structure comprising at least three consecutive layers which are separated from each other by rectifying junctions, among which layers are a first injecting layer serving to inject charge carriers into an adjoining, second intermediate layer and a collecting layer forming the last of said at least three consecutive layers, said collecting layer also forming a zone of one or more transistors of the integrated circuit. For a further description of I^2L circuits reference is invited to U.K. Patent Specification 1,398,862/3/4/5/6/7/8.

Although the notation I^2L could suggest that this invention is concerned exclusively with logic circuits, this is in fact not so, whilst on the contrary the use in analogue circuits should be considered. Hereinafter in this specification I^2L is to be understood to mean the particular variant in which the relevant transistors take the form of vertically arranged inversely operated transistors and the bias currents are fed to the base zones of said transistors.

In I^2L technology the problem arises of providing a coupling between transistors, having current injectors, which are generally set to a very small bias current and low power, and further transistors which would be capable of supplying far more power and which are consequently set to a higher bias current.

According to the invention there is provided an integrated semiconductor device comprising a semiconductor body having a portion in which a plurality of vertically arranged inversely operable transistors are present together with one or more multi-layer current injector structures for the supply of bias currents to said transistors, one of said transistors constituting a driver transistor which is coupled to a transistor operable at a higher bias current via circuit elements comprising a lateral transistor and a vertical transistor together integrated in an island region formed in the semiconductor body and isolated from the remainder of the semiconductor body, said island region being of one conductivity type and means being present for connecting the island region to a fixed potential, first and second separated zones of the opposite conductivity type being present in the island region and together with the separating part of the island region of the one conductivity type forming the lateral transistor, said region of the one conductivity type forming the collector zone of the vertical transistor of which the base zone is formed by said second zone of the opposite conductivity type, the emitter zone of the vertical transistor being formed by a zone of the one conductivity type present within the second zone of the opposite conductivity type, the said emitter zone being connected to the said transistor operable with a higher bias current, means being present for connecting the

lateral transistor first zone of the opposite conductivity type to a supply point for providing a current from said emitter zone which is larger than the injected bias current fed to the said inversely operable vertically arranged transistors.

Such an integrated device may be formed having a compact structure which demands little space and is fully compatible with the fabrication technology for obtaining I^2L circuits.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawing, in which

Figure 1 is a plan view,

Figure 2 is a cross-section of a part of a semiconductor body of an integrated semiconductor device in accordance with the invention.

Figure 3 shows the associated circuit diagram of the part of the device shown in Figures 1 and 2, and

Figure 4 is a circuit diagram of an arrangement including a device which is a modification of the device shown in Figures 1 to 3.

Figure 1 is a plan view of a semiconductor body, of which the section shown in the left of the Figure comprises inversely operated *n-p-n* transistors having current injectors.

The section shown in the right of the Figure comprises a transistor which operates at a higher bias current, whilst between said two sections a coupling section is shown schematically, which couples an output transistor of the left-hand section to the input of the transistor in the right-hand section. The three sections are represented as transistor structures realized in separate islands, but under certain circumstances it is possible to use only two islands, for example if the transistor in the right-hand section is connected as an emitter follower.

As appears from Figure 2 a semiconductor body is used which in this example has a *p*-type silicon substrate 1 and an *n*-type epitaxial layer 4, in which layer islands 4*a* to 4*c* are defined by deep p^+-diffused isolation regions2. In manufacture buried zones 3 of the n+ conductivity type are formed in the substrate 1, after which an epitaxial layer 4 of the *n*-conductivity type is grown. By means of the p+ doped isolation zone the layer 4 is divided into three parts, namely the islands 4*a*, 4*b* and 4*c*. With the aid of further photolithographic processes further *p*-type zones 6, 8 and thereafter *n*-type zones are formed in these three islands, the shape of which is clear from Figures 1 and 2. Thus, transistor structures are obtained in known manner, which in a conventional manner can be connected by means of conductor tracks. These conductor tracks are schematically represented by means of dashed lines in Figures 1 and 2. If desired the transistor structures within the islands 4*a* and 4*b* can be surrounded by a deep n+ doped zone 5, thus preventing the isolation zones 2 from collecting charges in an undesired manner.

One of the transistor structures in the island 4*a* is formed by the *n*-type material of the island 4*a* and the zones 6*a* and 7*a*. This transistor has the form of an inverse vertical transistor, *i.e.* viewed at the top of the semiconductor body the following zones are situated underneath each other; first the collector zone 7a, then the base zone 6a, and then the emitter zone 4a. This transistor 4a, 6a and 7a, which is represented by the symbol *a* in the equivalent diagram of Figure 3, receives its bias current from a so-called current injector. The p-zone 8a functions as an injecting layer which zone is laterally disposed relative to the zone 6a (and other transistor structures having the island material 4a as the common emitter zone). The zone 4a is connected to a point of fixed potential, for example earth, whilst the zone 8a is connected to a point with a supply voltage V_a or for example 1.5 V. As a result charge carriers (holes) from the zone 8a are injected into the zone 4a, which can reach the zone 6a (and also the other p-zones in the vicinity of the injector 8a), so that the zone 6a forming the base of the inverse vertical *n-p-n* transistor is forward-biassed relative to the zone 4a forming the emitter zone. As a result of this the desired transistor action is obtained between the zones 4a (emitter), 6a (base) and 7a (collector).

The bias current of this I^2L transistor is extremely small, which is generally considered a major advantage of the I^2L technology because this also minimizes the power consumption. However, the drawback is then that the power which can be supplied to an external load by such a transistor is also extremely low. Therefore, it is desirable that transistors which operate with a higher bias current can also be incorporated in the same semiconductor body.

Such a transistor is realized in the island 4c in Figures 1 and 2 and is represented by the symbol *c*- in Figure 3. The three zones 4c, 6c and 7c again constitute a vertical transistor but now in normal operation instead of the inverse operation as occurs with the transistor *a*. Therefore the zone 7c then functions as the emitter, the zone 6c as the base, and the zone 4c, whose area is much greater than that of the zone 7c, as the collector of the transistor. The collector-base current gain factor which can be achieved with such a transistor is several times greater than in the case of inverse operation.

In order to couple the output of the transistor *a* which functions as driver transistor, to the input of the transistor *c*, there is provided a coupling element in the form of the structure within the island 4b. This coupling element comprises the current injector 8b, which can inject charge carriers (holes) into the zone 4b for collection by the zone 6b which is laterally situated relative to the injector 8b. This zone 6b constitutes the base zone of a normally operated vertical transistor, of which the said zone 4b functions as the collector and the zone 7b as the emitter. This transistor *b* consequently has a high current gain factor inherent in normal

operation and is thus capable of matching the low current bias of I^2L transistors to the higher current bias which is required for the transistor *c*. The zone 4b is connected to a voltage V_{b2} (for example 4 V) which is preferably slightly higher than the voltage V_a at the injector 8a. This voltage must be supplied by a source of such a low internal resistance, that the structure 8b, 4b, 6b, 7b which, as appears from the equivalent diagram of Figure 3, has the character of a p-n-p-n structure does not become unstable. The voltage V_{b1} at the zone 8b is normally applied *via* some resistance (in a similar way as the voltage V_a at the zone 8a), because otherwise in the case of supply voltage and temperature variation excessive bias current variations might occur. Preferably, the injection currents of the injectors 8a and 8b are selected to be of the same magnitude.

Figure 4 is a schematic representation of a modification in which this current supply is achieved whilst moreover attention has been paid to the use of more current injectors than described in the foregoing. A supply voltage point V, to which for example 12 V is applied, is connected to a conductor 10 *via* a resistor R, which conductor *via* separate resistors R_1 leads to various current injectors (here represented by the symbol of a *p-n-p* transistor), which injectors have the character as described hereinbefore with reference to the zones 8a, 4a, 6a. By means of tappings on the resistor R the voltages V_{b1} and V_{b2} are obtained, the voltage V_{b1} again being applied to the zone 8b in a similar way, whilst the voltage V_{b2} is applied to the zone 4b *via* an emitter follower 12. As appears from the diagram of Figure 4 it is thus achieved in a simple manner that the internal resistance of the voltage source which is thus connected to the zone 4b, is comparatively low, whilst moreover the series resistances in series with the current injectors 8a and 8b remain sufficiently high to ensure low undesired excess currents.

The arrangement shown in Figure 4 may be embodied in the form of an integrated semiconductor device in which the resistor R with the tappings and the three resistors R_1 are formed in the same semiconductor body as the other circuit elements present.

WHAT WE CLAIM IS:

1. An integrated semiconductor device comprising a semiconductor body having a portion in which a plurality of vertically arranged inversely operable transistors are present together with one or more multi-layer current injector structures for the supply of the bias currents to said transistors, one of said transistors constituting a driver transistor which is coupled to a transistor operable at a higher bias current via circuit elements comprising a lateral transistor and a vertical transistor together integrated in an island region formed in the semiconductor body and isolated from the remainder of the semiconductor body, said island region being of one conductivity type and means being present for connecting the island region to a fixed potential, first and second separated zones of the opposite conductivity type being present in the island region and together with the separating part of the island region of the one conductivity type forming the lateral transistor, said region of the one conductivity type forming the collector zone of the vertical transistor of which the base zone is formed by said second zone of the opposite conductivity type, the emitter zone of the vertical transistor being formed by a zone of the one conductivity type present within the second zone of the opposite conductivity type, the said emitter zone being connected to the said transistor operable with a higher bias current, means being present for connecting the lateral transistor first zone of the opposite conductivity type to a supply point for providing a current from said emitter zone which is larger than the injected bias current fed to the said inversely operable vertically arranged transistors.

2. An arrangement including an integrated semiconductor device as claimed in Claim 1, wherein a resistor is present being a supply point and for supply of bias current to the said vertically arranged inversely operable transistors, said resistor comprising a tapping which is connected to the said electrically isolated island via an emitter-follower for supplying said fixed potential.

3. An integrated semiconductor device substantially as herein described with reference to Figures 1 to 3 of the accompanying drawing.

4. An arrangement substantially as herein described with reference to Figure 4 of the accompanying drawing.

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2. An arrangement including an integrated semiconductor device as claimed in Claim 1, wherein a resistor is present being a supply point and for supply of bias current to the said vertically arranged inversely operable transistors, said resistor comprising a tapping which is connected to the said electrically isolated island via an emitter-follower for supplying said fixed potential.

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