METHODS OF FORMING FULLY EMBEDDED BUMPLESS BUILD-UP LAYER PACKAGES AND STRUCTURES FORMED THEREBY

BACK GROUND OF THE INVENTION

As semiconductor technology advances for higher processor performance, advances in packaging architectures may include coreless bumpless build-up Layer (BBUL-C) package architectures and other such assemblies. Current process flows for BBUL-C packages involve building of the substrate on a temporary core/carrier capped with copper foil, which is etched off after the package is separated from the core.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming certain embodiments of the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. 1a-1g represent methods of forming structures according to an embodiment of the present invention.

FIGS. 2a-2j represent methods of forming structures according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the methods may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the embodiments. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the embodiments. In addition, it is

to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the embodiments. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the embodiments is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

Methods and associated structures of forming and utilizing microelectronic packaging structures, such as fully embedded coreless BBUL package structures, are described. Those methods may include forming a die embedded in a coreless substrate, wherein a mold compound surrounds the die, and wherein the die comprises TSV connections on a first side and C4 pads on a second side of the die, wherein a dielectric material is disposed on a first side and on a second side of the mold compound, and wherein interconnect structures are coupled to the C4 pads and to the TSV pads through the dielectric material on both sides of the die. Methods of the embodiments enable the formation of dual sided, fully embedded packages using bumpless build-up layer (BBUL) technology.

Methods and associated structures of the embodiments further include forming a first die embedded in a coreless substrate, a first dielectric material adjacent the first die, and a second die embedded in the coreless substrate, wherein the second die is disposed above the first die and a second dielectric material is adjacent the second die. Interconnect structures further connect the first die to solder connections on an outer portion of the coreless substrate, wherein the coreless substrate does not comprise PoP (package on package) lands to couple the second die to the coreless package. The methods of the embodiments further enable the formation of a package structure wherein the overall package is made completely by the BBUL process rather than by a hybrid process involving a BBUL package process and a BGA/wire bond packaging process.

FIGS. 1a-1g illustrate embodiments of methods of forming microelectronic structures, such as package structures, for example. FIG. 1a illustrates a carrier material 100. In one

embodiment, the carrier material 100 may comprise a multi-layer copper foil that may serve as a temporary carrier, such as a microelectronic die carrier 100. In other embodiments, the carrier material 100 may comprise any suitable conductive carrier material 100. In an embodiment, the carrier material 100 may optionally comprise an adhesive layer 102.

In an embodiment, a die 106 may be placed on the carrier material 100, which may in an embodiment comprise a temporary die carrier 100. The die 106 may comprise controlled collapse chip connections (C4) pads 104 and though silicon via (TSV) pads 105. In an embodiment, the C4 pads may be disposed on a first side 103 of the die 106, and the TSV pads may be disposed on a second side 101 of the die 106. The die 106 may be placed C4 side up, or in other embodiments may be placed TSV pad 105 side up on the die carrier 100. In an embodiment, the adhesive 102 can be dispensed either on the die 106 or on the carrier 100. In some cases, the 102 adhesive film and/or an attach process may be used to attach the die 106 to the temporary carrier 100.

In an embodiment, a mold compound 108 may be applied to surround/embed the die 106 (FIG 1b). In an embodiment, the mold compound 108 may be dispensed and cured to over-mold the die 106. The mold compound 108 may be applied such that the die 106 is completely embedded in the mold compound 108. A portion of the mold compound 108 may then be removed to expose the C4 pads 104 and TSV 105 pads (FIG. 1c). In an embodiment, back-grinding of the mold compound 108 may be performed to expose the C4 pads 104 and TSV pads 105, and the temporary carrier 100 may be removed from the die 106 during back-grinding removal process. In an embodiment, the die 106 may remain entirely embedded in the mold compound 108 after exposure of the C4 and TSV pads 104,105. The mold compound 108 may serve as a base for subsequently formed build-up layers of a microelectronic package structure formed according to embodiments herein, and may further serve to reduce warpage during subsequent processing of such a package structure. The remaining mold compound 108 may comprise a first surface 107 and a second surface 109.

Dielectric material 110, 110' may be formed on the first surface 107 and on the second surface 109 of the mold compound 108 that surrounds the die 106 (FIG. 1d). In an embodiment, the dielectric material 110, 110' may be formed/attached by a laminating process, for example. The dielectric material 110, 110' may provide a level plane for a subsequent build-up process.

In an embodiment, vias 112 may be formed in the dielectric material 110 on the first surface 107 of the molding compound 108, to connect to the C4 pads 104 of the die 106, and vias 112' may also be formed in the dielectric material 110' on the second surface 109 of the molding compound 108 to connect to the TSV pads 105 of the die 106. The vias 112, 112' may subsequently be filled with conductive material 113 (FIG. 1e). In an embodiment, a semi-additive process (SAP) may be used to form interconnect structures 114 (which may comprise first metal layers, for example) to connectively couple to the C4 pads 104 on the die 106, and interconnect structures 114' may also be formed to connectively couple to the TSV pads 105 of the die 106. In an embodiment, the interconnect structures 114 may be disposed on the first surface 107 of the molding compound 108 and may be connected to the C4 pads 104 by the conductive vias 113. The interconnect structures 114' may be disposed on the second surface 109 of the molding compound 108 and may be connected to the TSV pads 105 by the conductive vias 113'.

Subsequent layers may then be formed using SAP build-up processing, for example, wherein further dielectric layers, such as dielectric layers 110'', 110''', conductive vias 113'', 113''' and interconnect structures 114'', 114''' may be formed upon each other according to the particular design requirements, to form a coreless package structure 120 by utilizing the buildup process (FIG. 1f). In an embodiment, the coreless package structure 120 may comprise a BBUL coreless package structure 120, and the die 106 may be fully embedded in the coreless package structure 120.

In an embodiment, the coreless package structure 120 may comprise a dual-sided package 120 on both sides of the die 106, which is embedded in mold compound 108.

In an embodiment solder resist 116, 116' may be used to form openings 118, 118' to connectively couple to the C4 and/or the TSV pads 104, 105 on the outermost layer of the package structure 120. In an embodiment, solder resist can be used to open up the pads on the outermost layer of the package structure 120. In an embodiment, solder balls 122 may be formed in the openings 118' (and/or 118) to couple to the die 106. (FIG.1g). In an embodiment, the solder balls 122 may comprise ball gird array (BGA) balls 122, that may be attached to the package structure 120. In an embodiment, a additional dies and/or packages 124 may be attached/coupled through the openings 118 (and/or 118', referring back to FIG, 1g) to an outer portion of the coreless package structure 120. In another embodiment, through mold-vias (not shown) may be formed through the dielectric layers to increase power supply to the coreless package structure 120, for example.

Thus, methods of fabricating dual sided fully embedded package structures using BBUL technology are enabled. The coreless package structure 120 may be utilized in stacked die/package applications. Embodiments provide stiffer package structures owing to the presence of the mold compound, and enable a fully embedded die solution, thus reducing the package Z-height. The embodiments further facilitate the integration of TSVs for stacked package applications, while improving warpage, while providing for simultaneous processing of a base package and stacked package(s). The embodiments enable packaging, assembly, and/or test solutions for graphics, wireless CPU's/processors, Chipsets Multi-Chip/3D package structures/systems, including CPU's in combination with other devices such as Memory (e.g., flash/DRAM/SRAM/etc) and boards such as motherboards, for example.

FIGS. 2a-2j illustrate embodiments of methods of forming microelectronic structures, such as BBUL package structures, for example. FIG. 2a illustrates a carrier material 200. In one embodiment, the carrier material 200 may comprise a multi-layer copper foil that may serve as a carrier, such as a microelectronic die carrier. In other embodiments, the carrier material 200 may comprise any suitable conductive carrier material 200. In an embodiment, the carrier material

200 may comprise an adhesive layer 202, such as a die back side film (DBF) that may be pre-attached to a first side 201 of the carrier 200 and a second side of the carrier 203.

A first die 206, such as a first memory die 206 for example, may be mounted/attached on the first side 201 of the carrier 200 using the pre-attached DBF 202, for example. A second die, such as a second memory die 206', may be attached on the second side 203 of the carrier 200 using the pre-attached DBF 202, for example. The first and second die 206, 206' may comprise conductive structures 204, 204', respectively which may comprise C4 interconnect structures 204, 204', for example. A dielectric material 210 may be placed/laminated on the first side 201 of the carrier 200 (FIG. 2b). A dielectric material 210' may be placed/laminated on the second side of the carrier 203 such that the first die 206 and the second die 206' are fully embedded within the dielectric materials 210, 210' respectively. In an embodiment, the first memory die 206 may serve to be the first embedded die 206 in a BBUL process.

Vias 212, 212' may be formed through the dielectric material 210, 210', by UV/CO2 laser, for example, to expose the conductive structures 204, 204' on the die 206, 206' respectively (FIG. 2c).

The vias 212, 212' may subsequently be filled with conductive material 213, 213' (FIG. 2d). In an embodiment, a semi-additive process (SAP) may be used to form interconnect structures 214 (which may comprise a first metal layer, for example) to connectively couple to the C4 pads 204 on the first die 206. Interconnect structures 214' may also be formed to connectively couple to the C4 pads 204' of the second die 206'. In an embodiment, the interconnect structures 214 may be disposed on/over the dielectric material 210 and on/over the first die 206, and may be coupled to the C4 pads 204 by the conductive vias 213. The interconnect structures 214' may be disposed on/over the dielectric material 210' and on/over the second die 206', and may be connected to the C4 pads 204' by the conductive vias 213'.

Subsequent layers may then be formed using a SAP build-up processing, for example, wherein further dielectric material 210'', 210''', conductive vias 213'', 213''' and interconnect

structures 214'', 214''' may be formed upon each other according to the design requirements of the particular application, by utilizing a SAP buildup process (FIG. 2e). In an embodiment, a third die 216, such as a CPU die 216 may be mounted/attached above the first die 206, on/above the first surface 201 of the carrier 200. A fourth die 216', which may comprise a CPU die, for example, may be attached/mounted above the second die 206' (FIG. 2f). Additional dielectric material 211, 211' may be formed surrounding the third die 216, and the fourth die 216' respectively. Subsequent layers may then be formed using SAP build-up processing, for example, wherein additional conductive vias 213'', 213''' and interconnect structures 214', 214''' may be formed upon each other according to the particular design requirements (FIG. 2g). In an embodiment, further vias and metallization layers may be formed on the third and fourth dies 216, 216', according to the particular application, wherein greater than two levels of metallization may be formed utilizing the SAP build-up process.

In an embodiment, solder resist 216, 216' can be used/patterned on/above the third and fourth die 216, 216' to open up pads 215, 215' (FIG. 2h). In an embodiment, the first die 206 and the third die 216 may be separated from the second die 206' and the fourth die 216' along the temporary carrier 200 to form a first package structure 220 and a second package structure 220'. In an embodiment, the first and third die 206, 216 may comprise a first BBUL package structure 220 without package on package (PoP) lands after separation from the carrier 200. In an embodiment, the second and fourth die 206', 216' may comprise another, second BBUL package 220' without PoP lands after separation from the carrier 200.

In an embodiment, solder balls 222 may be formed on the pads 215 to couple to the die 206, 216 of the first package 220 (FIG. 2i). Solder balls 222' may be formed on the pads 215' to couple to the die 206', 216' on the second package (not shown). In an embodiment, the solder balls 222 may comprise ball gird array (BGA) balls 222 that may be attached to the package structure 220. Thus, the BBUL package structure 220, wherein there are no PoP lands, may comprise a BBUL coreless package structure 220, and the first and second die 206, 206' may be

fully embedded in the coreless BBUL package structure 220.

In an embodiment, additional die, such as a fifth 221 and a sixth die 221', for example, may be formed adjacent to the first die 206 in the first package 220 and the third die 206' in the second package 220' (not shown) respectively (FIG. 2j, depicting first package 220). In an embodiment, the fifth die 221 may be disposed in the dielectric material 210 on the first side of the carrier 200 and the sixth die 221' may be disposed in the dielectric material 210' on the second side of the carrier 200 of the second package 220' (not shown).

Thus, embodiments included herein comprise BBUL processes and structures wherein multiple dies are fully embedded within the BBUL package. In an embodiment, the top die, such as a top memory die, may be the first embedded die in the BBUL process of the embodiments herein. Benefits of the embodiments herein include overall cost of processing reduction of the final package, due to the removal of the PoP substrate and a CAM step (such as a memory die attach to PoP package, for example). The overall Z height of the final 'pure', non-PoP land comprising BBUL package may be reduced. PoP package solder joint reliability issues (which may be due to lack of anchoring of the copper PoP pad), may be eliminated. Furthermore, with the embedded stacked die, the BBUL package structures of the various embodiments herein reduce warpage, thus improving the yield during surface mount to a motherboard. The overall package of the various embodiments herein are made completely by the BBUL process alone, rather than by a hybrid process comprising a combination of BBUL package processing and BGA/wire bond package processing as in prior art processes/structures.

Prior art BBUL packages may in fact comprise a combination of a BBUL package and a PoP package, wherein the PoP package is surface mounted onto the BBUL. That is, only the lower package in the prior art is a BBUL process/package and the top PoP package is a non-BBUL package, the top die in the PoP portion not being fully embedded in the BBUL package. The embodiments herein eliminate the PoP package completely. The various embodiments enable packaging, assembly, and/or test solutions for CPU's/processors, chipsets multi-chip/3D

packages including CPU in combination with other devices, memory (e.g., flash, DRAM/, RAM/etc.), boards (e.g., motherboards, etc.).

Although the foregoing description has specified certain steps and materials that may be used in the method of the present invention, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims. In addition, it is appreciated that various microelectronic structures, such as package structures, are well known in the art. Therefore, the Figures provided herein illustrate only portions of an exemplary microelectronic device that pertains to the practice of the present invention. Thus the present invention is not limited to the structures described herein.

IN THE CLAIMS

What is claimed is:

1. A method comprising;

attaching a first die to a first side of a carrier;

attaching a second die to a second side of the carrier;

forming dielectric material on the first side of the carrier and forming dielectric material on the second side of the carrier;

forming via connections and interconnect structures through the dielectric material on the first side of the carrier to connect to the first die and forming via connections and interconnect structures through the dielectric material on the second side to connect to the second die;

attaching a third die on the dielectric material on the first side of the carrier and attaching a fourth die on the dielectric material on the second side of the carrier;

forming additional dielectric material and interconnect structures on the third die and forming additional dielectric material and interconnect structures on the fourth die; and

separating the first and third die from the second and fourth die along the carrier to form two separate package structures.

2. The method of claim 1 further comprising wherein the first and third die are fully embedded in a first package, and wherein the second and fourth die are fully embedded in a second package

3. The method of claim 2 further comprising wherein the first and second packages

do not comprise a PoP lands.

4. The method of claim 1 further comprising wherein the first and second die comprise a memory die.

5. The method of claim 1 further comprising wherein the first and second die comprise a CPU die.

6. The method of claim 4 further comprising attaching a fifth die adjacent the third die on the dielectric material on the first side of the carrier and attaching a sixth die adjacent the fourth die on the dielectric material on the second side of the carrier.

7. The method of claim 1 further comprising wherein the carrier material comprises copper.

8. The method of claim 1 further comprising wherein each of the two packages comprise coreless, bumpless, build up layer packages.

9. A method of forming a package structure comprising;

attaching a die to a carrier material;

forming a mold compound over the die;

removing a portion of the mold to expose pads on a first side and on a second side of the die;

forming dielectric material on first and second surfaces of the mold compound;

forming a coreless substrate by building up layers on the dielectric

material disposed on the first and second surfaces of the mold compound.

10. The method of claim 9 further comprising:

forming vias and interconnects to connect to the pads on the first and second sides of the die.

11. The method of claim 9 further comprising wherein the structure comprises a dual sided package, wherein the die is fully embedded in the dual sided package.

12. The method of claim 9 wherein the structure comprises a portion of a coreless, bumpless, build up layer package, and wherein a second die is attached to the package.

13. The method of claim 10 further comprising wherein the die comprises TSV pads on a first side and C4 pads on a second side of the die.

14. A structure comprising:

a die embedded in a coreless substrate, wherein a mold compound surrounds the die, and wherein the die comprises TSV connections on a first side and C4 pads on a second side of the die;

a dielectric material on a first side and on a second side of the mold compound; and

interconnect structures coupled to the C4 pads and to the TSV pads.

15. The structure of claim 14 wherein the structure comprises a dual sided package, wherein the die is fully embedded in the dual sided package.

16. The structure of claim 14 wherein the structure comprises a portion of a coreless, bumpless, build up layer package.

17. The structure of claim 16 wherein at least one of a second die and a second package is attached to an outer portion of the package.

18. The structure of claim 14 wherein solder interconnect structures are coupled to the die on an outer portion of the package.

19. A structure comprising:

a first die embedded in a coreless substrate;

a first dielectric material adjacent the first die;

a second die embedded in the coreless substrate, wherein the second die is disposed above the first die;

a second dielectric material adjacent the second die;

interconnect structures connecting the first die to solder connections on an outer portion of the coreless substrate, wherein the coreless substrate does not comprise PoP lands to connect the second die to the coreless package.

20. The structure of claim 19 wherein the first and second die are fully embedded in the coreless package.

21. The structure of claim 19 wherein the coreless substrate comprises a portion of a coreless bumpless buildup package structure.

22. The structure of claim 19 wherein the first die comprises a memory die.

23. The structure of claim 19 wherein the second die comprises a CPU die.

24. The structure of claim 19 wherein at least one additional die is disposed above the first die, adjacent to the second die, wherein the at least one additional die is not attached to the package with PoP lands and is fully embedded in the package.