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ABSTRACT

A scaleable integrated data processing device comprises a processing unit with one or more processors and a storage unit with one or more memories provided respectively in one or more processor layers (P), memory layers (M) or combined processors/memory layers (MP) which form main layers in the device. Each main layer comprises electrical conducting structures which form internal electrical connections in three dimensions in the layer. The data processing device also comprises a carrier substrate.

Each main layer (P,M,MP) is formed of a number of sublayers, which each comprises respectively dielectric, semiconducting and electrical conducting portions which are provided such that they form integrated active and passive circuit elements which are included in the processors and the memories, the circuit elements, the processors and the memories being mutually connected by the electrical conducting structures in each main layer. Further electrical conducting structures are provided in the data processing device in order to interconnect the main layers mutually and/or the main layers with the substrate or in order to create a connection to the exterior of the data processing device.

The integrated data processing device has a scalable architecture such that it in principle can be configured with almost unlimited processor and memory capacity. Particularly can the data processing device implement various forms of scalable parallel architectures integrated with optimal interconnectivity in three dimensions.

(Fig. 6)



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