

A NON-VOLATILE MEMORY CIRCUIT

This invention relates to non-volatile memory circuits, for example, for electronic watches.

According to the present invention there is provided a non-volatile memory circuit comprising: at least one
5 memory element; a voltage limiting element disposed between a data terminal to which a relatively high voltage signal is applied to write data into the memory element or elements and a power source terminal; and a current limiting element disposed between the data terminal and the memory element or elements.

10 In one embodiment the voltage limiting element is a capacitor. The current limiting element may be a resistor and inductance connected in series.

In another embodiment the voltage limiting element consists of a diode and a capacitor connected in parallel.

15 The current limiting element may be a relatively high resistance MOS transistor with drain and source connected.

In another embodiment the memory circuit includes a time-constant circuit for blocking or attenuating the signal applied to the data terminal unless it persists for a predetermined time.

Thus an inverter may control the current limiting element in dependence upon the output of the time constant circuit.

Preferably there are two voltage limiting elements connected in parallel and two current limiting elements connected in series.

5 The or each memory element may be an EEPROM element.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a circuit diagram of part of a conventional memory circuit;

10 Figure 2 is a block diagram of a non-volatile memory circuit according to the present invention; and

Figures 3 to 9 are circuit diagrams of embodiments of non-volatile memory circuits according to the present invention.

Figure 1 shows a conventional memory circuit for writing
15 data in an EPROM using FAMOS (Floating-Gate Avalanche Injection MOS) elements assembled into an integrated circuit for an electronic watch. Terminals A,B are preset either to a relatively high voltage V_{DD} or a relatively low voltage V_{SS} . When a negative high voltage is applied to a terminal V_{pp} , electrons are injected
20 into FAMOS elements 103,104 each of which is preset to a low condition and each of which is connected in series with a respective transistor 101,102. As the electrons injected into the FAMOS elements are maintained semi-permanently, the FAMOS elements act as a semiconductor memory into which data may be written.

25 However, when incorporating the circuit shown in Figure 1

into an integrated circuit for an electronic watch, there is the problem that electrons may be injected into the FAMOS elements by accident due to external noise or static electricity. This is because the drains of the FAMOS elements are connected with each other and the drains are themselves connected to a terminal pad which is also used as the terminal V_{pp} to which the high voltage for writing is applied.

Figure 2 is a block diagram of a non-volatile memory circuit according to the present invention. Two non-volatile memory elements 201,202 are arranged on the same substrate. Voltage limiting elements 203,204 limit the voltage applied to the non-volatile memory elements 203,204 when a high voltage which is greater than that required for writing or erasing is applied to a terminal V_{pp} . The above voltage limiting elements are disposed in parallel with a terminal to which the voltage V_{DD} or the voltage V_{SS} is applied and the terminal V_{pp} . Each voltage limiting element may be a transistor, diode or capacitor. Current limiting elements 205,206 are provided for limiting the current applied to the non-volatile memory elements. The current limiting elements 205,206 are disposed in series between the terminal V_{pp} and the non-volatile memory elements. Each current limiting element may be a transistor, diode or capacitor. By providing a voltage limiting element and a current limiting element erroneous writing and erasing of data is avoided.

Figure 3 is a circuit diagram of one embodiment of a non-volatile memory circuit according to the present invention. DC

resistors 305,306 formed in a P^- well and parasitic inductances 307,308 formed in aluminium wiring are used as current limiting elements. Further, capacitors 309,310 formed in $P^+ - N^-$ regions are used as voltage limiting elements. The resistors 305,306, inductances 307,308 and capacitors 309,310 form a low pass filter to remove or attenuate the high frequency component of external noise, static electricity, etc. When writing data into the non-volatile memory circuit a high voltage is applied to the terminal V_{pp} for a longer time than that in a non-volatile memory circuit having no low pass filter because of its time constant. However, this is only several milliseconds and so does not create any significant problem.

A low pass filter may be constructed by a resistor and capacitor or an inductance and capacitor. However, one pair of components in this embodiment is not sufficient to eliminate or attenuate the high frequency component of external noise, static electricity, etc. Thus in Figure 3, the resistors, inductances and capacitors are duplicated to form the low pass filter. The capacitors 309,310 are in parallel and the resistor 305 and inductance 307 are in series with the resistor 306 and the inductance 308. However, this low pass filter increases the voltage drop across the resistors 305,306 so that it is desirable to design the low pass filter taking into consideration the voltage needed for writing data and the frequency spectrum of external noise. In Figure 3 there is shown two memory elements one of which consists of a P-channel

transistor 301 and a FAMOS element 303 and the other of which consists of a P-channel transistor 302 and FAMOS element 304.

Figure 4 is a circuit diagram of another embodiment of a non-volatile memory circuit according to the present invention.

5 In Figure 4, a voltage limiting element is constructed by a $P^+ - N^-$ diode 405 and $P^+ - N^-$ capacitors 406, 407, 408. High resistance MOS transistors 409, 410 which can endure a relatively high voltage are used as current limiting elements. Ordinarily, a diode is formed parasitically on an integrated circuit. However, in this
10 embodiment the diode 405 is formed by controlling concentration of an N^- region so that it has a relatively low break-down voltage which is controlled to be within the normal voltage range for writing data that is approximately -15V. In the event of external noise having a comparatively high DC component the peak level
15 thereof is limited by the diode 405 to about 15V. The voltage applied thereafter is within the normal voltage range for writing data so that charge is not applied to the gates of FAMOS elements 403, 404 without respective P-channel transistors 401, 402 being switched ON. A relatively high break-down voltage transistor
20 together with a capacitor may be used as a low pass filter in place of the diode 405 and the capacitor 406.

Figure 5 is a circuit diagram of another embodiment of a non-volatile memory circuit according to the present invention. There are two basic differences between the embodiment of Figure
25 5 and the embodiments of Figures 3 and 4. One is that P-channel

and N-channel MOS transistors are used as limiting elements and the other is that a time-constant circuit is constituted by a capacitor 506 and a resistor 507. In Figure 5 a diode 505 is used as a voltage limiting element. The diode 505 is produced and operates in the same manner as the diode 405 of Figure 4. An N-channel transistor 509 and a P-channel transistor 510 are used as current limiting elements. When writing data, a voltage of approximately -15V is applied to the terminal V_{pp} . The gate voltage of an inverter 508 reduces from the voltage V_{DD} (= 0V) in the negative direction at a rate determined by the time constant of the time-constant circuit. When its gate voltage is greater than the threshold voltage of the inverter, the P-channel transistor 510 and the N-channel transistor 509 are switched on. The voltage applied to the terminal V_{pp} is transferred to FAMOS elements 503,504. Thereby, electric charge is injected into the FAMOS elements 503,504 selected by the voltage applied to a terminal A or terminal B via a respective transistor 501,502.

The following is a description of the case of the application of a pulse to the non-volatile memory circuit of Figure 5. A pulse of relatively high voltage and relatively narrow width is similar to static electrical noise. When the time constant of the time-constant circuit is large, the voltage at a point X is less than the threshold voltage of the inverter 508 and is close to the voltage V_{DD} . Accordingly, the P-channel transistor 509 and the N-channel transistor 510 are not switched ON and the

pulse (static electrical noise) applied to the terminal V_{pp} is attenuated. Thus a voltage applied to the terminal V_{pp} is not transferred to the FAMOS elements 503,504 unless it persists for a given period.

5 Figure 6 is a circuit diagram of an embodiment of a non-volatile memory circuit according to the present invention where the protective circuit of Figure 5 is applied to an EEPROM element. In Figure 6 transistors 601,602 are selection transistors and transistors 603,604 are memory transistors having a two-layer gate
10 construction. Data is written or erased as follows. When writing data into the transistor 603, a terminal A_1 is preset to the voltage V_{DD} and a terminal A_2 is preset to the voltage V_{SS} so that the transistor 601 is switched on and a voltage of +21V is applied to the gate of the transistor 603. Thereby, the upper
15 gate and drain of the transistor 603 become respectively +21V and V_{SS} so that electrons are stored in the floating gate by the tunnel effect and the threshold voltage increases. On the other hand, when erasing data from the transistor 603, the terminal
20 A_1 is preset to the voltage V_{DD} and the terminal A_2 to 21V so that the voltage V_{SS} and a voltage of 21V are applied respectively to the gate and the drain of the transistor 603. As a result, electrons are erased. Thus for erasing the applied voltage is of opposite polarity to that for writing. In the transistor 603,604, the thickness of the film between the floating gate and the drain
25 is partially thin, so that the tunnel effect is easily achieved.

In an EEPROM element of this construction when writing or erasing data, no DC circuit is produced between the high voltage terminals (V_{DD} (+21V) and V_{SS}). Thus it is possible to write or erase data with relatively little energy consumption.

5 Such an EEPROM element, however, is sensitive to external noise and static electricity which without a protection circuit would cause soft errors such as mis-writing or mis-erasing.

A P-channel transistor 605 is used as a voltage limiting element and P-channel and N-channel transistors 609,610 are
10 used as current limiting elements. The protective circuit shown in Figure 6 operates in the same manner as that of Figure 5. Namely, when writing data, a voltage of +21V is applied to the terminal V_{pp} and when erasing data 0V is applied thereto. There is a predetermined delay determined by a time constant circuit
15 consisting of a capacitor 606 and a resistor 607 before transistors 609,610 are switched ON. A pulse whose width is less than the time constant of the resistor 607 and the capacitor 606 can not be transferred to the gate of the transistor 603 or the transistor 604 because the transistors 609,610 are not switched
20 ON by an inverter 608 such as the inverter 508 of Figure 5.

Figure 7 is a circuit diagram of a further embodiment of a non-volatile memory circuit according to the present invention. In this embodiment, the break-down voltage of the drain of a transistor 1305 is used as a voltage limiting element. Generally,
25 in an enhancement type MOS transistor, when connecting the gate

electrode with the source electrode, a channel is not formed and so current does not flow. However, when a high voltage applied to the drain reaches a certain level, current suddenly begins to flow. The voltage at which current suddenly begins to flow, i.e. the break-down voltage is preset to be slightly higher than the voltage for writing data in FAMOS elements 1303,1304. It is, therefore, possible to write required data certainly and to protect the data from the effects of external noise and static electricity. Further, a transistor 1306 whose gate and drains are connected, is used as a current limiting element. The transistor 1306 is constructed as a diode acting in a direction opposite to flow of current from a terminal to which the voltage V_{DD} is applied. The break-down of the transistor 1306 is such as to limit any external high voltage.

In this embodiment, both voltage and current are limited in order to reduce any externally applied high voltage. The only components additional to memory elements consisting of the FAMOS elements 1303,1304 and P-channel transistors 1301,1302 are the two transistors 1305,1306 which greatly improve the reliability of the non-volatile memory circuit and writing in the FAMOS elements.

Figure 8 is a circuit diagram of yet another embodiment of a non-volatile memory circuit according to the present invention. Diodes 1405,1406 are formed by controlled P-type and N-type doping of a $P^+ - N^+$ junctions. The break-down voltage of these diodes is

slightly higher than the voltage required for writing. Resistors 1407,1408 formed as a P-well limit sharp punch through current, i.e. are current limiting elements. Also in this embodiment there are two protective circuits one, the diodes 1405,1406, for limiting voltage and the other, the resistors 1407,1408, for limiting current. However, P-well doping in this embodiment is less than that in the Figure 3 embodiment and so break-down voltage is higher. Therefore, this embodiment is more acceptable to external noise than the embodiment of Figure 3.

Figure 9 is a circuit diagram of a non-volatile memory circuit incorporating EEPROM elements. Transistors 1501,1502 select respective FAMOS elements 1503,1504 which have a double-layer gate construction. For example, in the case of writing data, first a terminal A_1 is preset to voltage V_{DD} and a terminal A_2 is preset to voltage V_{SS} and the transistor 1501 is switched on. Then a voltage of approximately +21V is applied to the terminal V_{PP} . In the case of erasing data, first the terminal A_1 is preset to the voltage V_{DD} and the terminal A_2 is preset to the voltage +21V and in consequence a voltage of +21V is applied to the drain of the FAMOS element 1503 and the voltage V_{SS} is applied to the gate thereof. In other words for erasing data voltages of opposite polarity to those of the writing data are required. The FAMOS elements 1503,1504 have a construction where only a gate layer formed between a floating gate and the drain is of reduced thickness and so electrons are stored and discharged by the polarity of the

voltage applied to the portion between the gate and the drain.

In an EEPROM element constructed on the above principle, when writing or erasing data, no DC current is produced between the high voltage terminal V_{pp} and the terminal to which the voltage V_{SS} is applied, and it is possible to write or erase data with relatively little energy consumption. Therefore, such EEPROM elements are sensitive to external noise and this causes data to be erroneously written or data mistakingly erased. This embodiment, as shown in Figure 9, utilises transistors 1505, 1506, 1507, the transistor 1505 utilising break-down voltage of an N-channel transistor to act as a voltage limiting element. The transistors 1506, 1507 act as current limiting elements.

As shown in Figures 3 to 9, resistors, diodes, transistors, capacitors, etc. are provided as voltage limiting elements and resistors, transistors, inductances, etc. are provided as current limiting elements. Mis-writing due to external noise or static electricity generated from the human body can be prevented by providing at least one voltage limiting element and one current limiting element. Further, in a non-volatile memory circuit for writing and for erasing data in EEPROM elements, as shown in Figures 6 or 9, it is possible to prevent erroneous writing and erasing due to noise or static electricity. Furthermore, the area of a memory chip incorporating the present invention is almost the same as a conventional memory chip because there is not much difference between the size of ordinary transistors

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and that of transistors used as voltage limiting elements and current limiting elements in a non-volatile memory circuit according to the present invention. The channel width of a transistor used as a voltage limiting element or a current limiting element in
5 a non-volatile memory circuit according to the present invention may be $50\mu\text{m}$ ($W = 50\mu\text{m}$) and the channel length may be $4\mu\text{m}$ ($L = 4\mu\text{m}$). In a non-volatile memory circuit according to the present invention, voltage may be dropped by 2 to 3 volts by the current limiting element. It is possible to assemble such a non-volatile memory
10 circuit in an electronic watch without any great difficulty.

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CLAIMS

1. A non-volatile memory circuit comprising: at least one memory element; a voltage limiting element disposed between a data terminal to which a relatively high voltage signal is applied to write data into the memory element or elements and a power source terminal;
5 and a current limiting element disposed between the data terminal and the memory element or elements.
2. A memory circuit as claimed in claim 1 in which the voltage limiting element is a capacitor.
3. A memory circuit as claimed in claim 1 or 2 in which the
10 current limiting element is a resistor and inductance connected in series.
4. A memory circuit as claimed in claim 1 in which the voltage limiting element consists of a diode and a capacitor connected in parallel.
- 15 5. A memory circuit as claimed in claim 1 or 4 in which the current limiting element is a relatively high resistance MOS transistor with drain and source connected.
6. A memory circuit as claimed in claim 1 including a time-constant circuit for blocking or attenuating the signal applied
20 to the data terminal unless it persists for a predetermined time.
7. A memory circuit as claimed in claim 6 in which an inverter controls the current limiting element in dependence upon the output of the time constant circuit.



8. A memory circuit as claimed in any preceding claim in which there are two voltage limiting elements connected in parallel and two current limiting elements connected in series.
9. A memory circuit as claimed in any preceding claim in which
- 5 the or each memory element is an EEPROM element.
10. A non-volatile memory circuit substantially as herein described with reference to any one of Figures 2 to 9 of the accompanying drawings.
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