



(51) International Patent Classification:
H01L 21/203 (2006.01) *H01L 21/02* (2006.01)
H01L 21/205 (2006.01)

(21) International Application Number:
PCT/US2011/029589

(22) International Filing Date:
23 March 2011 (23.03.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/318,693 29 March 2010 (29.03.2010) US

(71) Applicants (for all designated States except US): **S.O.I. TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Chemin Des Franques, Parc Technologique Des Fontaines, F-38190 Bernin (FR). **ARIZONA BOARD OF REGENTS FOR AND on behalf of ARIZONA STATE UNIVERSITY** [US/US]; 1475 North Scottsdale Road, Suite 200, Scottsdale, AZ 85257 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **LINDOW, Ed** [US/US]; 11740 North 93rd Place, Scottsdale, AZ 85260 (US). **ARENA, Chantal** [US/US]; 3847 E. Ivyglen Circle, Mesa, AZ 82505 (US). **BERTRAM, Ronald** [US/US]; 15508 South Moutain Road, Mesa, AZ 85212 (US). **DATTA, Ranjan** [IN/IN]; B-711, Sobha Windfall, Amruthahalli, Bangalore 560091 (IN). **MAHAJAN, Subhash** [US/US]; 8824 South Poplar Street, Tempe, AZ 85284 (US).

(74) Agents: **GUNN, J., Jeffrey** et al.; Traskbritten, 230 South 500 East, Suite 300, P.O. Box 2550, Salt Lake City, UT 84110-2550 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

— with international search report (Art. 21(3))

(54) Title: III-V SEMICONDUCTOR STRUCTURES AND METHODS FOR FORMING THE SAME

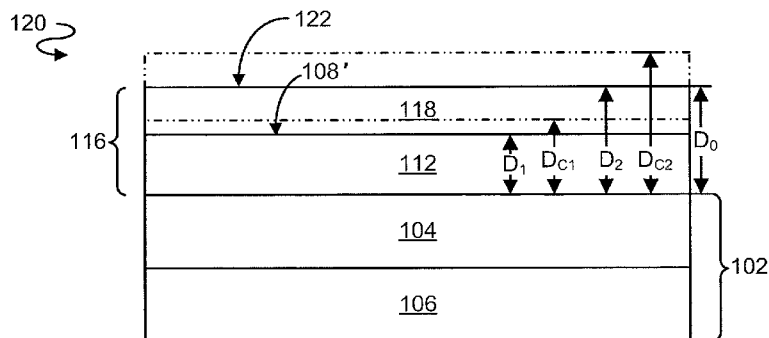


FIG. 1C

(57) Abstract: Embodiments of the invention relate to methods of fabricating semiconductor structures, and to semiconductor structures fabricated by such methods. In some embodiments, the methods may be used to fabricate semiconductor structures of III-V materials, such as InGaN. A semiconductor layer is fabricated by growing sublayers using differing sets of growth conditions to improve the homogeneity of the resulting layer, to improve a surface roughness of the resulting layer, and/or to enable the layer to be grown to an increased thickness without the onset of strain relaxation.