processing on the third analog signal to generate a fourth analog signal, and to send the fourth analog signal through the second communication interface, wherein the first analog signal is generated by a response device that receives the fourth analog signal after the response device performs a fourth processing on the fourth analog signal.

14. The device according to claim 11 or 13, wherein the main control chip further comprises: a control end electrically connected to the first switch module;

the main control chip is configured to send a control signal to the control end when the first digital signal is received; and

the control end is configured to, after receiving the control signal, control the first switch module to turn off the path between the first stationary end and the first connection end, and to control the first switch module to turn on the path between the first stationary end and the second connection end.

15. The device according to claim 12, wherein the main control chip further comprises: a control end electrically connected to the first switch module and the second switch module;

the main control chip is configured to send a control signal to the control end, when the first digital signal is received; and

the control end is configured to, after receiving the control signal, control the first switch module to turn off the path between the first stationary end and the first connection end, to control the first switch module to turn on the path between the first stationary end and the second connection end, to control the second switch module to turn off the path between the second stationary end and the fourth connection end, and to control the second switch module to turn on the path between the second stationary end and the third connection end.

16. The device according to claim 12 or 15, wherein

the main control chip is further configured to obtain a second processing time period T2, the second processing time period T2 is a difference between a time point when the first digital signal is received and a time point when the third analog signal is sent to the sending circuit module, to determine whether a time difference between the second processing time period T2 and the first processing time period T1 is less than a preset value, to determine that communication data between the circuit delay self-measurement device and the response device is not hijacked, in response to determining that the time difference is less than the preset value.