# INTERFACE DEVICE FOR CONVERTING THE FORMAT OF AN INPUT SIGNAL

This invention relates to interface devices for converting the format of input signals such as their data transfer rate, data transfer order, and data transfer method.

A block data transfer circuit using a DMA (Direct Memory Access) technique and a cycle steal circuit has been used as an interface device for converting the format of an input signal. Using the DMA technique block transfer data cannot be read whilst writing in a random access memory, and vice versa. For example, suppose that the display data signal is converted, data cannot be read while it is written into the random access memory, and output data for display is thus not transferred to a display device. Therefore, the display device may not display the data correctly during this time.

In a cycle steal circuit, reading and outputting of the content of a random access memory are synchronised with a write cycle. Therefore, the transfer rate of the output signal is limited by that of the input signal, and the transfer rate cannot be selected as desired.

The present invention seeks to provide an interface device where the format of an input signal is converted into an output signal with the most appropriate transfer rate, order or method, and the transfer rate of the output signal has no limit imposed upon it.

According to the present invention, there is provided an interface device for converting the format of an input signal, comprising a data input circuit for receiving an input signal; a random access memory to store temporarily data sent from said data input circuit; a data output circuit for producing an output signal after reading data from said random access memory; a write address counter to count memory addresses supplied to said random access memory for writing input data; a clock generation circuit for generating a clock signal which operates asynchronously with a clock signal of said write address counter; a read address counter for counting addresses of said random access memory for reading data in dependence upon said clock signal generated by said clock generation circuit; and a read/write control circuit to divide the memory cycle synchronously with the shorter of the cycles of said write address counter and of said read address counter, which cycles are asynchronous with each other in such a manner that the memory cycle is divided into a read cycle having one predetermined period and a write cycle having another predetermined period, thereby alternately generating a writing cycle and a reading cycle in such a manner that one of the writing operation and the reading operation which has the shorter cycle is always effected in one of the divided cycles and the other operation is effected in the other cycle immediately after the increment of the address counter responsive to the clock signal with the longer cycle.

Preferably said read/write control circuit comprises a memory cycle dividing circuit to generate a signal from the clock signal of the address counter of

the operation which has the shorter cycle, which generated signal divides the memory cycle, thereby sharing the memory cycle between the writing cycle and the reading cycle alternately and a reading judge circuit to control said memory cycle dividing circuit so that the writing operation is effected in every said writing cycle and the reading operation is effected in said reading cycle immediately after the increment of said read address counter by controlling the renewal of the other operation address by deferring it if the increment of the other operation address counter coincides with the increment of the shorter cycle operation address counter.

In the preferred embodiment the data input circuit includes a serial/parallel conversion circuit in which serial data of the input signal is converted into parallel data.

The data output circuit may include a data conversion circuit for converting data read from the random access memory to produce the output signal.

The invention extends to apparatus including an interface device according to the invention for converting a video data signal into a display data signal for a liquid crystal display device or a plasma display device or an electro-luminescence display device.

The principle of operation of an interface device according to the present invention is as follows. The data input circuit receives an input signal and data is written at an address specified by the write address counter under the control of the read/write control circuit. Then, written data is read out from the address specified by the read address counter and an output signal produced via the data output circuit under the control of the read/write control circuit.

Thus, the data format of both the input signal and the output signal can be changed into any format via the data input circuit and the data output circuit by storing the data in the random access memory temporarily. Data transfer order for the output signal is also easily set by changing the counting method of

the read address counter.

Since the read cycle and write cycle are controlled by the read/write control circuit in a time sharing manner, the signal output will never be interrupted by the signal fed to the random access memory.

The read address counter to set the transfer rate of the output signal works asynchronously with the write address counter to set that of the input signal. The transfer rate of the signal output is not limited by that of the signal input, and can be set to any value.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of an interface device according to the present invention;

Figure 2 shows schematically the format of a video data signal;

Figure 3 shows schematically the format of an LCD data signal;

Figure 4 is a block diagram of a read/write control circuit of the interface device of Figure 1; and

Figure 5 is a timing chart illustrating the operation of the read/write control circuit of Figure 4.

The embodiments of the present invention are described below with reference to the drawings. In the following description the signal to be converted is a display data signal used in a display device and a data signal for a cathode ray tube (CRT) display device (hereinafter referred to as a "video data signal" )

is converted into a data signal for a liquid crystal display (LCD) device (hereinafter referred to as an "LCD data signal").

Referring to Figure 1 there is shown one embodiment of an interface device according to the present invention. A video data signal 2 is sent from a personal computer 1 through the interface device which produces an LCD data signal 4 for an LCD device 3.

Formats for both the video data signal 2 and the LCD data signal 4 will first be explained. The data format of the video data signal 2 in a non-interlace mode is shown in Figure 2. The screen size (hatched) of a CRT display device is 640 dots by 400 lines. A display data area 101 and a data transfer order 102 are also indicated in Figure 2. A transfer clock signal, a video data signal for one horizontal scanning period, and a video data signal for a single frame display period are indicated by waveforms (a), (b) and (c), respectively. Video data signals are sent serially for sequential dot scanning by the CRT display device. As shown in Figure 2, blanking areas called back porch and front porch periods are provided around the display data area for retrace of the scanning beam.

The characteristics of a typical video data signal are: data transfer rate - 21Mbps; clock frequency - 21MHz; data transfer order - intermittent data transfer including both back porch and front porch periods as invalid data periods; and data transfer method - serial transfer.

The format of the LCD data signal 4 on a screen 103 of an LCD device of 640 horizontal lines, each of 400 dots, and with a data transfer order 104 are shown in Figure 3. A transfer clock signal and the LCD data signal are indicated by waveforms (a) and (b), respectively.

An LCD device of line sequential scanning type outputs one line of data at transferred timing as picture elements. Since the LCD data signal for the next line of data can also be sent within the time required for sending one line of data, a plurality of bits can be sent in parallel. Figure 3 shows the case where four bits are sent in parallel. The LCD data signal has the features: data transfer rate - 14Mbps; clock frequency - 3.5MHz; data transfer order - split screen alternate data transfer; data transfer method - 4-bit in parallel.

From the above it will be appreciated that the video data signal and the LCD data signal are different in transfer rate, order and method. Both the video data signal and the LCD data signal, however, have almost the same frame frequency to transfer one

frame of screen data and this is usually about 60Hz. However, there is a great difference in the clock frequencies. There are two reasons for this:

1. In the case of the video data signal the blanking areas called the back porch and the front porch periods must be provided around the display data area 101 shown in Figure 2, and data for one frame is sent within less than two-thirds of the time required for displaying one frame of data. Therefore, it requires a high clock frequency.

On the other hand in the case of the LCD data signal, the time required for transferring data for one frame is the same as that required for displaying one frame of data. Therefore, it does not require such a high clock frequency.

2. Since the video data signal for a CRT display device is of the dot sequential scanning type because a scanning beam is used, data is sent serially, while the LCD signal is of the line scanning type and a plurality of bits are sent to a segment driver simultaneously.

As stated above, Figure 3 shows 4-bit parallel data transfer, data of one frame is transferred within a quarter of the time of that required for serial data transfer.

In the present embodiment, data of one frame are mixed with that of the next frame. However, in general, in personal computers only part of the data is renewed in the next frame. Therefore, displayed data hardly differs from the transferred data and hardly any impression is made on the human eye. When data is renewed

all at once, mixed data is less than renewed data. Therefore, it seems that the display of the LCD device has changed in an instant.

The interface device of Figure 1 is based upon the above points, the video data signal for the CRT display device being converted and outputted in the most appropriate format for the LCD device 3. Software development for the CRT display device can also be used for the LCD device without any modifications.

In the interface device shown in Figure 1, the video data signal 2 is fed to a serial/parallel (S/P) conversion circuit 8 forming part of a data input circuit 5, and there, serial data is converted to parallel data.

A clock signal 9 for S/P conversion is generated by a phase lock look (PLL) circuit 12 controlled by a horizontal synchronous signal (HSC) 10. The frequency and phase of the clock signal 9 are made appropriate for input of the video data signal 2. The frequency of the clock signal 9 in this embodiment is 21MHz.

A horizontal back porch decision circuit and horizontal dot counter 6, a vertical back porch decision circuit and vertical line counter 7 recognise both the back porch period as an invalid data period and a display period by input of the horizontal synchronous signal 10 and a vertical synchronous (VSC) signal 11, then pick up and convert only valid display data in the video data signal.

In a random access memory (RAM) 16 where 8 bits are regarded as one word, the output of a write address counter 13 are counted

when 8 bit data is inputted. A read/write (R/W) control circuit 17 outputs control signals 18,19 and data sent to the S/P conversion circuit 8 and write addresses counted in the write address counter 13 are outputted to a data bus 14 and an address bus 15, respectively.

By a control signal 20 from the R/W control circuit 17, the data in the S/P conversion circuit 8 is written into the RAM 16. On the other hand, a clock generation circuit 25 generates the read clock signal 26 which works asynchronously with the write clock signal 9.

An LCD data conversion circuit 24 within a data output circuit 22 converts the data read from the RAM 16 into 4 bit parallel data. The LCD data signal 4 is outputted in accordance with the clock signal 26. The transfer clock frequency in this embodiment is 3.5MHz. An LCD control signal generation circuit 23 also forming part of the output circuit 22 generates a control signal 29 required for the LCD device 3.

A read address counter 27 is counted once 8 bits of data are outputted. Then the R/W control circuit 17 switches the control signal 18 to output the counted read address to the address bus 15. Thus, the RAM 16 outputs data to the data bus 14. The LCD data conversion circuit 24 takes in data via a control signal 21 and outputs it as the LCD data signal. The read address counter 27 counts the address of one line of display data in the upper sceen and the lower screen in turn in accordance with the transferred order of the LCD data signal. This, in outline, is the operation of the interface device.

The operation of the R/W control circuit 17 will now be described with reference to Figure 4 which shows the R/W control circuit 17 in detail and to Figure 5 which is a timing chart of the operation of the R/W control circuit. The R/W control circuit 17 enables operation of both writing and reading data and to this end performs the operations of: synchronisation of the write address counter 13 and the read address counter 27, and generation of a signal for switching read addresses and write addresses.

In Figure 4 a signal 42 generated by a reading judge circuit 35 indicates read address change. In other words, a rising differentiation circuit 36 differentiates the rising edge of a clock signal 31 for the read address counter to generate a signal 40. The signal 40 is sent to a latch 38 which outputs the signal 42. A signal 41 sent to the latch 38 is generated by differentiating the falling edge of a clock signal 30 of the write address counter 13, having a narrower pulse width than that of the signal 40. Therefore, when the rising edge of the clock signal 31 coincides with the falling edge of the clock signal 30, the signal 42 outputted from the latch 38 does not change because the clock signal 41 is low level. It changes when the latter is high level. In other words, when switching edges of the write clock signal 30 and a read clock signal 31 coincide, the circuit 35 outputs the signal 42 behind time so that the output of a newly read address may be sent to the next cycle.

Since the clock signal 30 works asynchronously with the clock signal 31, there exists every possible timing relationship.

Therefore, as shown above, the falling edge of the clock signal 30 and the switch output timing of the read address counter 27 occurs at the same time as the rising edge of the clock signal 31 and the count timing of the read address counter at random with a given probability.

The circuit 35 sends the control signal 21 for reading new addresses as data from the RAM 16 to the next cycle so that reading out may be performed successfully. The R/W control circuit 17 prevents misoperation of the circuit such as the control signal 21 is not outputted while the read address is changed and vice versa. Thus asynchronous operation of the read address counter 27 with the write address counter 13 becomes possible.

After the read address is changed and the signal 42 is outputted, an RS flip-flop 39 is set and a signal 43 is high level. Thus, reset status of flip-flops 45,46 are cancelled and the clock signal 30 can be inputted. After the clock signal 30 is inputted, the flip-flop 45 produces the control signal 21 to indicate the read address change and is synchronised with the clock signal 30 of the write address counter. The signal 21 is outputted to a latch 28 and the LCD data conversion circuit 24 as shown in Figure 1, and data is read out from the RAM 16.

The latch 28 latches the read address of the read address counter 27 on a bus 33 and outputs it on a bus 34 synchronously with the signal from the write address counter 30. The LCD data conversion circuit 24 takes in the data from the RAM 16 upon receipt of the control signal 21.

A signal 44 from the flip-flop 46 is used to reset the RS flip-flop 39, and the LCD conversion circuit 24 has wait status for read address change. A memory cycle dividing circuit generates the signal 18, which is the inverted signal of the clock signal 30, to switch read addresses and write addresses. A write address is outputted to the address bus 15 when the signal 18 is at low level, while a read address is outputted to the address bus when it is at high level as shown in Figure 1. The timing chart in Figure 5 also illustrates these signals. The address bus 15 is time shared by the clock signal 30 and write addresses and read addresses are outputted in turn.

The write address is renewed every cycle, while the read address is renewed only at the next read cycle after the read address counter 27 is counted. The control signal 21 is only produced at that time and the LCD data conversion circuit 24 takes in new data from the RAM 16.

As described above the R/W control circuit 17 synchronises the addresses counted asynchronously relative to each other and control the read cycle and write cycle in a time sharing manner. Asynchronous writing and reading of the data is thus accurately accomplished. Accordingly, the present invention is desirably applied to, for example, information display peripherals such that data loss or data deficiency causes that the user cannot recognise the displayed characters, such as an LCD display device for displaying characters.

The operation of the video data signal input is shown in Figure 4. Since the video data signal is not inputted during the back porch and front porch period, the R/W control circuit

generates only read cycle. In this case the signal 18 is set to high level so that the read address is outputted at any time. Every time the read address counter 27 is counted, the control signal 21 is outputted and new data is read from the RAM 16.

The R/W control circuit illustrated in Figure 4 is only one of many embodiments of circuits to perform the same function. Moreover, there are other methods of controlling read and write cycles. As explained above, the interface device according to the present invention and described above enables the conversion of video data signals for a CRT display device into LCD data signals for a liquid crystal display device, the signals having different transfer rate, order and method. Essentially in this interface device signals are input into a data input circuit, data is temporarily stored in a RAM, and then read out to produce output signals via a data output circuit. Since the read/write control circuit synchronises asynchronous addresses, writing of input data and reading of output data are performed asynchronously. Therefore, the transfer rate of the output signal can be set at any value appropriate for the LCD display device. Thus the video data signal can be converted into an LCD data signal in the interface device enabling replacement of a conventional large CRT display device which has a relatively large power consumption with a thin LCD device which consumes less power. There is no need to change both hardware and software for signal conversion. The smallness and lightness of an LCD display device meet the needs of small personal computers. Data output is performed asynchronously with data input and data remains displayed using

back-up or auxiliary batteries to operate the interface device and the LCD device independently even when there is power failure.

Whilst the present invention is described in relation to the conversion of a video data signal for a CRT display device into that for an LCD device, conversion for other display devices such as plasma display devices, electro-luminescence display devices, etc., can be achieved similarly. Further, conversion of the video data signal for a CRT display device into a signal for devices other than display devices, such as video printers is possible. In this case, output data can be taken out at appropriate timing by reconfiguring the data output circuit 22 for handshaking with a central processing unit or a DMA controller of a video printer. These applications are possible since input and output of data are performed asynchronously.

The interface device according to the present invention and described above has a range of uses and so can be used for general data conversion.

# C L A I M S

1. An interface device for converting the format of an input signal, comprising a data input circuit for receiving an input signal; a random access memory to store temporarily data sent from said data input circuit; a data output circuit for producing an output signal after reading data from said random access memory; a write address counter to count memory addresses supplied to said random access memory for writing input data; a clock generation circuit for generating a clock signal which operates asynchronously with a clock signal of said write address counter; a read address counter for counting addresses of said random access memory for reading data in dependence upon said clock signal generated by said clock generation circuit; and a read/write control circuit to divide the memory cycle synchronously with the shorter of the cycles of said write address counter and of said read address counter, which cycles are asynchronous with each other in such a manner that the memory cycle is divided into a read cycle having one predetermined period and a write cycle having another predetermined period, thereby alternately generating a writing cycle and a reading cycle in such a manner that one of the writing operation and the reading operation which has the shorter cycle is always effected in one of the divided cycles and the other operation is effected in the other cycle immediately after the increment of the address counter responsive to the clock signal with the longer cycle.

2. A device as claimed in claim 1, in which said read/write control circuit comprises a memory cycle

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dividing circuit to generate a signal from the clock signal of the address counter of the operation which has the shorter cycle, which generated signal divides the memory cycle, thereby sharing the memory cycle between the writing cycle and the reading cycle alternately and a reading judge circuit to control said memory cycle dividing circuit so that the writing operation is effected in every said writing cycle and the reading operation is effected in said reading cycle immediately after the increment of said read address counter by controlling the renewal of the other operation address by deferring it if the increment of the other operation address counter coincides with the increment of the shorter cycle operation address counter.

3. A device as claimed in claim 1 or 2, in which the data input circuit includes a serial/parallel conversion circuit in which serial data of the input signal is converted into parallel data.

4. A device as claimed in any preceding claim, in which the data output circuit includes a data conversion circuit for converting data read from the random access memory to produce the output signal.

5. An interface device for converting the format of an input signal, substantially as herein described with reference to and as shown in the accompanying drawings.

6. Apparatus including an interface device according to any of the preceding claims, for converting a video data signal into a display data signal for a liquid crystal display device or a plasma display device or an electro-luminescence display device.

* C L M S *