What is claimed is:

CLAIMS

1. A device comprising:

a substrate having a high voltage (HV) device region, wherein the HV device region is defined with first and second device isolation regions and an internal dielectric region, and wherein the device isolation regions and internal dielectric region are shallow trench isolation (STI) regions;

a HV transistor disposed in the HV device region, wherein the HV transistor comprises

a gate ~~dielectric layer~~ disposed on the substrate,

~~a gate disposed on the gate dielectric layer,~~

a source region disposed in the substrate adjacent to the gate and first device isolation region,

a drain region disposed in the substrate adjacent to the second device isolation region;

a drift well disposed in the substrate, wherein the drift well encompasses the drain region and extends under a portion of the gate;

a body well disposed in the substrate, wherein the body well encompasses the source region and extends laterally toward the drift well; and

at least one buried RESURF region disposed within the drift well, wherein the at least one buried RESURF region comprises a first buried RESURF region which is disposed under the internal dielectric region, wherein the first buried RESURF region is an extended buried RESURF region which comprises

a planar top surface which is contiguous and in direct contact with a bottom surface of the internal dielectric region,

first and second edges that extend laterally beyond edges of the internal dielectric region and a vertical depth of the extended buried RESURF region is substantially constant for portions of the buried RESURF region that are under the internal dielectric region and portions of the buried RESURF region that extend beyond and are outside of the internal dielectric region, and the extended buried RESURF region effectively reduces electric fields that are caused by material discontinuities at the edges of the internal dielectric region.

2. The device of claim 1 wherein:

the substrate, the body well and the at least one buried RESURF region comprise second polarity type dopants; and

the source and drain regions and the drift well comprise first polarity type dopants.

3. The device of claim ~~2~~ 1 wherein the STI regions have a top surface which is substantially planar with a top surface of the substrate.

4. The device of claim ~~3~~ 1 wherein the drain region is displaced away from the internal dielectric region ~~is disposed within the drift well~~.

5. The device of claim ~~4~~ 1 wherein the internal dielectric region comprises a width which is wider than a width of the first and second device isolation regions along a channel length direction of the HV device region.

6. The device of claim 5 wherein:

the first device isolation region surrounds the HV transistor;

the internal dielectric region comprises a racetrack shape; and

the second device isolation region is enclosed by the internal dielectric region.

7. The device of claim 5 wherein

the internal dielectric region comprises a finger-type layout having one or more fingers;

the first device isolation region surrounds the HV transistor and extends into the fingers of the internal dielectric region in an interdigitated manner; and

the second device isolation region is enclosed by the internal dielectric region.

8. The device of claim ~~3~~ 1 wherein: ~~the at least one buried RESURF region extends laterally beyond edges of the internal dielectric region and a vertical depth of the buried RESURF region is substantially constant for portions of the buried RESURF region that are under the internal dielectric region and portions of the buried RESURF region that are outside of the internal dielectric region~~

the HV transistor further comprises a drain field plate (DFP) disposed on the substrate, wherein the gate and the DFP each comprises a gate electrode and a gate dielectric, and wherein a first portion of the gate electrode of the gate and DFP is in direct contact with a portion of the internal dielectric region while a second portion of the gate electrode of the gate and DFP is disposed over and in direct contact with the gate dielectric.

9. The device of claim ~~3~~ 8 wherein the gate dielectric of the DFP is disposed over and in direct contact with a portion of the drift well which separates the drain region from the internal dielectric region ~~the at least one buried RESURF region is disposed between edges of the internal dielectric region~~.

10. The device of claim ~~3~~ 1 wherein the at least one buried RESURF region comprises a second buried RESURF region which is disposed below the first buried RESURF region and vertically separated from the first buried RESURF region by a portion of the drift well.

11. The device of claim 10 wherein the second buried RESURF region has a greater lateral separation from the source region compared to a lateral separation of the first buried RESURF region from the source region.

12. The device of claim ~~8~~ 10 wherein lateral edges of the first and second buried RESURF regions are aligned.

13. The device of claim 1 further comprising a body well contact disposed within the body well, wherein the body well contact comprises second polarity type dopants.

14. The device of claim 1 wherein the drift well extends laterally from the second device isolation region to underlap a portion of the gate, and wherein the drift well also encompasses the internal dielectric region ~~further comprising a drain field plate (DFP) disposed over the gate dielectric layer and extending laterally from the drain region at least to a first edge of the internal dielectric region~~.

15. A method for forming a high voltage (HV) device comprising:

providing a substrate;

forming first and second device isolation regions and an internal dielectric region in the substrate, wherein the device isolation regions and internal dielectric region are shallow trench

isolation (STI) regions which have a top surface which is substantially planar with a top surface of the substrate;

forming a gate ~~dielectric~~ over the substrate;

~~forming a gate on the gate dielectric;~~

forming a source region in the substrate adjacent to a first side of the gate and first device isolation region;

forming a drain region in the substrate adjacent to a second side of the gate;

forming a drift well in the substrate, wherein the drift well encompasses the drain region and extends under a portion of the gate;

forming a body well in the substrate, wherein the body well encompasses the source region and extends laterally toward the drift well; and

forming at least one buried RESURF region within the drift well, wherein the at least one buried RESURF region comprises a first buried RESURF region which is formed under the internal dielectric region, wherein the first buried RESURF region is an extended buried RESURF region which comprises

a planar top surface which is contiguous and in direct contact with a bottom surface of the internal dielectric region,

first and second edges that extend laterally beyond edges of the internal dielectric region and a vertical depth of the first buried RESURF region is substantially constant for portions of the extended buried RESURF region that are under the internal dielectric region and portions of the buried RESURF region that extend beyond and are outside of the internal dielectric region, and the extended buried RESURF region effectively reduces electric fields that are caused by material discontinuities at the edges of the internal dielectric region.

16. The method of claim 15 wherein ~~the STI regions have a top surface which is substantially planar with a top surface of the substrate~~ drain region is displaced away from the internal dielectric region.

17. The method of claim 16 wherein forming the gate also simultaneously forms a drain field plate (DFP) over the substrate, wherein the gate and the DFP each comprises a gate electrode and a gate dielectric, and wherein a first portion of the gate electrode of the gate and DFP is in direct contact with a portion of the internal dielectric region while a second portion of the gate electrode of the gate and DFP is formed over and in direct contact with the gate dielectric ~~the at least one buried RESURF region extends beyond edges of the internal dielectric region~~.

18. The method of claim 17 wherein the gate dielectric of the DFP is formed over and in direct contact with a portion of the drift well which separates the drain region from the internal dielectric region ~~portion of the buried RESURF region which extends beyond the edges of the internal dielectric region is at the same vertical depth as a portion of the buried RESURF region under the internal dielectric region~~.

19. The method of claim 15 wherein forming the at least one buried RESURF region comprises ~~forming a first buried RESURF region that is contiguous with the internal dielectric region and~~ forming a second buried RESURF region below and displaced a distance away from a bottom of the first buried RESURF region.

20. The method of claim 19 wherein lateral edges of the first and second buried RESURF regions are not aligned.

21. A high voltage (HV) transistor comprising:

a semiconductor substrate having a first conductivity type;

an internal dielectric region disposed in the substrate, the internal dielectric region having a top surface which is substantially planar with a top surface of the substrate;

a gate ~~dielectric layer~~ disposed on the substrate;

~~a gate disposed on the gate dielectric layer;~~

a source region disposed in the substrate adjacent to the gate;

a drain region disposed in the substrate, wherein the drain region is separated from the source region by the internal dielectric region;

a drift well disposed in the substrate, wherein the drift well encompasses the drain region, extends under a first portion of the gate, and is separated from the source region by a second portion of the gate;

a body well disposed in the substrate, wherein the body well encompasses the source region and extends laterally under the gate toward the drift well; and

a first buried RESURF region disposed within the drift well and under the internal dielectric region, wherein the first buried RESURF region is an extended buried RESURF region which comprises

a planar top surface which is contiguous and in direct contact with a bottom surface of the internal dielectric region,

first and second edges that extend laterally beyond edges of the internal dielectric region and a vertical depth of the buried RESURF region is substantially constant for portions of the buried RESURF region that are under the internal dielectric region and portions of the buried RESURF region that extend beyond and are outside of the internal dielectric region, and the extended buried RESURF region effectively reduces electric

fields that are caused by material discontinuities at the edges of the internal dielectric region.

22. The device of claim 21 wherein the internal dielectric region is a shallow trench isolation (STI) region comprising a deposited oxide layer and having a depth in the range of about 200 to 600 nm.

23. The device of claim 21 wherein the drain region is displaced away from ~~the first buried RESURF region is contiguous with~~ the internal dielectric region.

24. The device of claim ~~23~~ 21 further comprising a second buried RESURF region which is disposed below the first buried RESURF region and vertically separated from the first buried RESURF region by a portion of the drift well.

25. The device of claim 24 wherein the second buried RESURF region has a greater lateral separation from the source region compared to a lateral separation of the first buried RESURF region from the source region.

26. The device of claim 24 wherein lateral edges of the first and second buried RESURF regions are aligned.

27. The device of claim 21 wherein the HV transistor further comprises a drain field plate (DFP) disposed on the substrate, wherein the gate and the DFP each comprises a gate electrode and a gate dielectric, wherein a first portion of the gate electrode of the gate and DFP is in direct contact with a portion of the internal dielectric region while a second portion of the gate

electrode of the gate and DFP is disposed over and in direct contact with the gate dielectric ~~the first buried RESURF region extends laterally beyond edges of the internal dielectric region~~.

28. The device of claim 27 wherein the gate dielectric of the DFP is disposed over and in direct contact with a portion of the drift well which separates the drain region from the internal dielectric region ~~portion of the buried RESURF region which extends beyond the edges of the internal dielectric region is at the same vertical depth as a portion of the buried RESURF region under the internal dielectric region~~.

29. The device of claim 27 wherein the drain region is disposed adjacent to the DFP and underlaps a portion of the DFP.