

DUAL DAMASCENE PROCESS

FIELD OF THE INVENTION

[0001] The present invention relates to a dual damascene process, and more particularly to a dual damascene process including a single etching step.

BACKGROUND OF THE INVENTION

[0002] Aluminum multilevel interconnection is widely used in semiconductor process for a long time. However, since the linewidth of interconnection wires become narrower and narrower but more and more data should be carried, copper wiring gradually appear advantages over aluminum wiring due to its lower resistivity. Nevertheless, conventional subtractive etching method used for forming aluminum wires is not suitable for forming copper wires, and a new damascene process is thus developed. In the damascene process, a hole already formed in a dielectric layer is filled with metal material to provide the interconnection structure, which is not formed by etching metal layer. Moreover, several dual damascene processes are proposed to combine via formation and trench formation so that only one metal-fill step is required to form inter-metal wires and contacts.

[0003] Please refer to FIG. 1, a schematic diagram illustrating a known dual damascene structure. The dual damascene structure 1 includes a substrate 11, a dielectric layer 12 and a metal structure 13. The substrate 11 may have conductive layout therein to be electrically connected. There is a T-shape hole in the dielectric layer 12 wherein the upper portion is called as a trench and the lower portion is called as a via

hole. The T-shape hole is filled with the metal structure 13 to provide interconnection and circuit layout.

[0004] Compared to the conventional subtractive etching method, the dual damascene process is much more complex. There are three known dual damascene processes, including trench first process, via first process and self-aligned process, and brief description related to the processes is given in the following paragraphs.

[0005] Please refer to FIGs. 2A-2C, schematic diagrams illustrating the trench first process. A first dielectric layer 221, an etch stop layer 222 and a second dielectric layer 223 are sequentially formed on a substrate 21. Then, a first photoresist 241 for defining a trench 261 is formed on the second dielectric layer 223. After a first etching step reaching the etch stop layer 222, an unprotected portion of the second dielectric layer 223 is etched off to form the trench 261 (FIG. 2A). Then, the first photoresist 241 is stripped off and the second dielectric layer 223 and a portion of the etch stop layer 222 are covered with a second photoresist 242 for defining a via hole (FIG. 2B). A second etching step is performed through an unprotected portion of the etch stop layer 222 to etch the etch stop layer 222 and the first dielectric layer 221 to form the via hole 262. After removal of the second photoresist 242, the resultant structure is ready for a metal-fill step for filling the trench 261 and the via hole 262 (FIG. 2C).

[0006] Please refer to FIGs. 3A-3C, schematic diagrams illustrating the via first process. A first dielectric layer 321, an etch stop layer 322 and a second dielectric layer 323 are sequentially formed on a substrate 31. Then, a first photoresist 341 for defining a via hole 362 is formed on the second dielectric layer 323. After a first etching step, a portion of the second dielectric layer 323, the etch stop layer 322 and the first dielectric

layer 321 are etched off to form the via hole 362 in the first dielectric layer (FIG. 3A). Then, the first photoresist 341 is stripped off and a second photoresist 342 for defining a trench 361 is formed on the second dielectric layer 323 (FIG. 3B). A second etching step is performed to etch off an unprotected portion of the second dielectric layer 323 to form the trench 361. After removal of the second photoresist 342, the resultant structure is ready for metal-fill step for filling the trench 361 and the via hole 362 (FIG. 3C).

[0007] Please refer to FIGs. 4A-4C, schematic diagrams illustrating the self-aligned process. A first dielectric layer 421 and an etch stop layer 422 are sequentially formed on a substrate 41. Then, a first photoresist 441 for defining a via hole 462 is formed on the etch stop layer 422. After a first etching step, the etch stop layer 422 is “opened” (FIG. 4A). The first photoresist 441 is stripped off, and a second dielectric layer 423 and a second photoresist 442 for defining a trench 461 are formed on the opened etch stop layer 422 (FIG. 4B). A second etching step is performed to form the trench 461 in the second dielectric layer 423. After the etching step reaches the etch stop layer 422, the first dielectric layer 421 is etched through the opening of the etch stop layer 422 to form the via hole 462 in the first dielectric layer 421. Hence, the trench 461 and the via hole 462 are formed in the same etching step. After removal of the second photoresist 442, the resultant structure is ready for metal-fill step for filling the trench 461 and the via hole 462.

[0008] From above description, it is known that at least two etching steps are necessary for all the three dual damascene processes. Each etching step is usually followed by several wafer-treating steps such as cleaning. Hence, too many etching steps adversely affect the production

efficiency, especially when the dual damascene process is performed several times for a specific wafer to achieve multilevel interconnection. An improved and simplified dual damascene process with competitive cost and shorter cycle time is desired.

SUMMARY OF THE INVENTION

[0009] The present invention provides a dual damascene process for forming a trench and a via hole in a single etching step.

[0010] In accordance with an aspect of the present invention, the dual damascene process includes the following steps. At first, a dielectric layer, a reversed trench organic anti-reflective coating (ARC) layer, and a mask layer are sequentially formed on a substrate. The mask layer has a thinner portion corresponding to a position of a to-be-formed trench in the dielectric layer and a thicker portion, and an opening corresponding to a via-pattern is then formed on the thinner portion. During a single etching step with different etching conditions by selectively using the thinner portion or the thicker portion of the mask layer as etching masks, a trench and a via hole are then formed in the dielectric layer.

[0011] In an embodiment, the single etching step includes the following etching sub-steps. The reversed trench organic ARC layer is etched through the opening of the mask layer to expose a portion of the dielectric layer corresponding to a via-pattern. Next, the dielectric layer is partially etched through the exposed portion of the dielectric layer along with the mask layer till the thinner portion of the mask layer is entirely etched off. Then, the reversed trench organic ARC layer is etched by using the remaining mask layer as the etching mask to expose another portion of the dielectric layer corresponding to a trench-pattern. At last,

the dielectric layer is etched through the exposed portion of the dielectric layer along with the mask layer till the mask layer is entirely etched off.

[0012] In accordance with another aspect of the present invention, the dual damascene process includes the following steps. At first, a dielectric layer and a mask layer are sequentially formed on a substrate. The mask layer has a thinner portion corresponding to a position of a to-be-formed trench in the dielectric layer and a thicker portion, and an opening corresponding to a via-pattern is formed on the thinner portion. During a single etching step with different etching recipes, a trench and a via hole are then formed in the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and the accompanying drawings, in which:

[0014] FIG. 1 is a schematic diagram illustrating a typical dual damascene structure in the prior arts.

[0015] FIGs. 2A-2C are schematic diagrams illustrating a conventional trench first process for forming the dual damascene structure.

[0016] FIGs. 3A-3C are schematic diagrams illustrating a conventional via first process for forming the dual damascene structure.

[0017] FIGs. 4A-4C are schematic diagrams illustrating a conventional self-aligned process for forming the dual damascene structure.

[0018] FIGs. 5A-5I are schematic diagrams illustrating a dual damascene process of an embodiment according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0019] It is to be understood that other embodiment may be utilized and structural changes may be made without departing from the scope of the present invention. Also, it is to be understood that the phraseology and terminology used herein are for the purpose of description and should not be regarded as limiting. The use of “including,” “comprising,” or “having” and variations thereof herein is meant to encompass the items listed thereafter and equivalents thereof as well as additional items. Unless limited otherwise, the terms “connected,” “coupled,” and “mounted,” and variations thereof herein are used broadly and encompass direct and indirect connections, couplings, and mountings.

[0020] According to the conventional dual damascene process, at least two etching steps are required, for example, one for via-etching and the other one for trench-etching. To reduce the etching steps, the present invention provides a process flow to form a trench and a via hole in a single etching step. FIG. 5A-5J are schematic diagrams illustrating the novel dual damascene process.

[0021] Please refer to FIG. 5A. At first, a substrate layer 51 including conductive layout is provided. The conductive layout may include contacts, electrodes, wires, interconnection structure or other conductive component to be electrically connected to external interconnection structure, for example, a Cu contact 511 in FIG. 5A. An inter-metal dielectric (IMD) layer 52 is formed on the substrate 51. The

IMD layer 52 may have a laminated structure for providing different function. In this embodiment, an etch stop layer 521, an IMD oxide layer 522 and an IMD top layer 523 are sequentially formed on the substrate 51. Although chemical vapor deposition (CVD) silicon oxide is the most used IMD material, the present invention is not limited to this, and may involve tetraethyl orthosilicate (TEOS), phosphorsilicate glass (PSG), fluorosilicate glass (FSG) or other dielectric layer formed by CVD, plasma enhanced (PE) CVD, high density plasma (HDP) CVD, or spin-on method.

[0022] Then, an organic anti-reflective coating (ARC) layer 53 is formed on the IMD layer 52 (FIG. 5B). It is to be noted that a reversed trench lithography procedure is performed to make the organic ARC layer 53 to have a reversed trench structure. That is, a portion of the organic ARC layer 53 corresponding to a trench to be formed in the IMD layer 52 is raised, in other words, higher and thicker than other portions. A thicker portion 531 and a thinner portion 532 of the organic ARC layer 53 are shown in this diagram.

[0023] A mask layer 54 and a photoresist layer 55 with a via-pattern are sequentially formed on the reversed trench organic ARC layer 53 (FIG. 5C). The mask layer 54 overlying the organic ARC layer 53 may be a Si-rich ARC layer, formed by spin-on method or CVD-related method, which is a single-layer or multi-layer widely used at sub-65nm IC fabrication and has good step coverage capability and good adhesion capability to photoresist. Therefore, the formed mask layer 54 has a relatively planar profile and includes a thinner portion 541 and a thicker portion 542 corresponding to the thicker portion 531 and the thinner portion 532 of the organic ARC layer 53, respectively. In other words, the

position of the thinner portion 541 of the mask layer 54 corresponds to the position of the trench to be formed in the IMD layer 52.

[0024] FIGs.5D-5I illustrating the one-step etching recipes in sequence. Several etching conditions are listed in the description, but it is not intended to limit the etching conditions. Other proper etchant gases may be applicable according to the material and required etching rates of the etched layers and associated mask layers.

[0025] At the beginning of the etching step (FIG. 5D), the mask layer 54 is opened according to the via-pattern of the photoresist layer 55. In this etching sub-step, $\text{CF}_4/\text{Ar}/\text{O}_2$ based etching may be performed. Then, the etching step goes to FIG. 5E. CO/O_2 based etching clears the photoresist layer 55 and continues the downward etching through the opened mask layer 54. Preferably, the etching rate of the mask layer 54 ranges from 1/5 to 1/15 of the etching rate of the organic ARC layer 53. If the mask layer 54 includes Si-rich ARC material, the etching rate of the mask layer 54 is about 1/6 to 1/10 of the etching rate of the organic ARC layer 53. Hence, the mask layer 54 can protect the layers below before the downward etching through the opening reaches the IMD layer 52.

[0026] Now, the etching step starts to etch the IMD layer 52 to form a via profile 61 in the IMD layer 52. At the same time, the thinner portion 541 as well as a portion of the thicker portion 542 of the mask layer 54 is consumed (FIG. 5F). In this embodiment, $\text{C}_4\text{H}_8/\text{CF}_4/\text{O}_2$ based etching is utilized. By adjusting thickness of the thinner portion 541 of the mask layer and the etching time, when the via profile 61 is formed, the removal of the thinner portion 541 of the mask layer 54 just finishes. Then, a trench profile 62 is formed by CO/O_2 based etching to remove the unprotected organic ARC layer 53, i.e. the thicker portion 531 of the

organic ARC layer 53 (FIG. 5G). The resultant structure includes the trench profile 62 and the via profile 61.

[0027] Since the trench profile 62 and the via profile 61 are formed, an anisotropic downward etching is performed to etch the IMD layer 52 to “push down” the trench profile 62 and the via profile 61. The etching also removes the remaining portion of the mask layer 54 (FIG. 5H). C_4F_8 or C_4F_6 or $C_5F_8/Ar/O_2$ or N_2 based etching is selected in this etching sub-step. By adjusting thickness of the thicker portion 542 of the mask layer 54 and the etching time, when the via profile 61 reaches the IMD etch stop layer 521 or the bottom of the IMD layer 52, the removal of the remaining mask layer 54 just finishes. At last, the remaining organic ARC layer 53 is stripped off by O_2 or CO_2 based etching, and the IMD etch stop layer 521 is opened by CF_4/N_2 based etching, if required (FIG. 5I). The resultant dual damascene structure is ready for metal-fill step for filling the trench 72 and the via hole 71 to electrically connect the contact 511 with the filled metal. The metal may be selected from Cu, Cu alloy, Al, Al alloy and other metal or alloy. The method used for filling the trench 72 and the via hole 71 may be selected from CVD, PVD (physical vapor deposition), electroplating and combinations thereof. The metal layer (not shown) should be planarized by chemical mechanical polishing (CMP) or other planarizing process.

[0028] Furthermore, before the metal-filled step, a barrier layer (not shown) of Ta, TaN, TiN or other barrier layer is preferably formed to cover the surface of dual damascene structure to prevent metal ion migration into the IMD layer 52.

[0029] According to the present invention, the mask layer 54 does not have uniform thickness. In fact, the mask layer 54 has a thinner portion

541 and a thicker portion 542 to serve as hard masks for different etching stages. The thinner portion 541 serves as a hard mask for opening the organic ARC layer 53 to expose the IMD layer 52 corresponding to the via-pattern (FIG. 5E). Furthermore, when the thinner portion 541 of the mask layer 54 is entirely etched off, the via profile 61 in the IMD layer 52 is formed (FIG. 5F). Certainly, the thicker portion 542 is partially etched at this stage. Next, the remaining thicker portion 542 serves as a hard mask for opening the organic ARC layer 53 again to expose the IMD layer 52 corresponding to the trench-pattern (FIG. 5G). Furthermore, when the remaining thicker portion 542 of the mask layer 54 is entirely etched off, the trench 72 and the via hole 71 are formed in the IMD layer 52. Therefore, the mask layer 54 can be used to decide the starting points of via-etching and trench-etching due to thickness difference. In the above-described embodiment, the mask layer 54 includes the Si-rich ARC layer. In another embodiment, the mask layer 54 may further include a thin low temperature oxide (LTO) layer with higher etching rate.

[0030] As mentioned above, the thickness or etching rate of each of the organic ARC layer 53 and the mask layer 54 is critical for this approach. For example, the organic ARC layer 53 should be thick enough to avoid line edge roughness (LER) or striation occurring on the surface of the IMD layer 52 during the via-etching stage and the trench-etching stage. In addition, the thickness of the mask layer 54 should be well determined to assure correct depth of the formed trench 72 and via hole 71. If the thinner portion 541 or the thicker portion 542 of the mask layer 54 is too thick, there is undesired residual mask layer 54 after the formation of the via profile 61 or the formation of the trench 71 and the via hole 72. It adversely affects the removal of the organic ARC layer 53 in the

subsequent etching sub-steps. On the contrary, if the thinner portion 541 or the thicker portion 542 of the mask layer 54 is not thick enough, the mask layer 54 cannot provide good protection capability for the layers below, and the profile of the dual damascene structure is likely damaged.

[0031] In conclusion, under well etching control, the trench and the via hole of the dual damascene structure can be formed in a single etching step. The mask layer with different thickness provides hard masks for formation of different parts of the dual damascene structure. To provide the mask layer with different thickness, no additional etching step is required. By forming the mask layer with good step coverage capability on the reversed trench organic ARC layer, the mask layer with desired conformation is thus obtained. Hence, the present invention provides a simpler dual damascene process with improved cycle time compared with the conventional dual damascene processes.

[0032] The above description is given by way of example, and not limitation. Given the above disclosure, one skilled in the art could devise variations that are within the scope and spirit of the invention disclosed herein, including configurations ways of the recessed portions and materials and/or designs of the attaching structures. Further, the various features of the embodiments disclosed herein can be used alone, or in varying combinations with each other and are not intended to be limited to the specific combination described herein. Thus, the scope of the claims is not to be limited by the illustrated embodiments.

WHAT IS CLAIMED IS:

1. A dual damascene process, comprising steps of:
 - providing a substrate;
 - forming a dielectric layer on the substrate;
 - forming a reversed trench organic anti-reflective coating (ARC) layer on the dielectric layer;
 - forming a mask layer covering the reversed trench organic ARC layer to make the mask layer to have a relatively thinner portion and a relatively thicker portion wherein an opening is formed on the relatively thinner portion; and
 - partially etching the organic ARC layer and the dielectric layer in a single etching step to form a trench and a via hole of a dual damascene structure in the dielectric layer while the relatively thinner portion and the relatively thicker portion of the mask layer is selectively used as an etching mask.
2. The dual damascene process according to claim 1 wherein the step of forming the dielectric layer on the substrate further comprises a step of sequentially forming an inter-metal dielectric (IMD) etch stop layer, an IMD oxide layer and an IMD top layer.
3. The dual damascene process according to claim 2 wherein the single etching step further comprises an etch sub-step of etching the IMD etch stop layer to expose an underlying conductive component in the substrate.
4. The dual damascene process according to claim 1 wherein the reversed trench organic ARC layer is formed by a reversed trench lithography procedure so that the reversed trench organic ARC layer has a relatively thicker portion corresponding to a position of the trench and a relatively

thinner portion.

5. The dual damascene process according to claim 4 wherein the relatively thinner portion and the relatively thicker portion of the mask layer corresponds to the relatively thicker portion and the relatively thinner portion of the reversed trench organic ARC layer, respectively.

6. The dual damascene process according to claim 1 wherein the single etching step further comprises an etching sub-step to form the opening on the relatively thinner portion of the mask layer by using a photoresist layer with a via-pattern overlying the mask layer.

7. The dual damascene process according to claim 1 wherein the mask layer comprises a Si-rich ARC layer having an etching rate ranging from 1/6 to 1/10 of an etching rate of the reversed trench organic ARC layer.

8. The dual damascene process according to claim 7 wherein the mask layer further comprises a low temperature oxide layer combined with the Si-rich ARC layer.

9. The dual damascene process according to claim 1 wherein the single etching step further comprises sub-steps of:

etching the reversed trench organic ARC layer through the opening of the mask layer to expose a portion of the dielectric layer corresponding to the via-pattern;

partially etching the dielectric layer through the exposed portion of the dielectric layer along with the mask layer till the relatively thinner portion of the mask layer is entirely etched off;

using the remaining mask layer as the etching mask to etch the reversed trench organic ARC layer to expose another portion of the

dielectric layer corresponding to a trench-pattern; and

etching the dielectric layer through the exposed portion of the dielectric layer along with the mask layer till the mask layer is entirely etched off.

10. The dual damascene process according to claim 9, further comprising an etching sub-step to etch off the remaining reversed organic ARC layer.

11. The dual damascene process according to claim 1, further comprising steps of:

filling the trench and the via hole with a metal material; and
planarizing the metal material.

12. The dual damascene process according to claim 11 wherein before the step of filling the trench and the via hole, the dual damascene process further comprises a step of forming a barrier layer over the trench and the via hole.

13. A dual damascene process, comprising steps of:

providing a substrate;

forming a dielectric layer on the substrate;

forming a mask layer having a relatively thinner portion and a relatively thicker portion on the dielectric layer wherein an opening is formed on the thinner portion; and

partially etching the dielectric layer to form a trench and a via hole of a dual damascene structure in the dielectric layer in a single etching step while the relatively thinner portion and the relatively thicker portion of the mask layer is selectively used as an etching mask.

14. The dual damascene process according to claim 13 wherein before the step of forming the mask layer on the dielectric layer, the dual damascene

process further comprises a step of forming a reversed trench organic ARC layer on the dielectric layer wherein the mask layer covers the reversed trench organic ARC layer.

15. The dual damascene process according to claim 14 wherein the reversed trench organic ARC layer is formed by a reversed trench lithography procedure so that the reversed trench organic ARC layer has a relatively thicker portion corresponding to a position of the trench and a relatively thinner portion.

16. The dual damascene process according to claim 15 wherein the relatively thinner portion and the relatively thicker portion of the mask layer corresponds to the relatively thicker portion and the relatively thinner portion of the reversed trench organic ARC layer, respectively.

17. The dual damascene process according to claim 14 wherein the mask layer comprises a Si-rich ARC layer having an etching rate ranging from 1/6 to 1/10 of an etching rate of the reversed trench organic ARC layer.

18. The dual damascene process according to claim 17 wherein the Si-rich ARC layer is a tri-layer.

19. The dual damascene process according to claim 17 wherein the mask layer further comprises a low temperature oxide layer combined with the Si-rich ARC layer.

20. The dual damascene process according to claim 17 wherein the single etching step further comprises steps of:

partially etching the reversed trench organic ARC layer through the opening of the mask layer to expose a portion of the dielectric layer

corresponding to a via-pattern;

partially etching the dielectric layer through the exposed portion of the dielectric layer along with the mask layer till the relatively thinner portion of the mask layer is entirely etched off;

using the remaining mask layer as the etching mask to partially etch the reversed trench organic ARC layer to expose another portion of the dielectric layer corresponding to a trench-pattern; and

partially etching the dielectric layer through the exposed portion of the dielectric layer along with the mask layer till the mask layer is entirely etched off.