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APPARATUS AND METHOD FOR ENABLING ELEMENTS OF A PHASE LOCKED LOOP

Field of the Invention

The present invention relates generally to radio communication transceivers and, more particularly, to an apparatus and method for enabling elements of a phase locked loop in a radio communication transceiver.

Background of the Invention

FIG. 1 illustrates, by example, a block diagram of a conventional radio communication transceiver 100 (hereinafter referred to as "transceiver"). The transceiver 100 enables a mobile or portable subscriber unit to communicate with a base station (not shown), for example, over radio frequency (RF) channels in a radio communication system (not shown). The base station thereafter provides communications with a landline telephone system (not shown) and other subscriber units. An example of a subscriber unit having the transceiver 100 is a cellular radiotelephone.

The transceiver 100 of FIG. 1 generally includes an antenna 101, a duplex filter 102, a receiver 103, a transmitter 105, a reference frequency signal source 107, a receive (Rx) phase locked loop (PLL) frequency synthesizer 108, a transmit (Tx) PLL frequency synthesizer 109, a processor 110, an information source 106, and an information sink 104.

The interconnection of the blocks of the transceiver 100 and operation thereof is described as follows. The antenna 101 receives a RF signal 119 from the base station for filtering by the duplex filter 102 to produce an RF received signal at line 111. The duplex filter 102 provides frequency selectivity to separate the RF received signal at line 111 and the RF transmit signal at line 113. The receiver 103 is coupled to receive the RF received signal at line 111 and operative to produce a received baseband signal at line 112 for

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the information sink 104. The reference frequency signal source 107 provides a reference frequency signal at line 115. The Rx PLL frequency synthesizer 108 is coupled to receive the reference frequency signal at line 115 and information on a data bus 118 and operative to produce a receiver tune signal at line 116 to tune the receiver 103 to a particular RF channel. Likewise, the Tx PLL frequency synthesizer 109 is coupled to receive the reference frequency signal at line 115 and information on the data bus 118 and operative to produce a transceiver tune signal at line 117 to tune the transmitter 105 to a particular RF channel. The processor 110 controls the operation of the Rx PLL frequency synthesizer 108, the Tx PLL frequency synthesizer 109, the receiver 103, and the transmitter 105 via the data bus 118. The information source 106 produces a baseband transmit signal at line 114. The transmitter 105 is coupled to receive the baseband transmit signal at line 114 and operative to produce the RF transmit signal at line 113. The duplex filter 102 filters the RF transmit signal at line 113 for radiation by the antenna 101 as a RF signal 120.

The RF channels in a cellular radiotelephone system, for example, include voice and signaling channels for transmitting and receiving (hereinafter referred to as "transceiving") information between the base station and the subscriber units. The voice channels are allocated for transceiving voice information. The signaling channels, also referred to as control channels, are allocated for transceiving data and signaling information. It is through these signaling channels that the subscriber units gain access to the cellular radiotelephone system and are assigned a voice channel for further communication with the landline telephone system. In cellular radiotelephone systems capable of transceiving wide band data on the signaling channels, the frequency spacing of the signaling channels is a multiple of the frequency spacing of the voice channels.

In some cellular radiotelephone systems, the transceiver 100 and the base station intermittently transceive information therebetween on the signaling channel. One such system, for example, an interleaved data signaling method to synchronize the intermittent information. In this type of system, keeping the

transceiver 100 fully powered during the entire time that the transceiver 100 is tuned to the signaling channel unnecessarily drains the transceiver's battery during those times when the information is not received. Therefore, portions of the transceiver 100 can be powered off to prolong battery life when the transceiver is not transceiving information. Further, portions of the transceiver 100 can be powered off to prolong battery life when the signal quality is good enough such that further repetition of the same information is not needed. Intermittently powering on and off, i.e. enabling and disabling, the transceiver 100 during its receive operation is called discontinuous receive (DRX) mode of operation. In the DRX mode of operation, quickly enabling and disabling the portions of transceiver 100 increases the savings in battery life.

FIG. 2 illustrates, by example, a block diagram of a conventional phase locked loop (PLL) frequency synthesizer for use in the transceiver 100 of FIG. 1. The general structure of the PLL frequency synthesizer of FIG. 2 is the same for both the Rx PLL frequency synthesizer 108 and the Tx PLL frequency synthesizer 109.

The PLL frequency synthesizer 108 or 109 of FIG. 2 generally includes a reference divider 201, for discussion purposes, and a PLL 212. The PLL 212 generally includes a phase detector 202, a loop filter 203, a voltage controlled oscillator 204, and a loop divider 205. The reference divider 201 receives a reference frequency signal on line 115.

The interconnection of the blocks of the PLL frequency synthesizer 108 or 109 of FIG. 2 is described as follows. The reference divider 201 is coupled to receive the reference signal at line 115 and the data bus 118 and operative to produce a divided reference frequency signal at line 206. The phase detector 202 is coupled to receive a divided reference frequency signal at line 206 and a feedback signal at line 209, and operative to produce a phase error signal at line 207. The loop filter 203 is coupled to receive the phase error signal 207, and operative to produce a filtered signal at line 208. The voltage controlled oscillator 204 is coupled to receive the filtered signal at line 208 and operative to produce an output

frequency signal at line 116 or 117. The loop divider 205 is coupled to receive the output frequency signal at line 116 or 117, and operative to produce the feedback signal at line 209. The loop divider 205 and the reference divider 201 are coupled to receive programming information at the data bus 118.

The operation of the PLL frequency synthesizer 108 or 109 of FIG. 2 is described as follows. The PLL 212 is a circuit which produces the output frequency signal at line 116 or 117 synchronized to the reference frequency signal at line 115. The output frequency signal at line 116 or 117 is synchronized or "locked" to the reference frequency signal at line 115 when the frequency of the output frequency signal at line 116 or 117 has a predetermined frequency relationship to the frequency of the reference frequency signal at line 115. Under locked conditions, the 212 PLL typically provides a constant phase difference between the reference frequency signal at line 115 and the output frequency signal at line 116 or 117. The constant phase difference may assume any desired value including zero. Should a deviation in the desired phase difference of such signals develop, i.e., should a phase error at line 207 develop due to, e.g., variation in either the frequency of the reference frequency signal at line 115 or programmable parameters of the PLL via the data bus 118, the PLL adjusts the frequency of the output frequency signal at line 116 or 117 to drive the phase error at line 207 toward the value of the constant phase difference.

A problem exists when a PLL frequency synthesizer is re-enabled after a period of being disabled, such as occurs in the DRX mode. Assume, ideally, that the voltage on the frequency control line to the VCO remained a constant value throughout a disable/re-enable sequence. Even so, the frequency of the VCO when it is re-enabled may temporarily be different from the frequency it was just before it was disabled. This temporary difference lasts as long as is required for the VCO and its bias circuitry to stabilize. The VCO is typically very sensitive to power supply noise and spurious signals and therefore often employs a superfilter or considerable capacitive filtering in its power supply connection. A significant amount of time may be needed for the

VCO bias condition to settle to its steady state value. During this time the PLL will detect the phase and frequency error and drive the control line to correct the error. This correction will cause the VCO to overshoot its pre-disabled frequency even after the VCO bias condition reaches steady state. The resulting overshoot takes time to settle and more time is needed for the loop to lock than if the erroneous correction had been avoided.

One solution provided by the prior art is to minimize relock time in the DRX mode by keeping the VCO portion of the PLL enabled continuously while disabling the remainder of the PLL. However, a disadvantage of this solution is that the VCO draws a significant portion of the PLL current drain and the current savings in the DRX mode is diminished.

Another solution provided by the prior art is to operate the VCO discontinuously. However, a disadvantage of this solution is that the finite turn-on time of the VCO superfilter and/or bias current is ignored in the turn-on recovery scheme of the PLL. Furthermore, this solution causes power supply noise and spurious signals to be coupled to the output of the PLL.

Accordingly, there is a need for an apparatus and method for enabling elements of a phase locked loop which results in a fast lock time for the phase locked loop.

Brief Description of the Drawings

FIG. 1 illustrates a block diagram of a conventional radio communication transceiver.

FIG. 2 illustrates a block diagram of a conventional phase locked loop frequency synthesizer for use in the radio communication transceiver of FIG. 1.

FIG. 3 illustrates a block diagram of a phase locked loop for use in the radio communication transceiver of FIG. 1 in accordance with the present invention.

FIG. 4 illustrates a first graph representing an output frequency signal versus time, and a second graph representing an output voltage signal versus time, each signal represented in the

phase locked loop of FIG. 3 in accordance with the present invention.

FIG. 5 illustrates a flow chart describing the steps for enabling elements of the phase locked loop of FIG. 3.

Detailed Description of a Preferred Embodiment

In accordance with the present invention, the foregoing need is substantially met by an apparatus and method for enabling elements of a phase locked loop (PLL). According to the present invention, the PLL includes a plurality of elements. Each element is capable of being enabled and disabled responsive to a control signal. Each element produces an output signal. Each element has a response time defined by the difference in time between a first time at which the element is enabled and a second time, occurring after the first time, at which the output signal of the element reaches a steady state condition. A first element of the plurality of elements, having a first response time is enabled at the first time responsive to a first control signal. A second element of the plurality of elements, having a second response time less than the first response time, is enabled responsive to the first response time and a second control signal. The present invention advantageously provides fast lock time for the PLL.

The present invention can be more fully described with reference to FIGS. 3-5, wherein FIG. 3 illustrates a block diagram of a phase locked loop for use in the radio communication transceiver of FIG. 1 in accordance with the present invention. The general structure and operation of the PLL 300 is similar to the conventional PLL 212 of FIG. 2, except for the addition of a controller 301. The controller 301 is coupled to receive a PLL state control signal on the data bus 118 and operative to produce a first control signal at line 302 and a second control signal at line 303. The controller 301 enables a first element of the plurality of elements, having a first response time, at the first time responsive to the first control signal at line 302, and enables a second element of the plurality of elements, having a second response time less

than the first response time, responsive to the first response time and the second control signal.

According to a preferred embodiment of the present invention, the first element of the plurality of elements is a voltage controlled oscillator.

According to the preferred embodiment of the present invention, the second element of the plurality of elements is a loop divider. Alternatively the second element of the plurality of elements may be the phase detector 205 or the loop filter 203.

According to the preferred embodiment of the present invention the first response time is fixed. Alternatively, the first response time may also be variable. The controller 301 is coupled to receive an indication of the first response time at line 304 and operative to control the second control signal at line 303 responsive to the indication of the first response time.

FIG. 4 illustrates a first graph 400 representing an output frequency signal 116 or 117 versus time, and a second graph 401 representing a loop filter output voltage signal 208 versus time. The curves 403 and 405 represent the response of the prior art when PLL 212 is enabled. The curves 402 and 404 represent the response of PLL 300 when it is enabled with control signals 302 and 303 in accordance with the present invention. Graph 400 illustrates the output frequency signal 116 or 117 of the VCO 204 versus time. The second graph 401 represents the output voltage signal at line 208 of the loop filter 203 versus time. The time axis includes times t1-t4 which correspond between the first graph 400 and the second graph 401.

At time t1, PLL 212 and PLL 300 are both disabled. The output frequency signal 116 or 117 follows curve 406 and the frequency of the VCO output frequency signal 116 or 117 decreases as time increases until the frequency reaches zero between t1 and t2. Curve 406 is identical for PLL 212 and PLL 300 because the VCO 204 is disabled in both PLL's at time t1. Between time t1 and t2, the loop filter output voltage 208 is being held constant by the capacitance of the loop filter 203 as indicated by the curve 404 between time t1 and t2.

The curves 402 and 403, both beginning at time t2 are produced as follows. To produce curve 403, the PLL frequency synthesizer 300 is enabled, at time t2, according to the prior art. Prior art has the loop divider 205, the VCO 204, the loop filter 203 and the phase detector 202 enabled at the same time. The phase detector 202 would detect nearly instantaneously at time t2 that the frequency of the output frequency signal 204 is lower than the frequency corresponding to curve 407. A phase error signal 207, shown as curve 405 in second graph 401, would be produced to try to correct the frequency of the output frequency signal 204. The result would be that the frequency of the output frequency signal 204 would follow curve 403, which overshoots the frequency shown be curve 407. The overshoot exists because the corrective action of the PLL overcompensates for the slow response time of the output frequency signal 204. The frequency of the output frequency signal 204 using the prior art method follows curve 403 and does not settle to its final value until time t4.

The novel PLL 300 enables only the VCO 204 at time t2 with control signal 302. Control signal 303 keeps the other elements of the PLL 300 disabled. In the novel PLL 300, the phase detector 202 does not produce a phase error signal at line 207, as shown by curve 404 in graph 401. The result is that the frequency of the output frequency signal 204 follows curve 402 in graph 400. In the novel PLL 300, curve 402 does not overshoot and reaches its final frequency value at approximately t3, corresponding to the same frequency value as curve 407. In the novel PLL 300, the other elements of the PLL 300 are enabled at t3. The phase detector does not produce a large phase error signal 207 and the frequency of the output frequency signal 204 stabilizes in a very short time after time t3. In contrast, the prior art PLL 212 requires until time t4 to stabilize its output frequency, as shown by curve 403. The locktime of the PLL 300 has been shortened, over the prior art, by the difference in time represented by t4-t3.

FIG. 5 illustrates a flow chart describing the steps for enabling elements of the phase locked loop of FIG. 3. The flowchart begins at step 500. At step 501 a radio frequency signal is received to produce a received signal. At step 502 a radio frequency

receiver is enabled responsive to the received signal. The flowchart ends at step 506. The step of enabling the radio frequency receiver 502 includes steps 503-505. At step 503, the elements of the PLL frequency synthesizer is enabled. At step 504, a first element of the plurality of elements, having a first response time, is enabled at a first time responsive to a first control signal. At step 505, a second element of the plurality of elements, having a second response time less than the first response time, is enabled responsive to the first response time and a second control signal.

Step 503, in FIG. 5, enables the elements of the PLL frequency synthesizer in a unique way described by steps 504 and 505. At step 504, the element of the PLL frequency synthesizer with the slowest response time is enabled first. In the preferred embodiment, the VCO has the slowest response time and that is why it is enabled first with the first control signal which corresponds to control signal 302. At step 505, the second element with a response time less than the VCO 204 is enabled. In the preferred embodiment, the second element is the loop divider 205. The control signal 303 enables the loop divider 205 responsive to the first response time, which means that the control signal 303 is delayed until the VCO 204 has substantially reached a steady state frequency before the loop divider 205 is enabled. By enabling the VCO 204 first and waiting to enable the other elements of the PLL 300, the frequency of the output frequency signal 116 or 117 is prevented from overshooting, thereby reducing the locktime of the PLL 300.

In accordance with the present invention, the foregoing need is substantially met by an apparatus and method for enabling elements of a phase locked loop (PLL). According to the present invention, the PLL includes a plurality of elements. Each element is capable of being enabled and disabled responsive to a control signal. Each element produces an output signal. Each element has a response time defined by the difference in time between a first time at which the element is enabled and a second time, occurring after the first time, at which the output signal of the element reaches a steady state condition. A first element of the plurality of elements, having a first response time is enabled at the

first time responsive to a first control signal. A second element of the plurality of elements, having a second response time less than the first response time, is enabled responsive to the first response time and a second control signal. The present invention advantageously provides fast lock time for the PLL.

While the present invention has been described with reference to illustrative embodiments thereof, it is not intended that the invention be limited to these specific embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit and scope of the invention as set forth in the appended claims.

What is claimed is:

Claims

1. In a phase locked loop (PLL) including a plurality of elements, each element producing an output signal, each element having a response time defined by the difference in time between a first time (t2) at which the element is enabled and a second time (t3), occurring after the first time, at which the output signal of the element reaches a steady state condition, a method for enabling the plurality of elements of the PLL comprising the steps of:

enabling a first element of the plurality of elements, having a first response time, at the first time (t2) responsive to a first control signal; and

enabling a second element of the plurality of elements, having a second response time less than the first response time, responsive to the first response time and a second control signal.

2. A method according to claim 1 wherein the first element of the plurality of elements is a voltage controlled oscillator .

3. A method according to claim 1 wherein the second element of the plurality of elements is a loop divider.

4. A method according to claim 1 wherein the second element of the plurality of elements is a phase detector.

5. A method according to claim 1 wherein the second element of the plurality of elements is a loop filter.

6. A method according to claim 1 wherein the first response time is fixed.

7. A method according to claim 1 wherein the first response time is variable.

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8. A method according to claim 1 further comprising the steps of:

monitoring an indication of the first response time; and

controlling the second control signal responsive to the monitored indication of the first response time.

9. In a phase locked loop (PLL) having an enabled and a disabled state responsive to a PLL state control signal, the PLL including a plurality of elements , each element producing an output signal, each element having a response time defined by the difference in time between a first time (t2) at which the element is enabled and a second time (t3), occurring after the first time, at which the output signal of the element reaches a steady state condition, an apparatus for enabling the plurality of elements of the PLL comprising:

a controller coupled to receive the PLL state control signal and operative to produce first and second control signals, wherein the controller enables a first element of the plurality of elements, having a first response time, at the first time (t2) responsive to the first control signal, and enables a second element of the plurality of elements, having a second response time less than the first response time, responsive to the first response time and the second control signal.

10. An apparatus according to claim 9 wherein the controller is coupled to receive an indication of the first response time and operative to control the second control signal responsive to the indication of the first response time.

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