MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES AND SENSE AMPLIFIER THEREFOR

Abstract of the Disclosure

A memory (400) includes a sense amplifier (500) formed with current-to-voltage converters (512, 513) connected to multiple bit lines, with a common current source (548) forming a current reference, and a common latching comparator (530). A column decode select circuit (515) which selects one of the multiple bit lines is interposed between the current-to-voltage converters (512, 513) and an input of the latching comparator (530) . The distribution of the components of the sense amplifier (500) allows operation at low power supply voltages. The sense amplifier (500) uses a clamp and a loading device to establish a first discharge rate on a reference input of the latching comparator (530). The state of the selected memory cell establishes a second discharge rate on another input of the latching comparator (530), which is greater or less than the first discharge rate depending on the state of the memory cell. Portions of the comparator (530) also double as latches during a program mode.

Figure 5 accompanies this abstract.