

CLAIMS

What is claimed is:

1. A method implemented in a coding device, the method comprising:
parsing, by a processor of the computing device, a bitstream to obtain a prediction block and a transformed residual block corresponding to the prediction block;
determining, by the processor, a type of spatial varying transform (SVT) that was used to generate the transformed residual block;
determining, by the processor, a position of the SVT relative to the transformed residual block;
determining, by the processor, an inverse of the SVT based on the position of the SVT;
applying, by the processor, the inverse of the SVT to the transformed residual block to produce a reconstructed residual block; and
combining, by the processor, the reconstructed residual block with the prediction block to reconstruct an image block.
2. The method of claim 1, wherein the type of the SVT is a SVT vertical (SVT-V) type or a SVT horizontal (SVT-H) type.
3. The method of any of claims 1 to 2, wherein the SVT-V type includes a height that equals a height of the transformed residual block and a width that is half a width of the transformed residual block, and the SVT-H type includes a height that is half the height of the transformed residual block and a width that is equal to a width of the transformed residual block.
4. The method of any of claims 1 to 3, further comprising parsing an `svt_type_flag` from the bitstream to determine a type of the SVT.
5. The method of any of claims 1 to 4, further comprising determining a type of SVT by inference when only one type of SVT is allowed for the residual block.
6. The method of any of claims 1 to 5, further comprising parsing a position index from the bitstream to determine a position of the SVT.

7. The method of any of claims 1 to 6, wherein a position index contains a binary code indicating the position from a set of candidate positions determined according to a candidate position step size (CPSS).
8. The method of any of claims 1 to 7, wherein a most probable position of the SVT is assigned a least number of bits in the binary code indicating the position index.
9. The method of any of claims 1 to 8, wherein a position of the SVT is inferred by the processor when a single candidate position is available for the SVT transform.
10. The method of any of claims 1 to 9, wherein a position of the SVT is inferred by the processor when the residual block was generated by template matching in an inter-prediction mode.
11. The method of any of claims 1 to 10, wherein an inverse Discrete Sine Transform (DST) is employed for a SVT vertical (SVT-V) type transform positioned at a left boundary of the residual block.
12. The method of any of claims 1 to 11, wherein an inverse DST is employed for a SVT horizontal (SVT-H) type transform positioned at a top boundary of the residual block.
13. The method of any of claims 1 to 12, wherein an inverse Discrete Cosine Transform (DCT) is employed for a SVT-V type transform positioned at a right boundary of the residual block.
14. The method of any of claims 1 to 13, wherein an inverse DCT is employed for a SVT-H type transform positioned at a bottom boundary of the residual block.
15. The method of any of claims 1 to 14, further comprising horizontally flipping samples in the reconstructed residual block prior to combining the reconstructed residual block with the prediction block when a right side neighbor of a coding unit associated with the reconstructed

residual block has been reconstructed and a left side neighbor of the coding unit has not been reconstructed.

16. A method implemented in a coding device, the method comprising:
receiving a video signal from a video capture device, the video signal including an image block;
generating, by a processor of the computing device, a prediction block and a residual block to represent the image block;
selecting, by the processor, a transform algorithm for a spatial varying transform (SVT) based on a position of the SVT relative to the residual block;
converting, by the processor, the residual block into a transformed residual block using the SVT that was selected;
encoding, by the processor, a type of the SVT into a bitstream;
encoding, by the processor, a position of the SVT into the bitstream; and
encoding, by the processor, the prediction block and the transformed residual block into the bitstream for transmission to a decoder.

17. The method of claim 16, wherein the type of the SVT is a SVT vertical (SVT-V) type or a SVT horizontal (SVT-H) type.

18. The method of any of claims 16 to 17, wherein the SVT-V type includes a height that equals a height of the residual block and a width that is half a width of the residual block.

19. The method of any of claims 16 to 18, wherein the SVT-H type includes a height that is half the height of the residual block and a width that is equal to a width of the residual block.

20. The method of any of claims 16 to 19, wherein the position of the SVT is encoded in a position index.

21. The method of any of claims 16 to 20, wherein a position index contains a binary code indicating the position from a set of candidate positions determined according to a candidate position step size (CPSS).
22. The method of any of claims 16 to 21, wherein a most probable position of the SVT is assigned as a least number of bits in the binary code indicating the position index.
23. The method of any of claims 16 to 22, wherein a Discrete Sine Transform (DST) algorithm is employed by the processor for a SVT vertical (SVT-V) type transform positioned at a left boundary of the residual block.
24. The method of any of claims 16 to 23, wherein a DST algorithm is selected by the processor for a SVT horizontal (SVT-H) type transform positioned at a top boundary of the residual block.
25. The method of any of claims 16 to 24, wherein a Discrete Cosine Transform (DCT) algorithm is selected by the processor for a SVT-V type transform positioned at a right boundary of the residual block.
26. The method of any of claims 16 to 25, wherein a DCT algorithm is selected by the processor for a SVT-H type transform positioned at a bottom boundary of the residual block.
27. The method of any of claims 16 to 26, further comprising horizontally flipping, by the processor, samples in the residual block prior converting, by the processor, the residual block into the transformed residual block when a right side neighbor of a coding unit associated with the residual block has been encoded and a left side neighbor of the coding unit has not been encoded.
28. A coding apparatus, comprising:
a receiver configured to receive a picture to encode or to receive a bitstream to decode;

a transmitter coupled to the receiver, the transmitter configured to transmit the bitstream to a decoder or to transmit a decoded image to a display;

a memory coupled to at least one of the receiver or the transmitter, the memory configured to store instructions; and

a processor coupled to the memory, the processor configured to execute the instructions stored in the memory to perform the method in any of claims 1 to 27.

29. The coding apparatus of claim 28, further comprising a display configured to display an image.

30. A system, comprising:

an encoder; and

a decoder in communication with the encoder, wherein the encoder or the decoder includes the coding apparatus of any of claims 28 to 29.

31. A means for coding, comprising:

receiving means configured to receive a picture to encode or to receive a bitstream to decode;

transmission means coupled to the receiving means, the transmission means configured to transmit the bitstream to a decoder or to transmit a decoded image to a display means;

storage means coupled to at least one of the receiving means or the transmission means, the storage means configured to store instructions; and

processing means coupled to the storage means, the processing means configured to execute the instructions stored in the storage means to perform the method in any of claims 1 to 27.

CLAIMS

1. A method implemented in a coding device, the method comprising: parsing, by a processor of the coding device, a bitstream to obtain a prediction block and a transformed residual block corresponding to the prediction block;
determining, by the processor, a type of spatial varying transform (SVT) that was used to generate the transformed residual block;
determining, by the processor, a position of a block of the SVT relative to the transformed residual block;
determining, by the processor, an inverse of the SVT based on the position of the block of the SVT;
applying, by the processor, the inverse of the SVT to the transformed residual block to produce a reconstructed residual block; and
combining, by the processor, the reconstructed residual block with the prediction block to reconstruct an image block.
2. The method of claim 1, wherein the type of the SVT is a SVT vertical (SVT- V) type or a SVT horizontal (SVT-H) type.
3. The method of claim 2, wherein the S VT-V type includes a height that equals a height of the transformed residual block and a width that is half a width of the transformed residual block, and the SVT-H type includes a height that is half the height of the transformed residual block and a width that is equal to a width of the transformed residual block.
4. The method of claim 1, further comprising parsing an svt type flag from the bitstream to determine a type of the SVT.

5. The method of claim 1, further comprising determining a type of SVT by inference when only one type of SVT is allowed for the residual transformed block.
6. The method of claim 1, further comprising parsing a position index from the bitstream to determine the position of the block of the SVT.
7. The method of claim 1, wherein a position index contains a binary code indicating the position from a set of candidate positions determined according to a candidate position step size (CPSS).
8. The method of claim 7, wherein a most probable position of the SVT is assigned a least number of bits in the binary code indicating the position index.
9. The method of claim 1, wherein the position of the block of the SVT is inferred by the processor when a single candidate position is available for the SVT transform.
10. The method of claim 1, wherein the position of the block of the SVT is inferred by the processor when the transformed residual block was generated by template matching in an inter-prediction mode.
11. A method implemented in a coding device, the method comprising:
receiving a video signal from a video capture device, the video signal including an image
block;
generating, by a processor of the coding device, a prediction block and a residual block to represent
the image block;

selecting, by the processor, a transform algorithm for a spatial varying transform (SVT) based on a position of a block of the SVT relative to the residual block;

converting, by the processor, the residual block into a transformed residual block using the SVT that was selected;

encoding, by the processor, a type of the SVT into a bitstream;

encoding, by the processor, the position of the block of the SVT into the bitstream; and encoding, by the processor, the prediction block and the transformed residual block into the bitstream for transmission to a decoder.

12. The method of claim 11, wherein a Discrete Sine Transform (DST) algorithm is employed by the processor for a SVT vertical (SVT-V) type transform positioned at a left boundary of the residual block.

13. The method of claim 11, wherein a Discrete Sine Transform (DST) algorithm is selected by the processor for a SVT horizontal (SVT-H) type transform positioned at a top boundary of the residual block.

14. The method of claim 11, wherein a Discrete Cosine Transform (DCT) algorithm is selected by the processor for a SVT vertical (SVT-V) type transform positioned at a right boundary of the residual block.

15. The method of claim 11, wherein a DCT algorithm is selected by the processor for a SVT-H type transform positioned at a bottom boundary of the residual block.

16. The method of claim 11, further comprising horizontally flipping, by the processor, samples in the residual block prior converting, by the processor, the residual block into the transformed residual block when

a right side neighbor of a coding unit associated with the residual block has been encoded and a left side neighbor of the coding unit has not been encoded.

17. A coding apparatus, comprising:

a memory storing instructions;

a processor coupled to the memory, the processor configured to execute the instructions stored in the memory to cause the coding apparatus to:

parse a bitstream to obtain a prediction block and a transformed residual block corresponding to the prediction block;

determine a type of spatial varying transform (SVT) that was used to generate the transformed residual block;

determine a position of a block of the SVT relative to the transformed residual block;

determine an inverse of the SVT based on the position of the block of the SVT;

apply the inverse of the SVT to the transformed residual block to produce a reconstructed residual block; and

combine the reconstructed residual block with the prediction block to reconstruct an image block.

18. The coding apparatus of claim 17, further comprising a display configured to display an image based on the image block.

19. A coding apparatus, comprising:

a memory storing instructions;

a processor coupled to the memory, the processor configured to execute the instructions stored in the memory to cause the coding apparatus to:

receive a video signal from a video capture device, the video signal including an image block;

generate a prediction block and a residual block to represent the image block;

select a transform algorithm for a spatial varying transform (SVT) based on a position of a block of the SVT relative to the residual block;

convert the residual block into a transformed residual block using the SVT that was selected;

encode a type of the SVT into a bitstream;

encode the position of the block of the SVT into the bitstream; and

encode the prediction block and the transformed residual block into the bitstream for transmission to a decoder.

20. The coding apparatus of claim 19, further comprising a transmitter coupled to the processor, the transmitter configured to transmit the bitstream to the decoder.