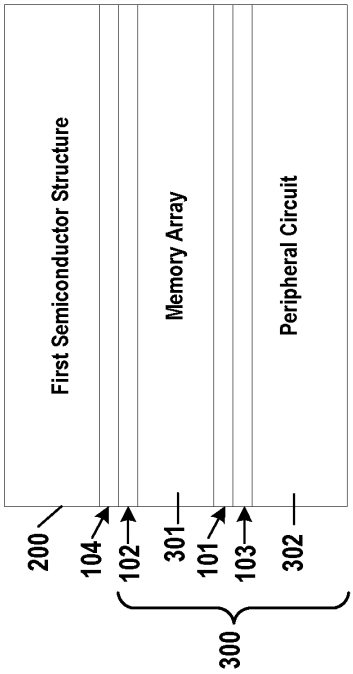

First Semiconductor Structure
Memory Array
Peripheral Circuit
200
104
102
301
101
103
302
300

FIG. 1

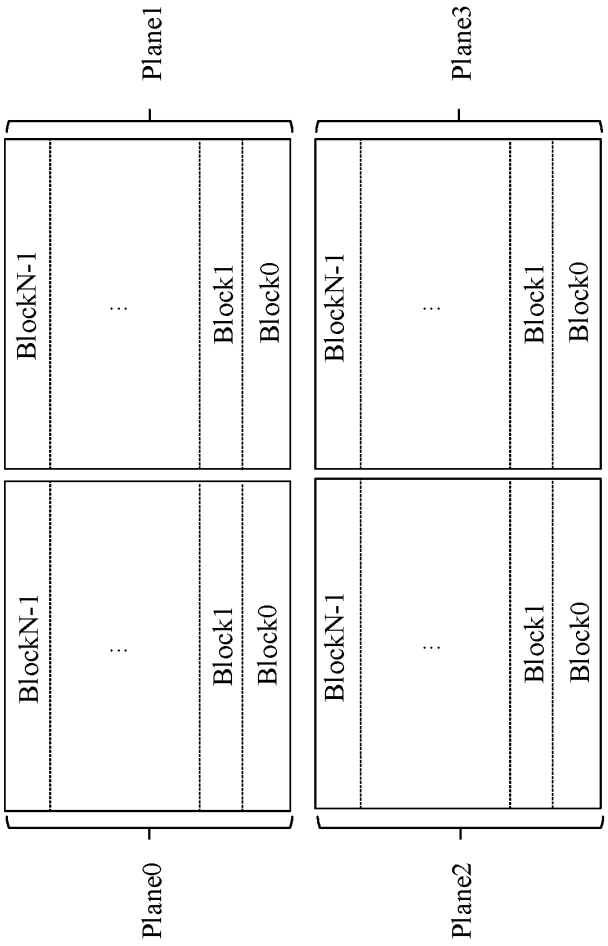


FIG. 2

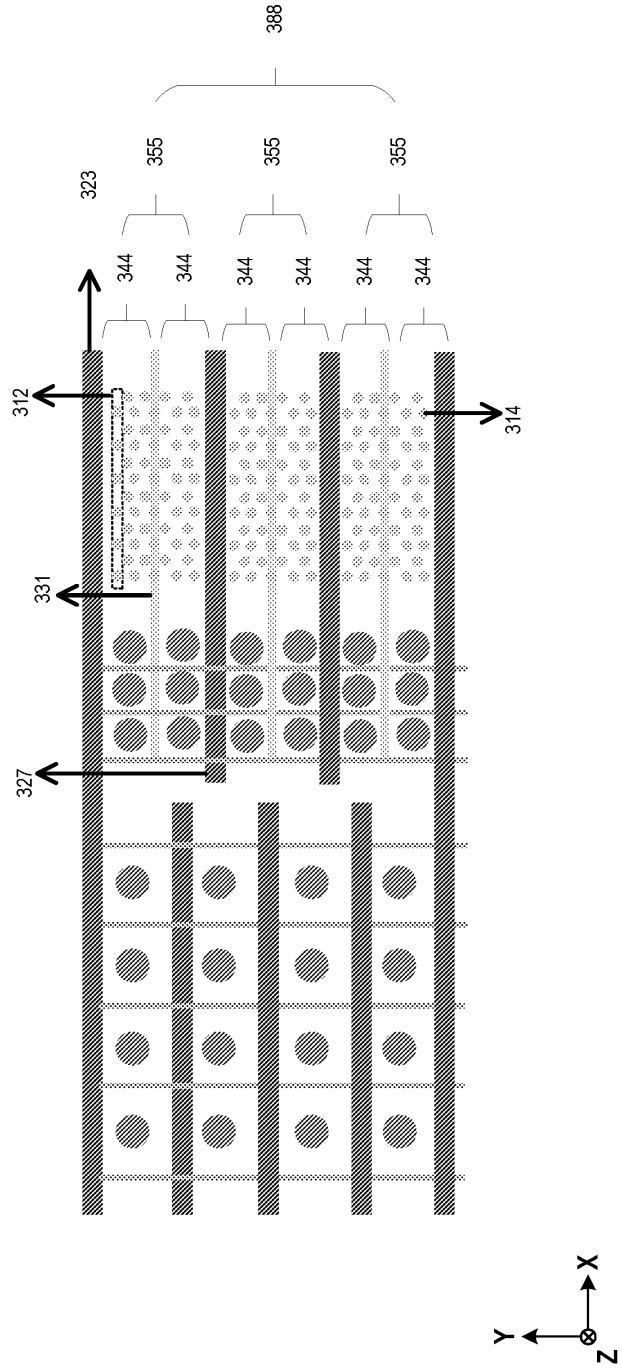


FIG. 3

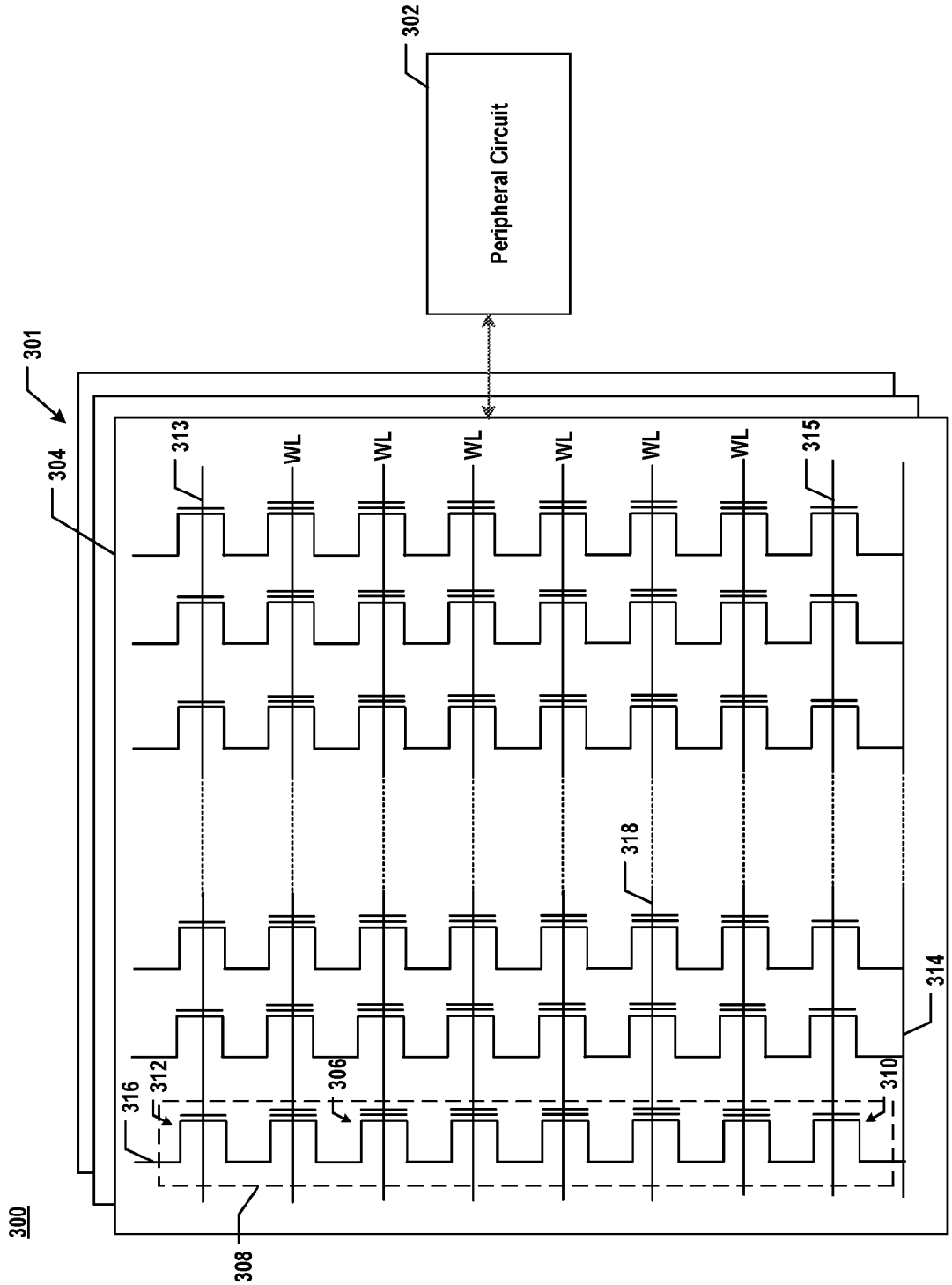

302
Peripheral Circuit
301
304
313
WL
WL
WL
WL
WL
WL
315
318
314
316
312
306
310
308
300

FIG. 4

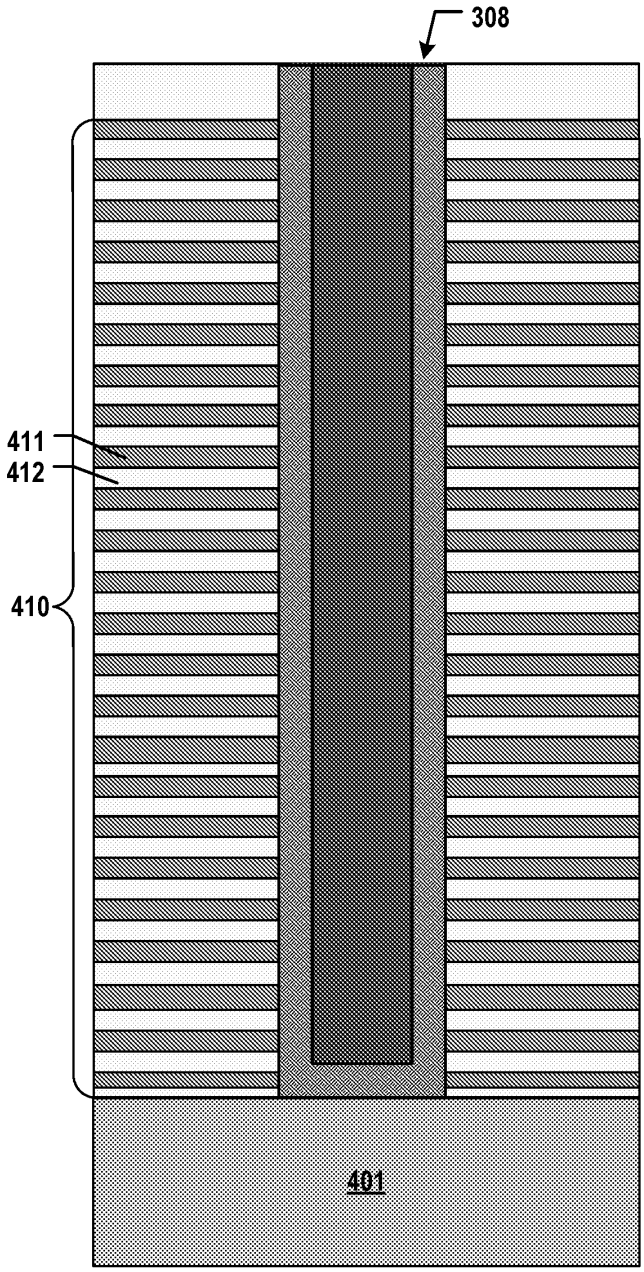


FIG. 5

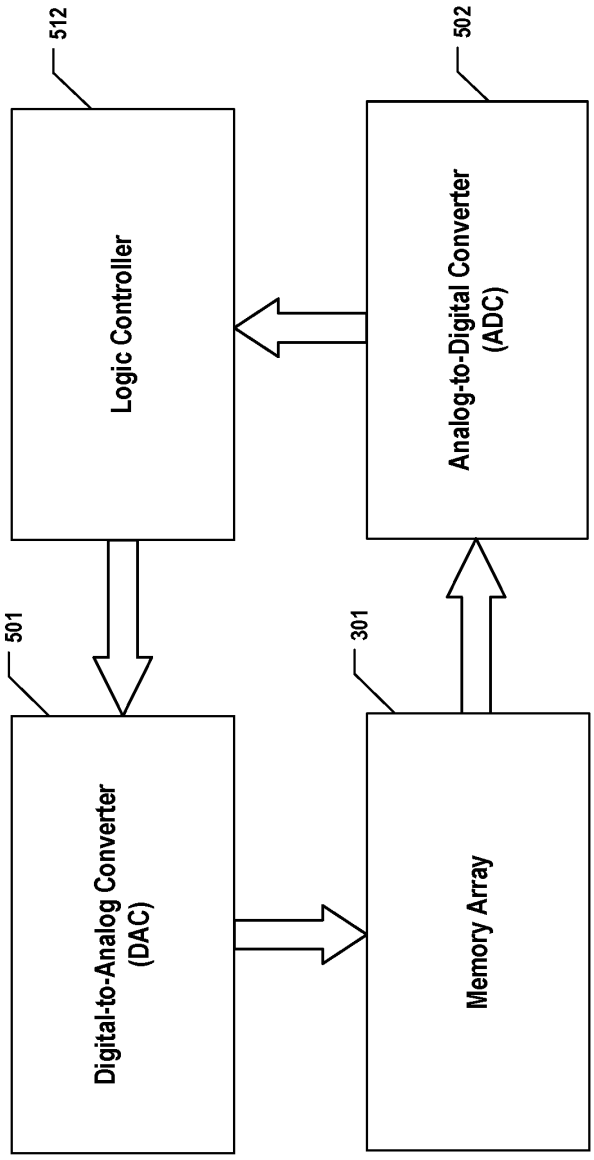

512
Logic Controller
502
Analog-to-Digital Converter (ADC)
501
Digital-to-Analog Converter (DAC)
301
Memory Array

FIG. 6

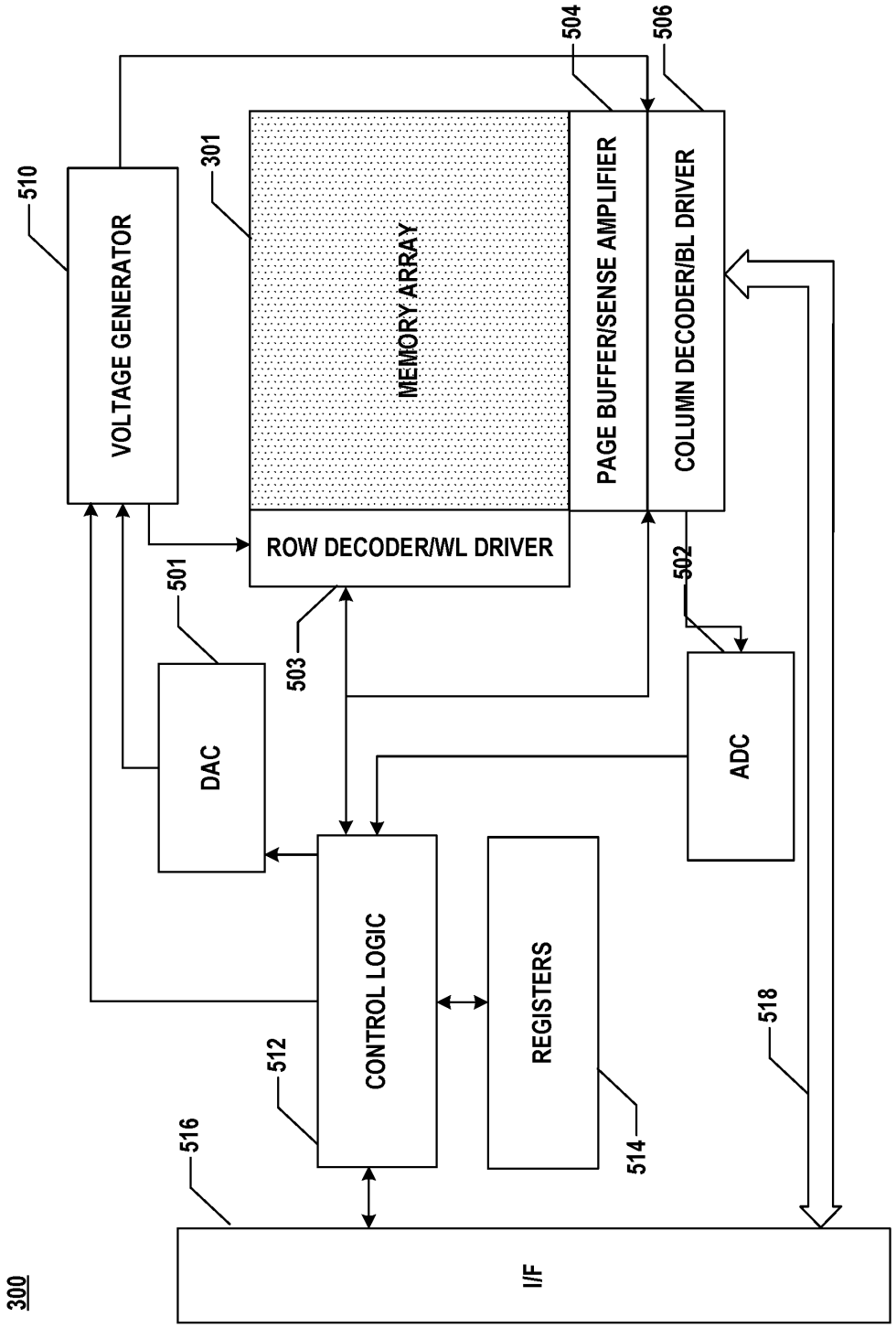

300
I/F
516
CONTROL LOGIC
512
REGISTERS
514
518
DAC
501
503
ADC
502
ROW DECODER/WL DRIVER
MEMORY ARRAY
301
VOLTAGE GENERATOR
510
PAGE BUFFER/SENSE AMPLIFIER
504
COLUMN DECODER/BL DRIVER
506

FIG. 7

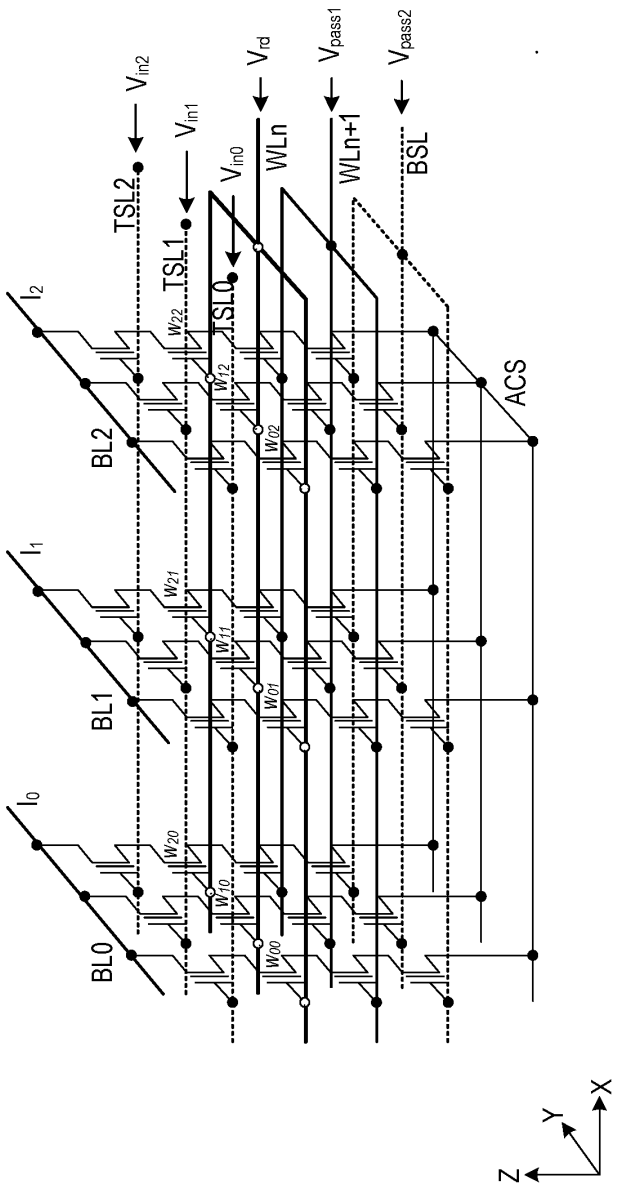

V_{in2}
V_{in1}
V_{in0}
V_{rd}
V_{pass1}
V_{pass2}
TSL2
TSL1
TSL0
WLn
WLn+1
BSL
ACS
I_2
I_1
I_0
BL2
BL1
BL0
w_{22}
w_{12}
w_{02}
w_{21}
w_{11}
w_{01}
w_{20}
w_{10}
w_{00}
Z
Y
X

FIG. 8

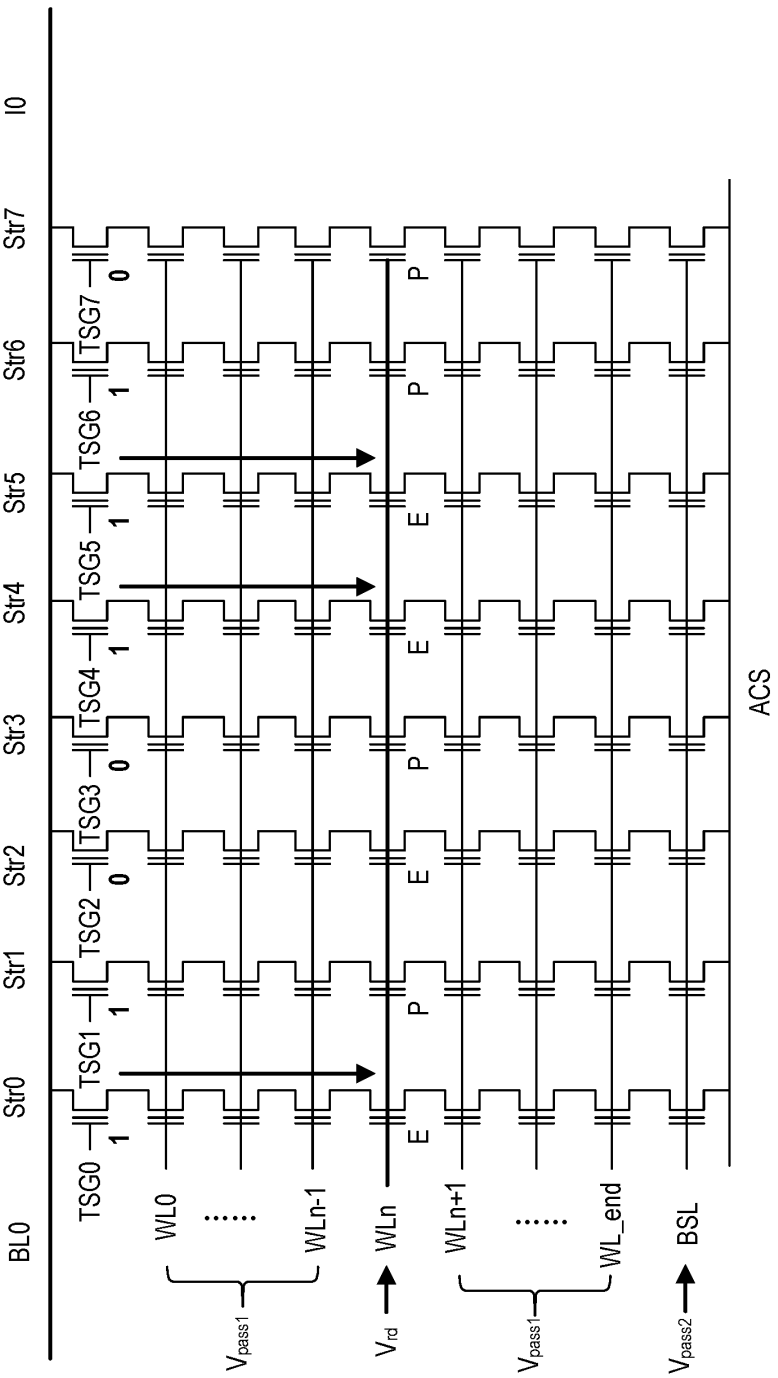

BL0
Str0
Str1
Str2
Str3
Str4
Str5
Str6
Str7
I0
TSG0
TSG1
TSG2
TSG3
TSG4
TSG5
TSG6
TSG7
1
0
E
P
WL0
WLn-1
WLn
WLn+1
WL_end
BSL
ACS
V_{pass1}
V_{rd}
V_{pass1}
V_{pass2}

FIG. 9

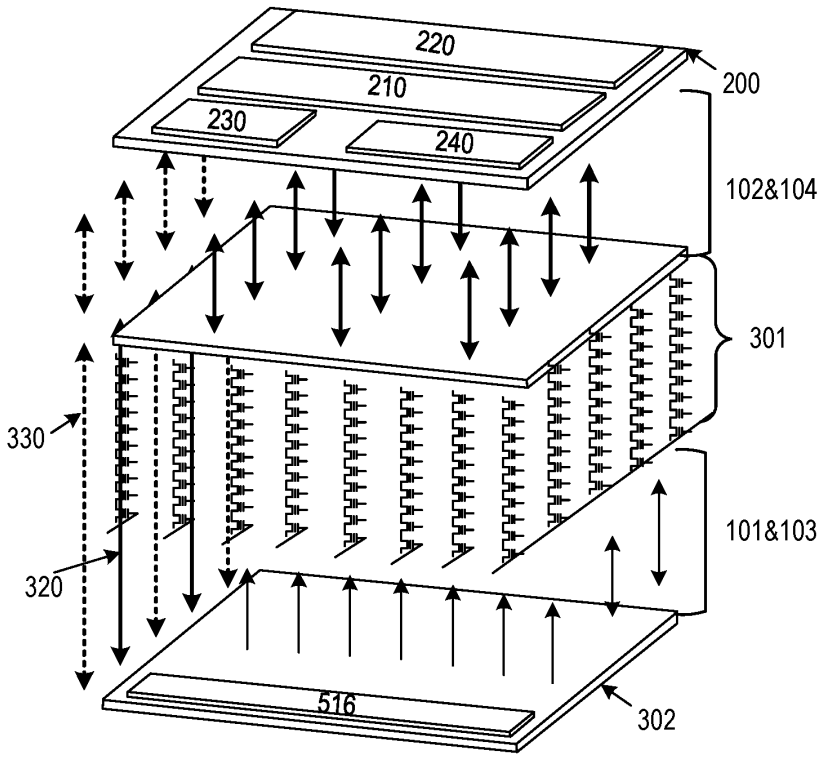


FIG. 10

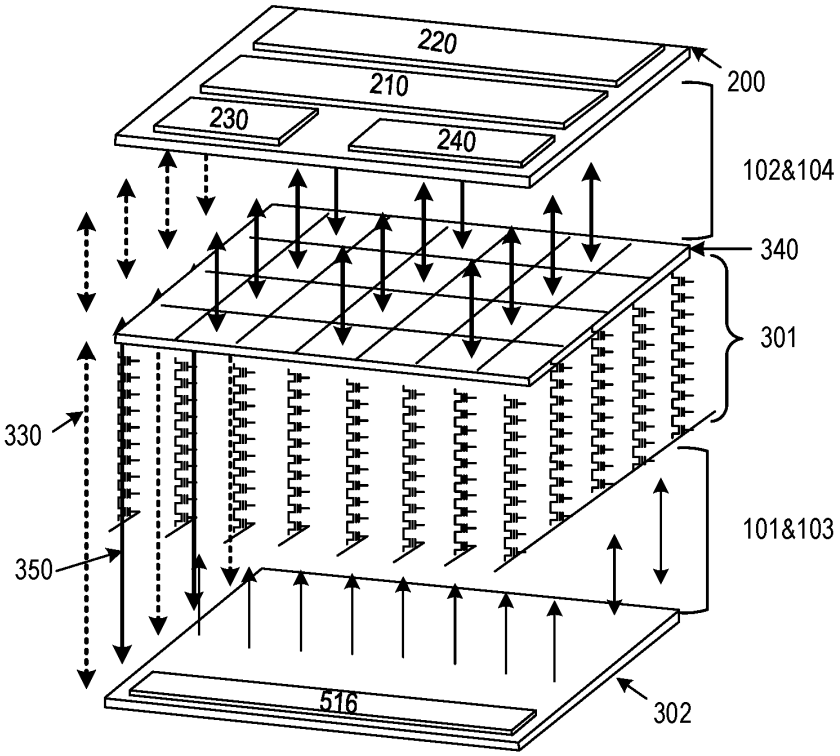


FIG. 11

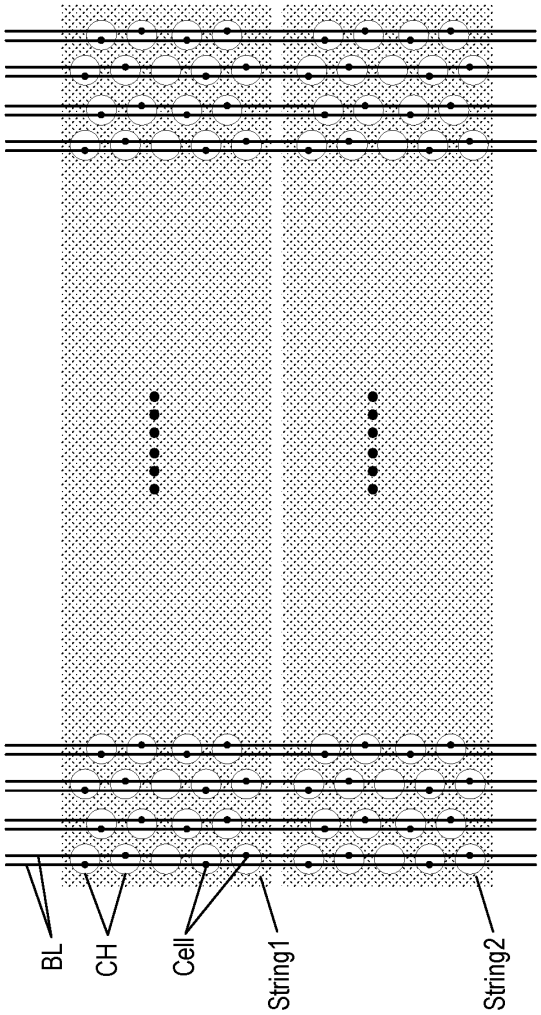


FIG. 12A

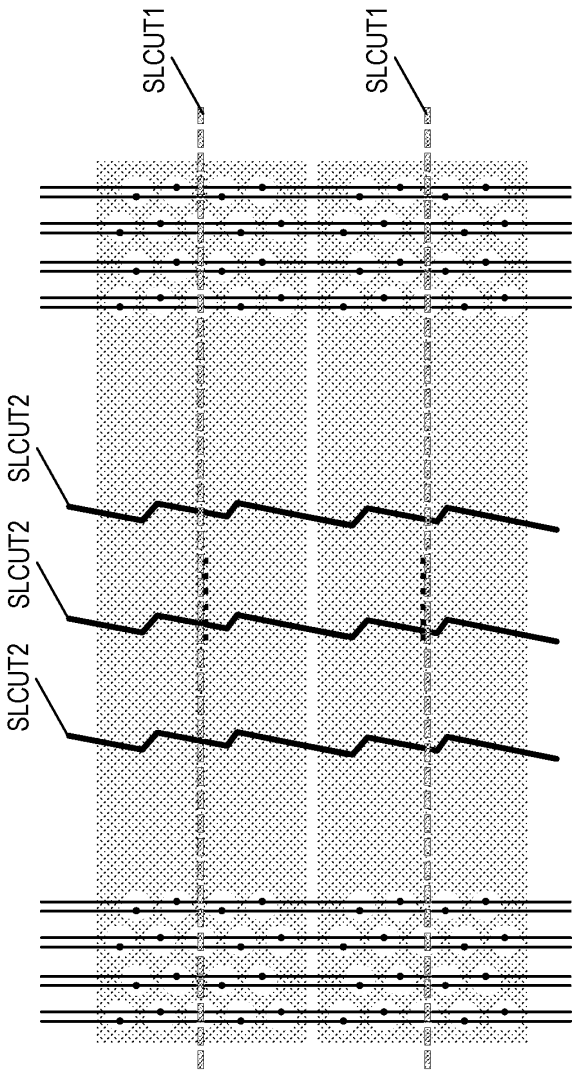


FIG. 12B

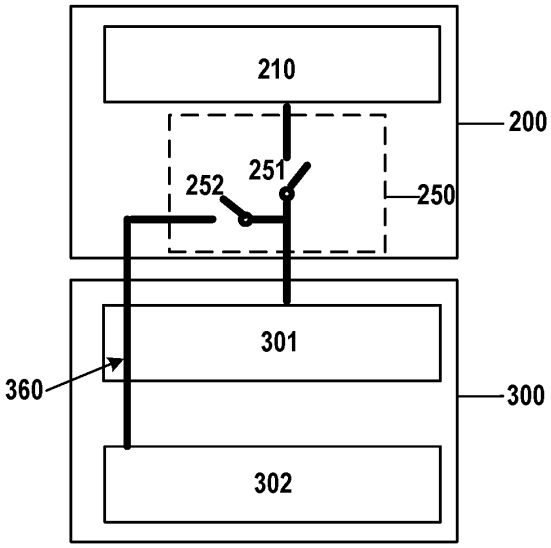


FIG. 13A

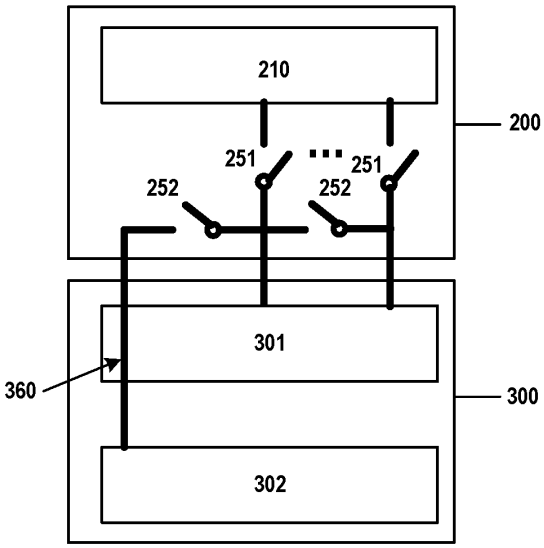


FIG. 13B

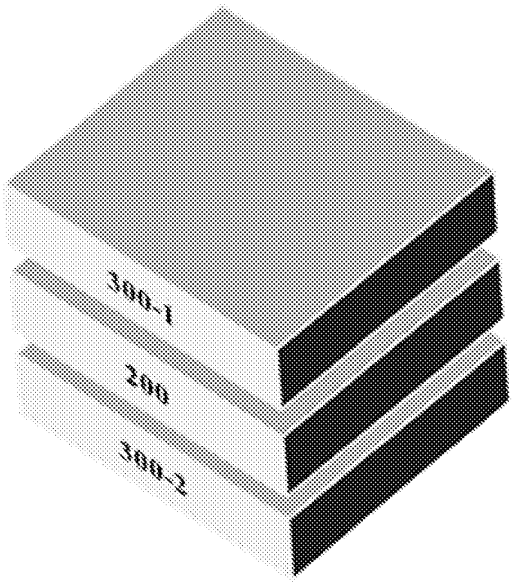


FIG. 14A

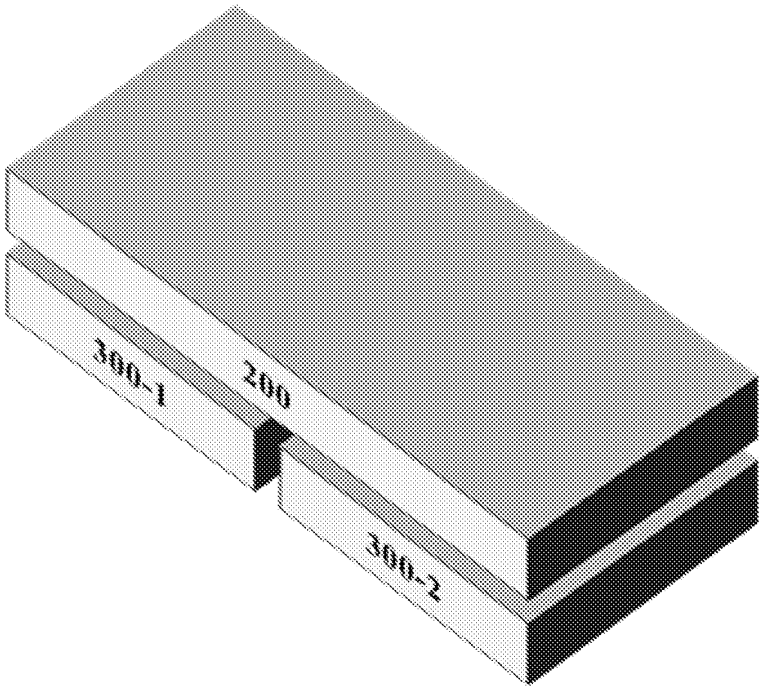


FIG. 14B

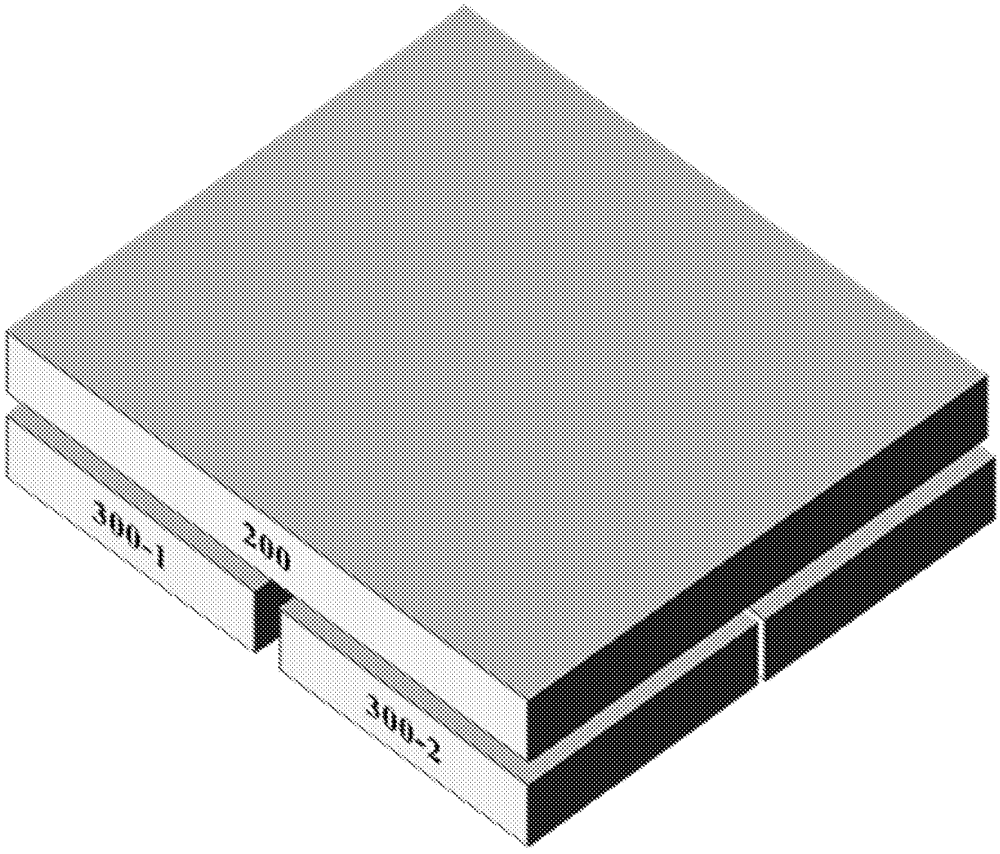


FIG. 14C

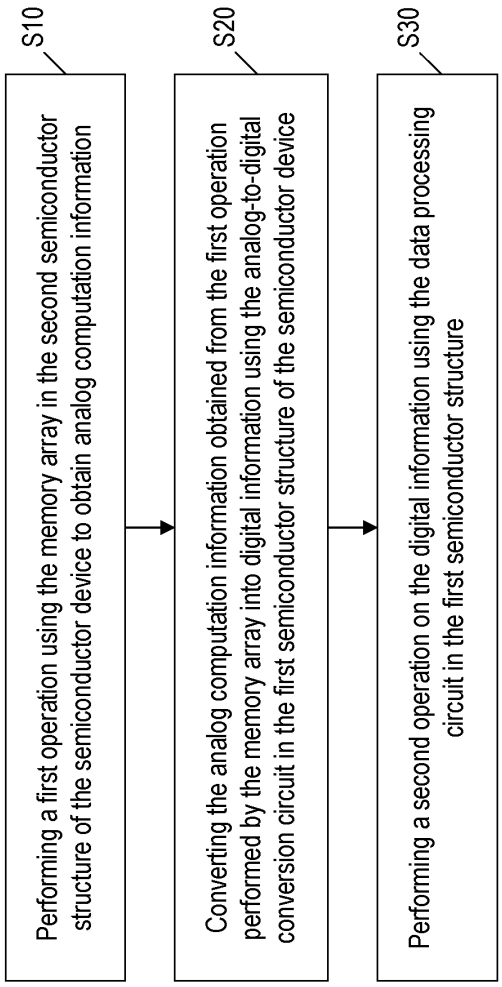

S10
Performing a first operation using the memory array in the second semiconductor structure of the semiconductor device to obtain analog computation information
S20
Converting the analog computation information obtained from the first operation performed by the memory array into digital information using the analog-to-digital conversion circuit in the first semiconductor structure of the semiconductor device
S30
Performing a second operation on the digital information using the data processing circuit in the first semiconductor structure

FIG. 15