(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 April 2002 (11.04.2002)

PCT

(10) International Publication Number
WO 02/029557 A3

(51) International Patent Classification[7]: G06F 9/38, 9/455

(21) International Application Number: PCT/US01/42533

(22) International Filing Date: 5 October 2001 (05.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/684,113 6 October 2000 (06.10.2000) US

(71) Applicants: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). **ANALOG DEVICES, INC.** [US/US]; One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 (US).

(72) Inventors: **OVERKAMP, Gregory, A.**; P.O. Box 163442, Austin, TX 78716 (US). **SINGH, Ravi, P.**; 12349 Metric Boulevard, #829, Austin, TX 78758 (US). **ROTH, Charles, P.**; 13305 Tichester Court, Austin, TX 78729 (US).

(74) Agent: **HARRIS, Scott, C.**; Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA 92122 (US).

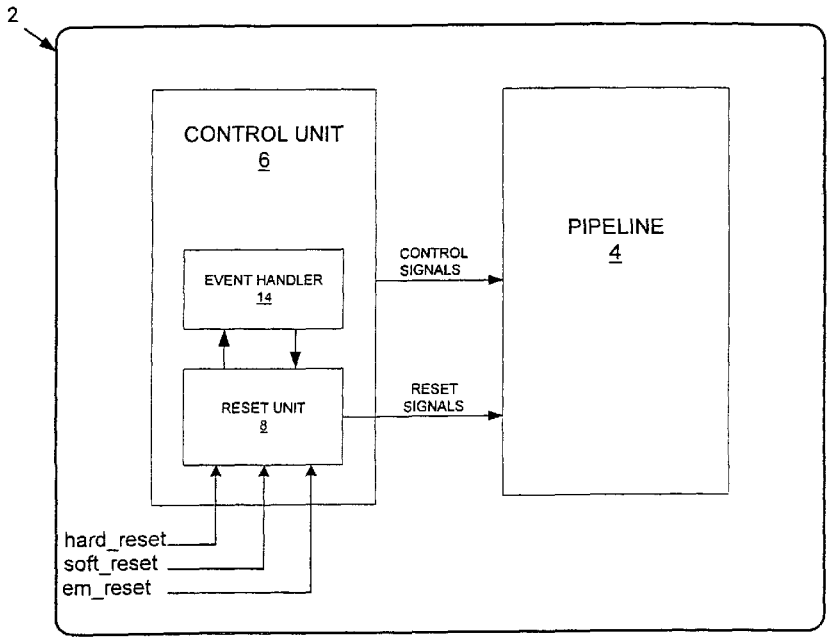
(81) Designated States *(national)*: CN, JP, KR, SG.

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
15 August 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: RESETTING A PROGRAMMABLE PROCESSOR



(57) Abstract: In one embodiment, a pipelined processor includes a reset unit that provides an output reset signal to at least one stage of the pipeline. The reset unit is adapted to detect at least a hard reset request, a soft reset request and an emulation reset request. The pipeline comprises N stages and the reset unit asserts the reset signal for at least N cycles of a clock after the reset request has been cleared. Each stage if the pipeline has a storage circuit for storing a corresponding valid bit. At least one of the storage circuits is cleared in response to the reset signal. In addition, the reset unit handles the reset request as a reset event having an assigned priority.

WO 02/029557 A3