

CLAIMS:

1. A method of forming a Light Emitting Diode (LED) precursor comprising:
 - (a) forming a first semiconducting layer comprising a Group III-nitride on a
5 substrate, the first semiconducting layer having a growth surface on an opposite side of the first semiconducting layer to the substrate;
 - (b) selectively removing a portion of the first semiconducting layer to form a mesa structure such that the growth surface of the first semiconducting layer comprises a mesa surface and a bulk semiconducting surface;
 - 10 (c) forming a monolithic LED structure on the growth surface of the first semiconducting layer such that the monolithic LED structure covers the mesa surface and the bulk semiconducting surface, the monolithic LED structure comprising a plurality of layers, each layer comprising a Group III-nitride, including:
 - a second semiconducting layer;
 - 15 - an active layer provided on the second semiconducting layer, the active layer configured to generate light; and
 - a p-type semiconducting layer provided on the active layer,wherein a potential barrier is provided between a first portion of the p-type semiconducting layer covering the mesa surface and a second portion of the p-type
20 semiconducting layer covering the bulk semiconducting surface, the potential barrier surrounding the first portion of the p-type semiconducting layer covering the mesa surface.
2. A method according to claim 1, wherein the second semiconducting layer comprises an un-doped Group III-nitride.
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3. A method according to claim 1 or claim 2, wherein the second semiconducting layer is formed on the growth surface to provide an inclined sidewall portion extending between a first portion of the second semiconducting layer on the mesa surface of the first semiconducting layer and a second portion of the second semiconducting layer on the bulk
30 semiconducting surface of the first semiconducting layer.
4. A method according to claim 3, wherein
the p-type semiconducting layer comprises Al, and is formed such that a higher concentration of Al is incorporated into an inclined sidewall portion of the p-type
35 semiconducting layer than the first portion of the p-type semiconducting layer covering the

mesa surface such that the potential barrier is formed in the inclined sidewall portion of the p-type semiconducting layer between the first portion of the p-type semiconducting layer and the second portion of the p-type semiconducting layer.

- 5 5. A method according to claim 4 wherein the inclined sidewall portion of the p-type semiconducting layer comprises p-type $\text{Al}_x\text{Ga}_{1-x}\text{N}$, wherein $2 \leq x \leq 50 \%$; and
the first portion of the p-type semiconducting layer comprises p-type $\text{Al}_y\text{Ga}_{1-y}\text{N}$,
wherein $1 \leq y \leq 15 \%$.
- 10 6. A method according to any of claims 1 to 3, wherein a portion of the p-type semiconducting layer encircling the first portion of the p-type semiconducting layer covering the mesa surface is selectively removed to expose the active layer below.
- 15 7. A method according to claim 6, wherein the portion of the p-type semiconducting layer encircling the first portion of the p-type semiconducting layer covering the mesa surface is selectively removed using an anisotropic etchant.
- 20 8. A method according to any preceding claim, wherein selectively removing portions of the first semiconducting layer to form the mesa structure comprises:
selectively forming a mesa-defining mask layer on the first surface;
selectively removing unmasked portions of first semiconducting layer to
expose the bulk semiconducting surface of the first semiconductor layer; and
removing the mesa-defining mask layer.
- 25 9. A method according to any preceding claim, wherein the first semiconducting layer comprises GaN, wherein optionally the first semiconducting layer is an n-type semiconductor.
- 30 10. A method according to any preceding claim, wherein a height of the mesa structure between the mesa surface and the bulk semiconducting surface is at least 200 nm.
- 35 11. A method of forming a LED array precursor comprising
(a) forming a first semiconducting layer comprising a Group III-nitride on a substrate, the first semiconducting layer having a growth surface on an opposite side of the first semiconducting layer to the substrate;

(b) selectively removing portions of the first semiconducting layer to form a plurality of mesa structures such that the growth surface of the first semiconducting layer comprises a plurality of mesa surfaces and a bulk semiconducting surface;

(c) forming a monolithic LED array structure on the growth surface of the first
5 semiconducting layer such that the monolithic LED array structure covers the mesa surfaces and the bulk semiconducting surface, the monolithic LED array structure comprising a plurality of layers, each layer comprising a Group III-nitride, including:
- an n-type semiconducting layer;
- an active layer provided on the n-type semiconducting layer, the active
10 layer configured to generate light; and
- a p-type semiconducting layer provided on the active layer;

wherein a potential barrier is provided between each mesa portion of the p-type semiconducting layer covering each mesa surface and a bulk portion of the p-type semiconducting layer covering the bulk semiconducting surface, the potential barrier
15 surrounding each mesa portion of the p-type semiconducting layer covering the mesa surface.

12. A light emitting diode (LED) precursor comprising:
a first semiconducting layer comprising a Group III-nitride, the first semiconducting
20 layer including a mesa structure extending from a major surface of the first semiconducting layer to define a growth surface including a bulk semiconductor surface and a mesa surface;

a monolithic LED structure provided on the growth surface of the first semiconducting layer such that the monolithic LED structure covers the mesa surface and
25 the bulk semiconducting surface, the monolithic LED structure comprising a plurality of layers, each layer formed comprising a Group III-nitride, including:

- an n-type semiconducting layer;
- an active layer provided on the n-type semiconducting layer, the active
layer configured to generate light; and
30 - a p-type semiconducting layer provided on the active layer;

wherein a potential barrier is provided between a first portion of the p-type semiconducting layer covering the mesa surface and a second portion of the p-type semiconducting layer covering the bulk semiconducting surface, the potential barrier
35 surrounding the first portion of the p-type semiconducting layer covering the mesa surface.

13. A LED precursor according to claim 12, wherein the second semiconducting layer comprises an inclined sidewall portion extending between a first portion of the second semiconducting layer on the mesa surface of the first semiconducting layer and a second portion of the second semiconducting layer on the bulk semiconducting surface of the first semiconducting layer.
14. A LED precursor according to claim 13, wherein:
the p-type semiconducting layer comprises Al, wherein:
an inclined sidewall portion of the p-type semiconducting layer comprises a higher concentration of Al than the first portion of the p-type semiconducting layer covering the mesa surface such that a potential barrier is formed in the inclined sidewall portion of the p-type semiconducting layer between the first portion of the p-type semiconducting layer and the second portion of the p-type semiconducting layer.
15. A LED precursor according to any of claims 12 to 14, wherein a portion of the p-type semiconducting layer encircling the first portion of the p-type semiconducting layer covering the mesa structure is selectively removed to expose the active layer below.
16. A LED precursor according to any of claims 12 to 15, wherein a height of the mesa structure between the mesa surface and the bulk semiconducting layer surface is at least 200 nm.
17. A LED precursor according to any of claims 12 to 16, wherein a surface area of the mesa surface is no greater than 100 μm x 100 μm .
18. A LED precursor according to any of claims 12 to 17, wherein a height of the mesa structure between the mesa surface and the bulk semiconducting layer surface is at least equal to a cross-sectional width of the mesa surface of the mesa structure.
19. A light emitting diode array precursor comprising:
a first semiconducting layer comprising a Group III-nitride, the first semiconducting layer including a plurality mesa structures, each mesa structure extending from a major surface of the first semiconducting layer to define a growth surface including a bulk semiconductor surface and a plurality of mesa surfaces;

a monolithic LED array structure provided on the growth surface of the first semiconducting layer such that the monolithic LED array structure covers each of the mesa surfaces and the bulk semiconducting surface, the monolithic LED array structure comprising a plurality of layers, each layer comprising a Group III-nitride, including:

- 5 - an n-type semiconducting layer;
- an active layer provided on the n-type semiconducting layer, the active layer configured to generate light; and
- a p-type semiconducting layer provided on the active layer;

10 wherein a potential barrier is provided between each mesa portion of the p-type semiconducting layer covering each of the mesa surfaces and a bulk portion of the p-type semiconducting layer covering the bulk semiconducting surface, the potential barrier surrounding each of the mesa portions of the p-type semiconducting layer covering the mesa surface.

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