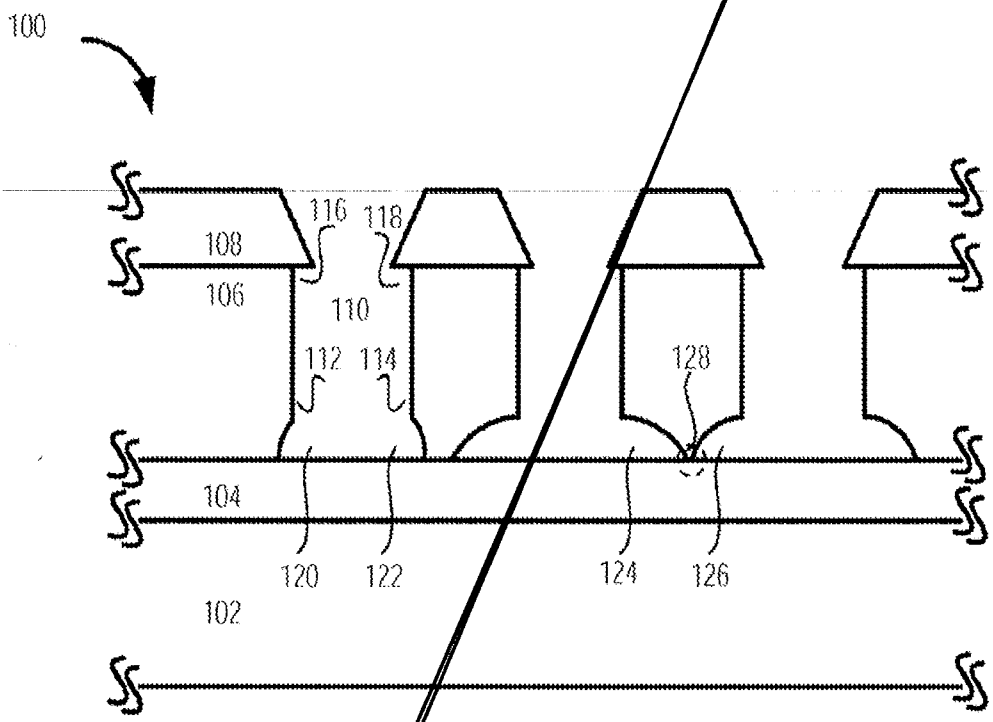


FIG. 1
(PRIOR ART)

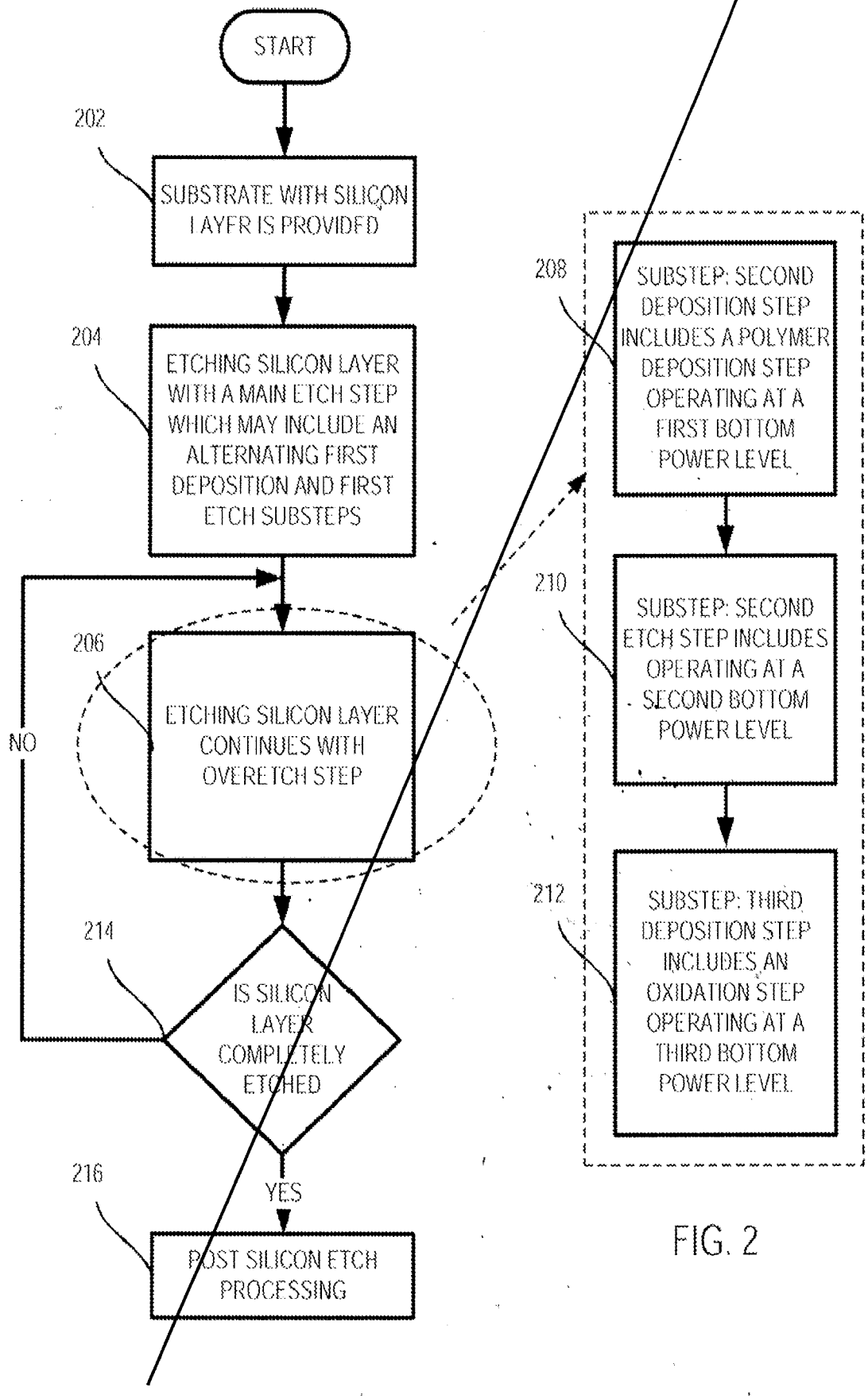

START
202
SUBSTRATE WITH SILICON LAYER IS PROVIDED
204
ETCHING SILICON LAYER WITH A MAIN ETCH STEP WHICH MAY INCLUDE AN ALTERNATING FIRST DEPOSITION AND FIRST ETCH SUBSTEPS
206
ETCHING SILICON LAYER CONTINUES WITH OVERETCH STEP
NO
214
IS SILICON LAYER COMPLETELY ETCHED
YES
216
POST SILICON ETCH PROCESSING
208
SUBSTEP: SECOND DEPOSITION STEP INCLUDES A POLYMER DEPOSITION STEP OPERATING AT A FIRST BOTTOM POWER LEVEL
210
SUBSTEP: SECOND ETCH STEP INCLUDES OPERATING AT A SECOND BOTTOM POWER LEVEL
212
SUBSTEP: THIRD DEPOSITION STEP INCLUDES AN OXIDATION STEP OPERATING AT A THIRD BOTTOM POWER LEVEL

FIG. 2

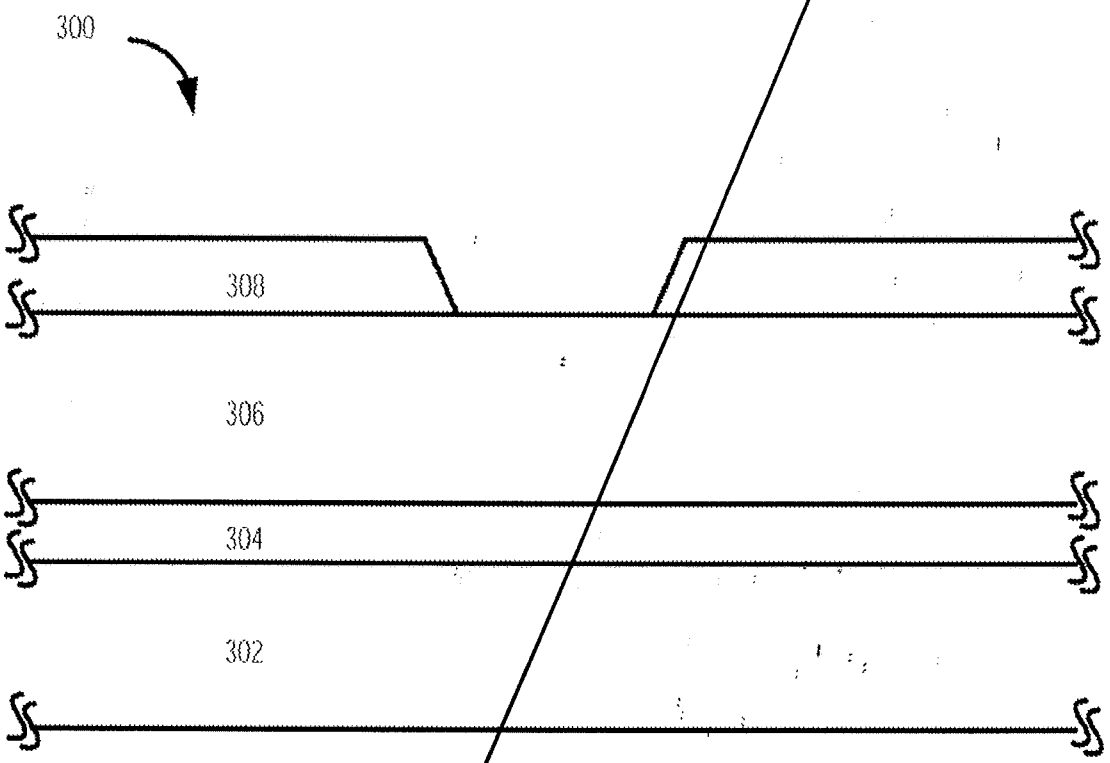


FIG. 3

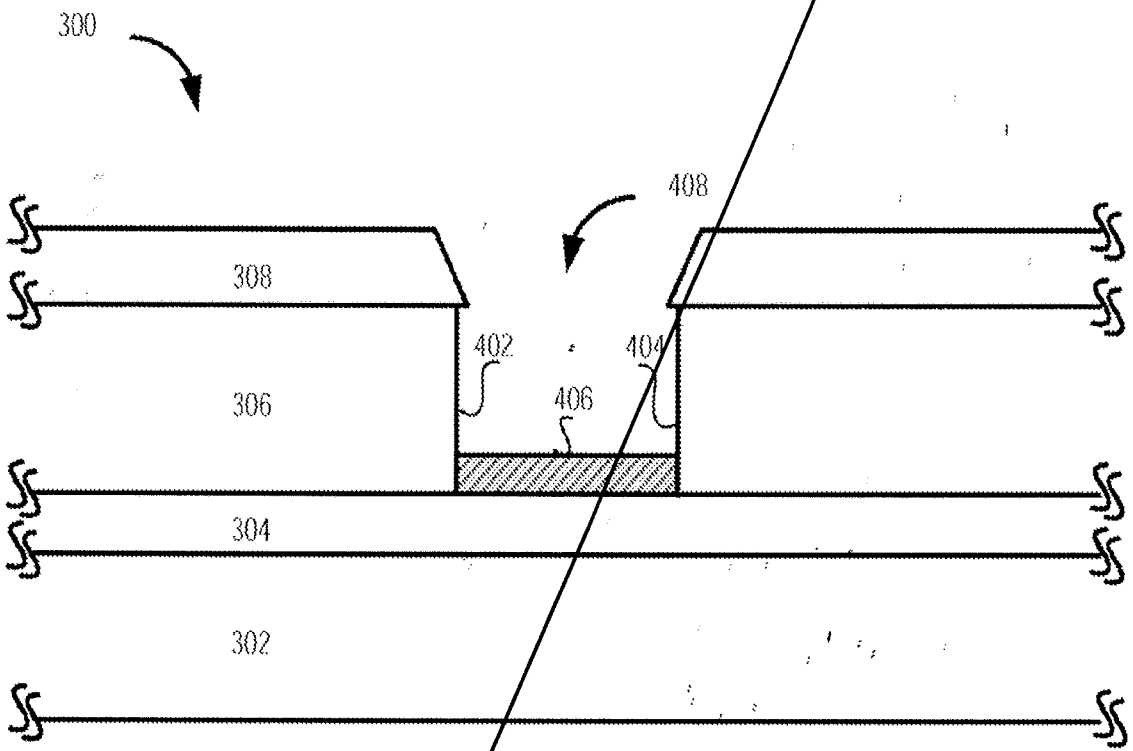


FIG. 4

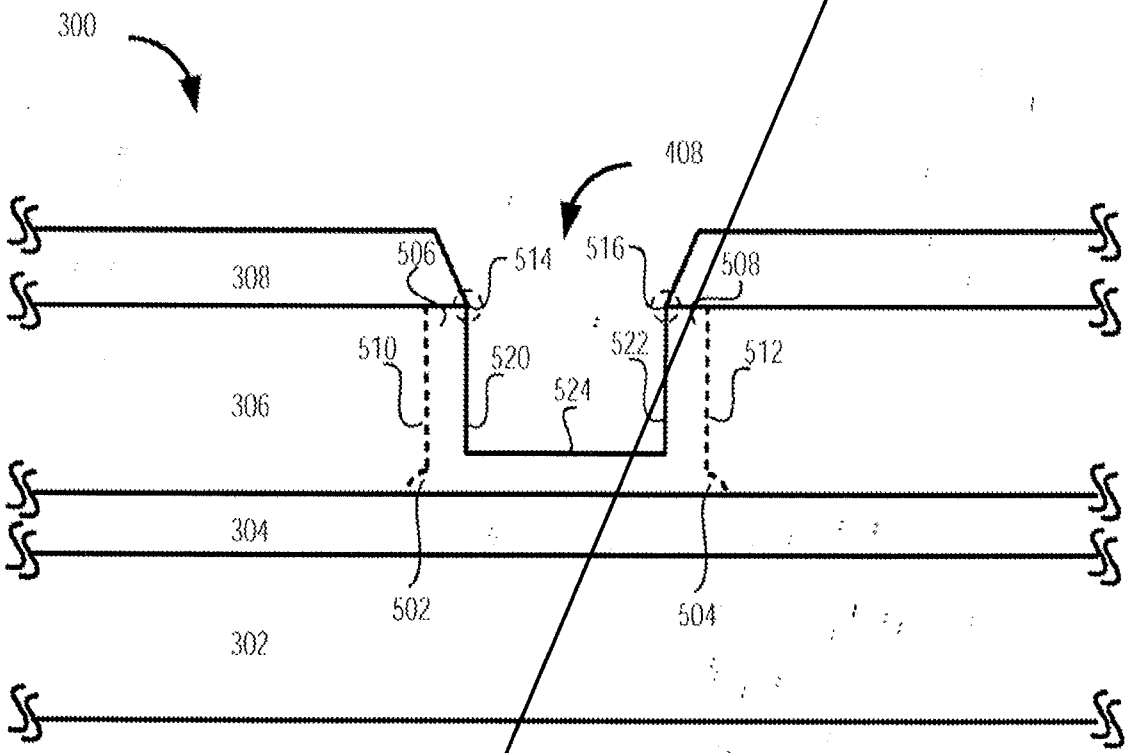

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FIG. 5

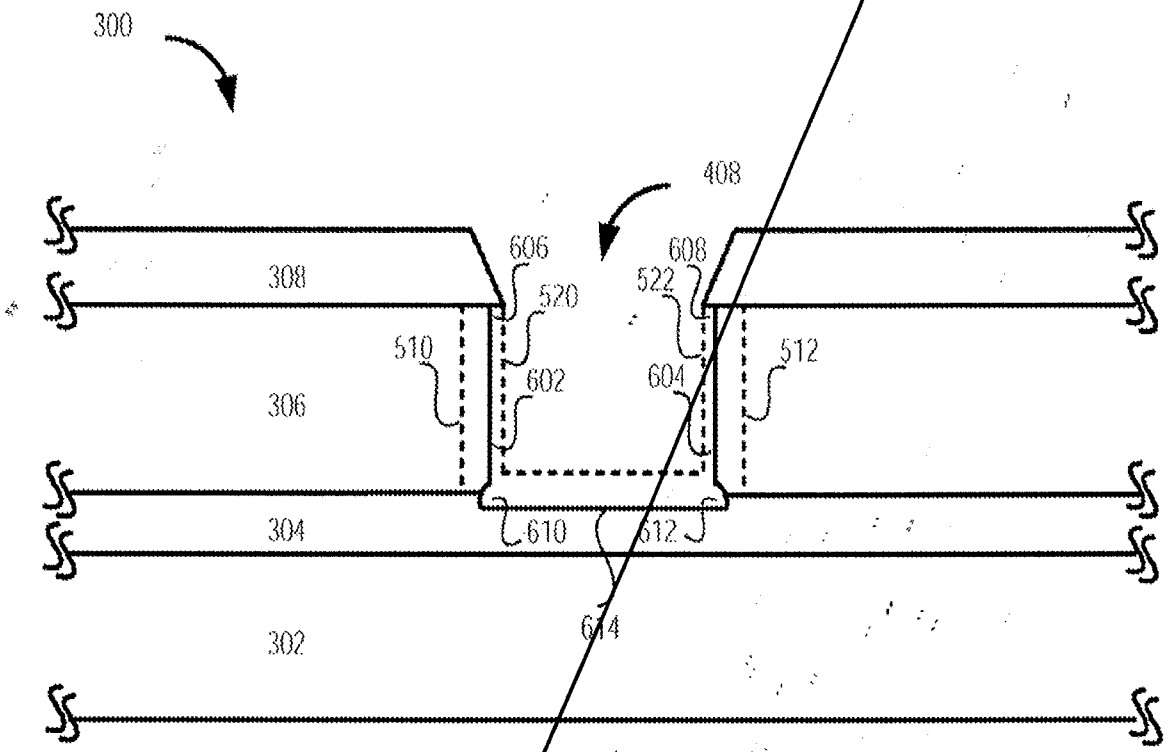

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FIG. 6

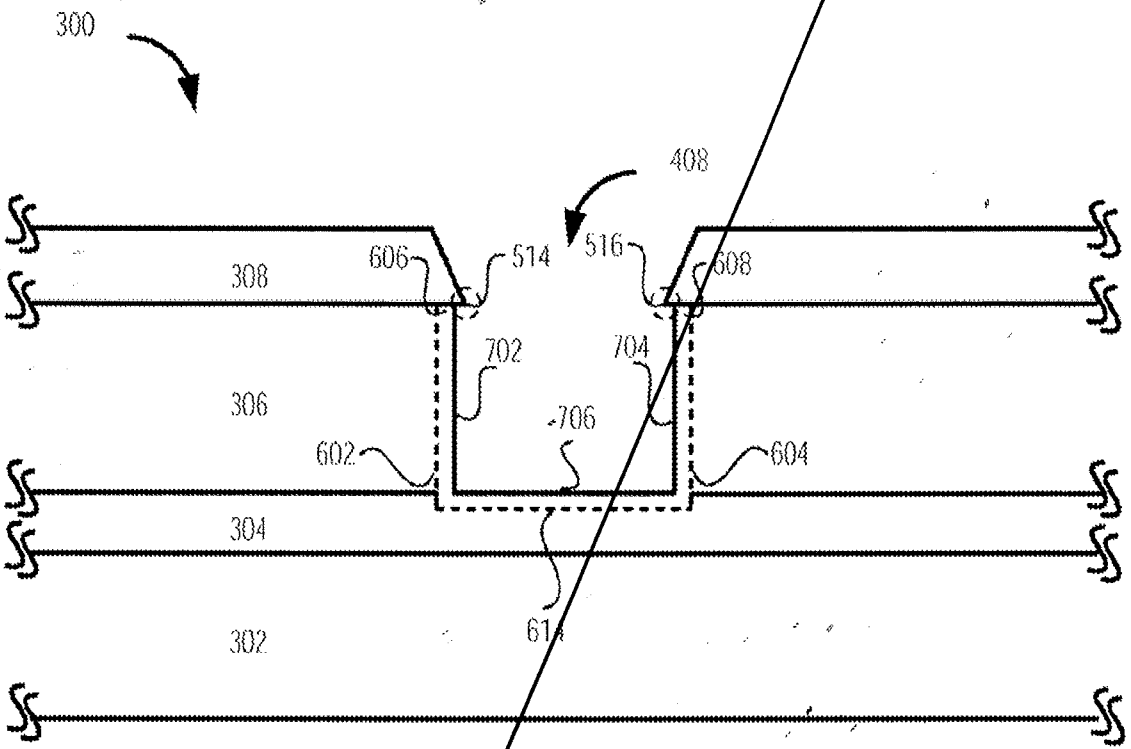


FIG. 7

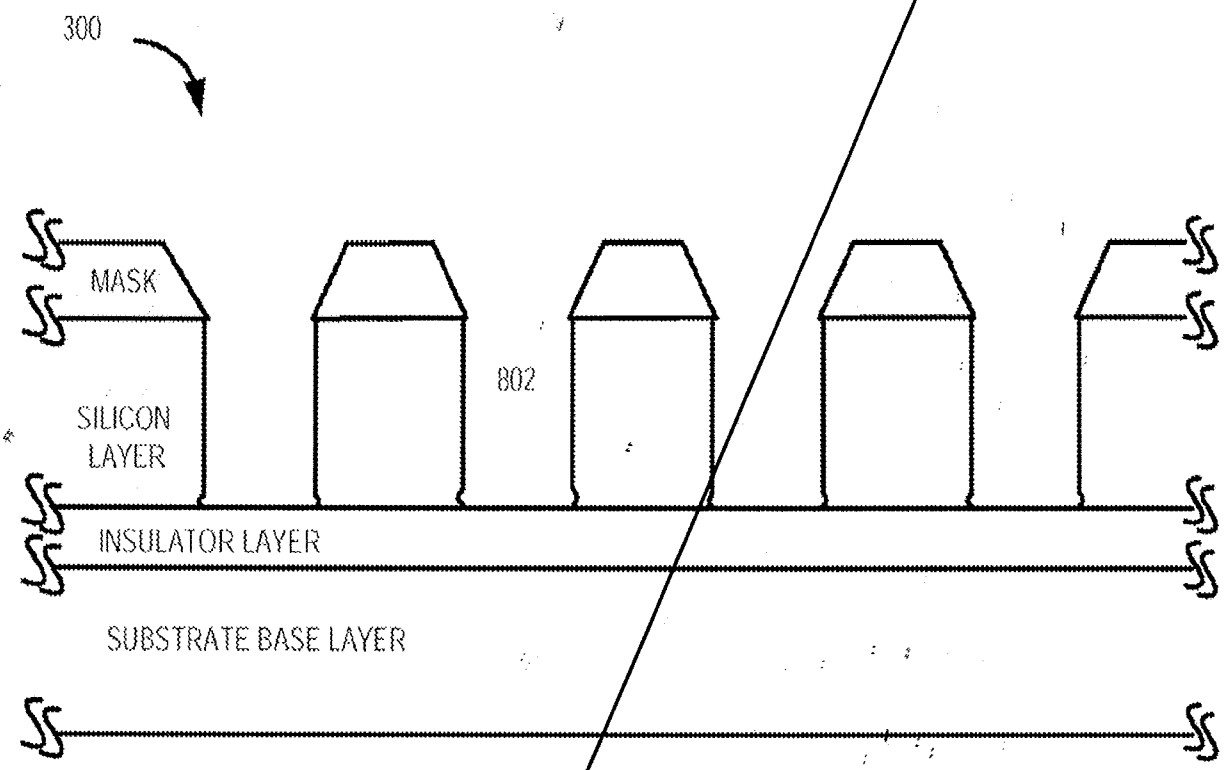

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MASK
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SILICON LAYER
INSULATOR LAYER
SUBSTRATE BASE LAYER

FIG. 8A

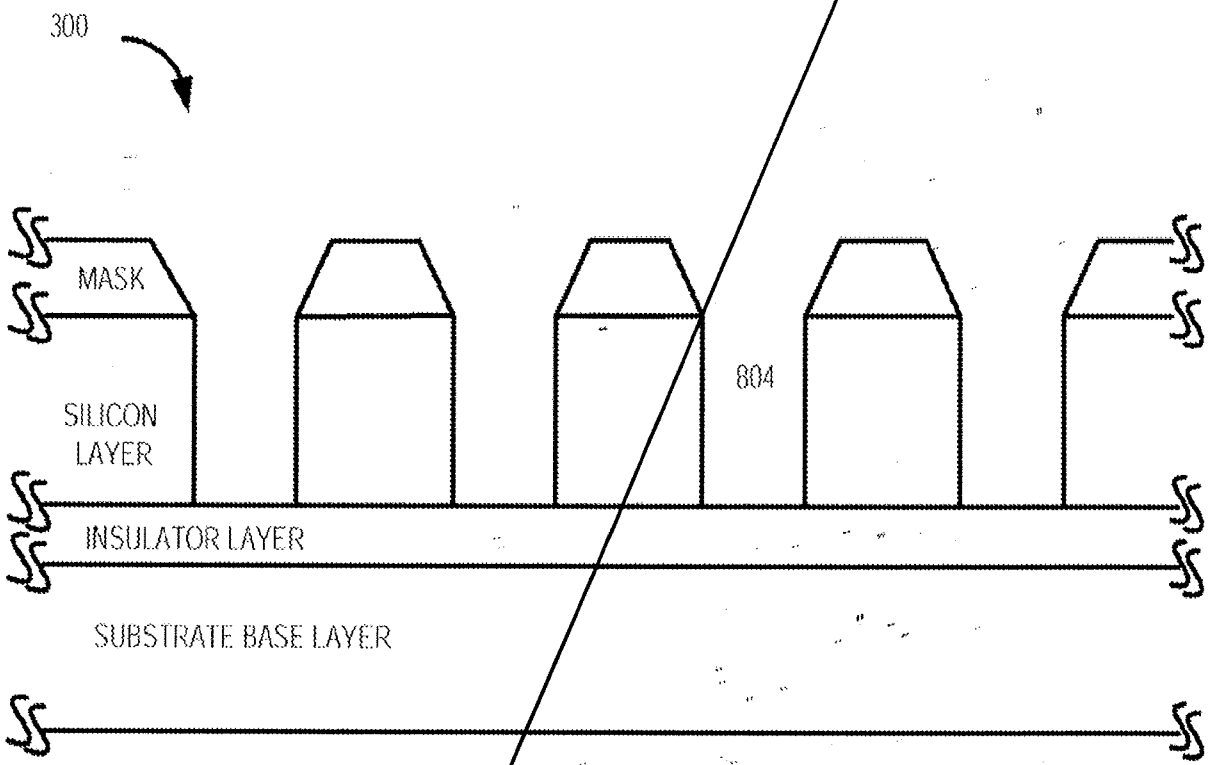

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MASK
804
SILICON LAYER
INSULATOR LAYER
SUBSTRATE BASE LAYER

FIG. 8B

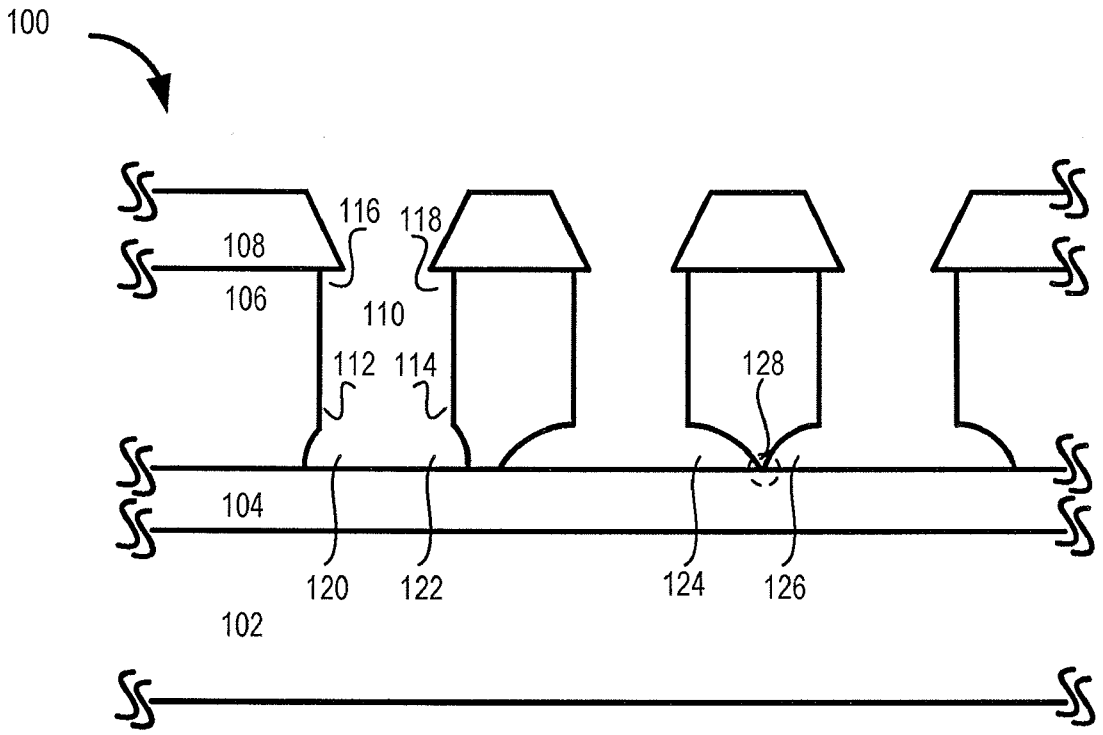


FIGURE 1
(PRIOR ART)

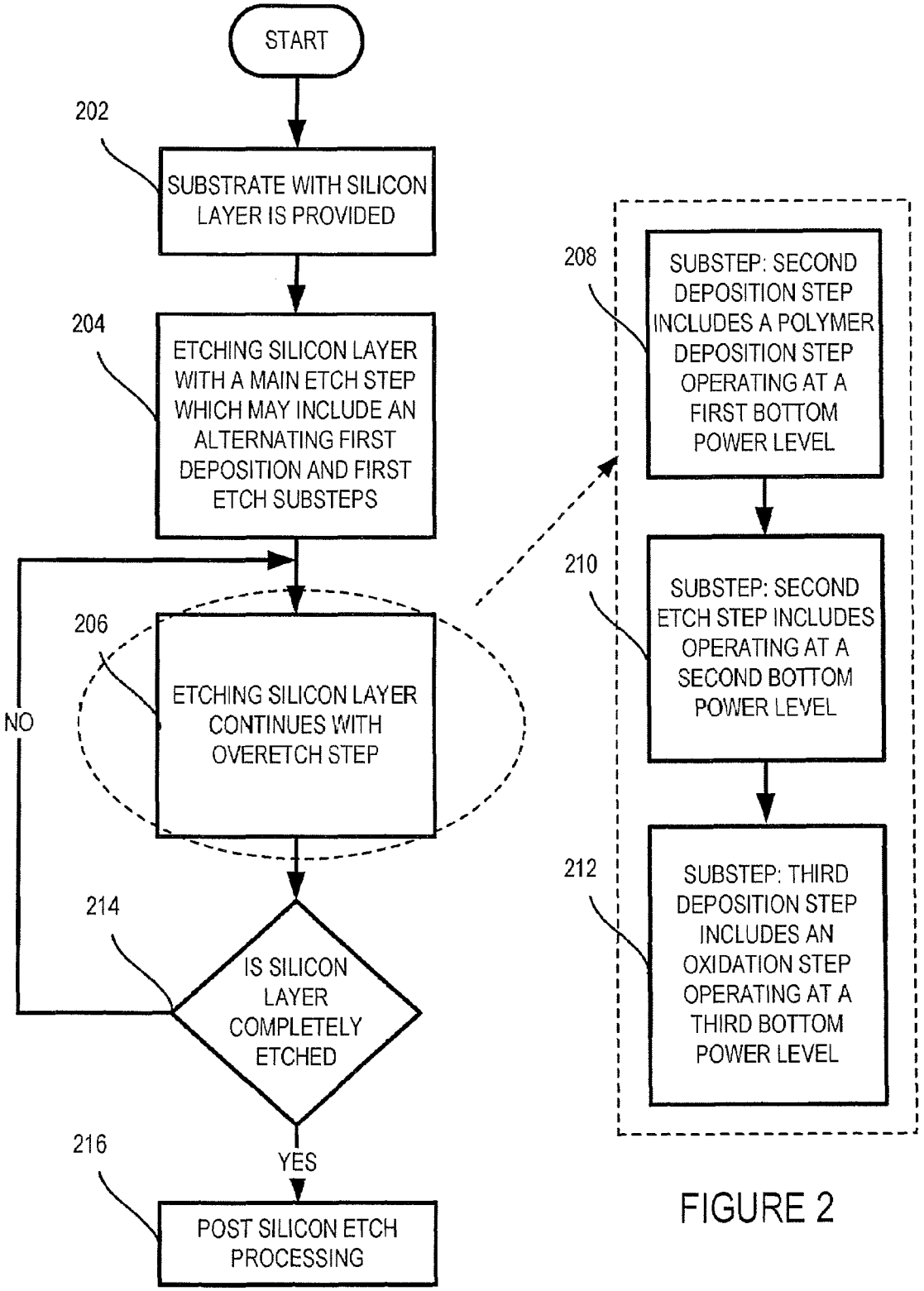

START
202
SUBSTRATE WITH SILICON LAYER IS PROVIDED
204
ETCHING SILICON LAYER WITH A MAIN ETCH STEP WHICH MAY INCLUDE AN ALTERNATING FIRST DEPOSITION AND FIRST ETCH SUBSTEPS
206
ETCHING SILICON LAYER CONTINUES WITH OVERETCH STEP
NO
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IS SILICON LAYER COMPLETELY ETCHED
YES
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POST SILICON ETCH PROCESSING
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SUBSTEP: SECOND DEPOSITION STEP INCLUDES A POLYMER DEPOSITION STEP OPERATING AT A FIRST BOTTOM POWER LEVEL
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SUBSTEP: SECOND ETCH STEP INCLUDES OPERATING AT A SECOND BOTTOM POWER LEVEL
212
SUBSTEP: THIRD DEPOSITION STEP INCLUDES AN OXIDATION STEP OPERATING AT A THIRD BOTTOM POWER LEVEL

FIGURE 2

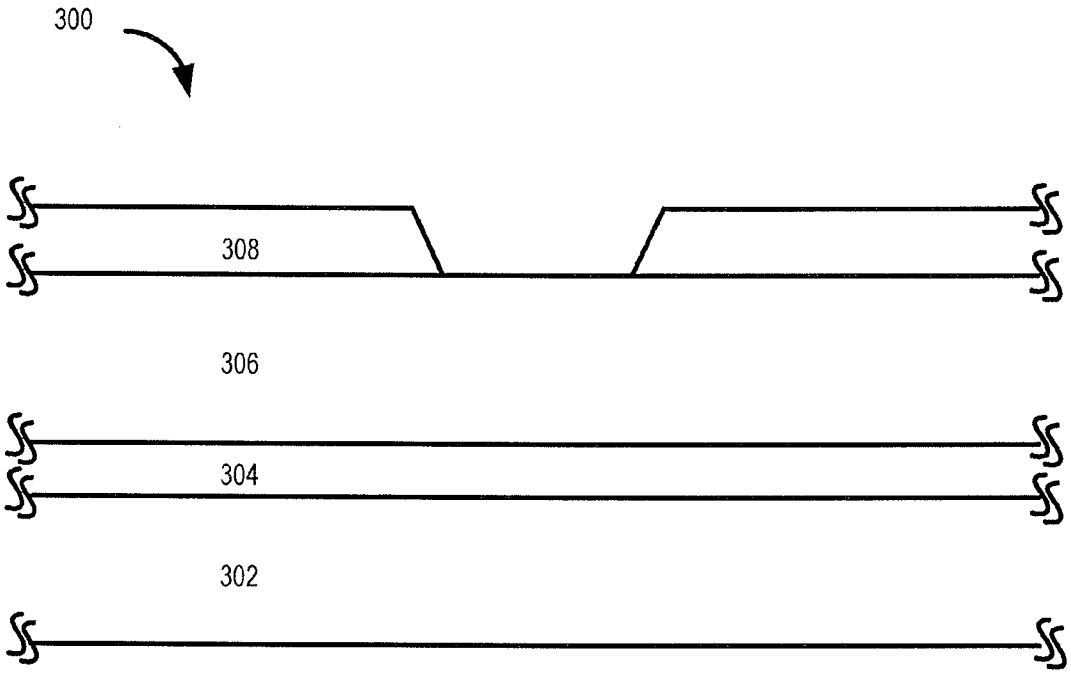


FIGURE 3

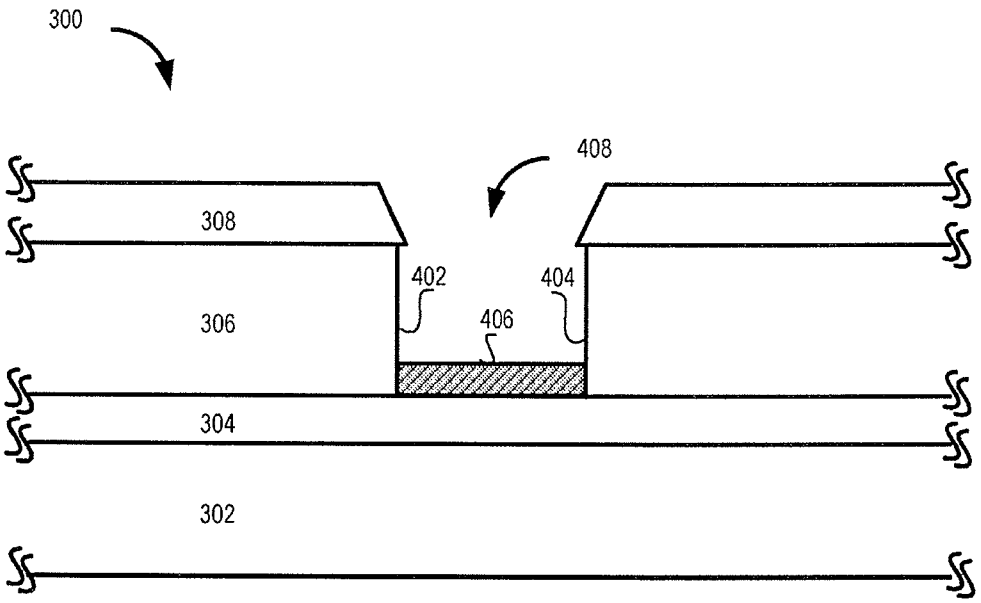


FIGURE 4

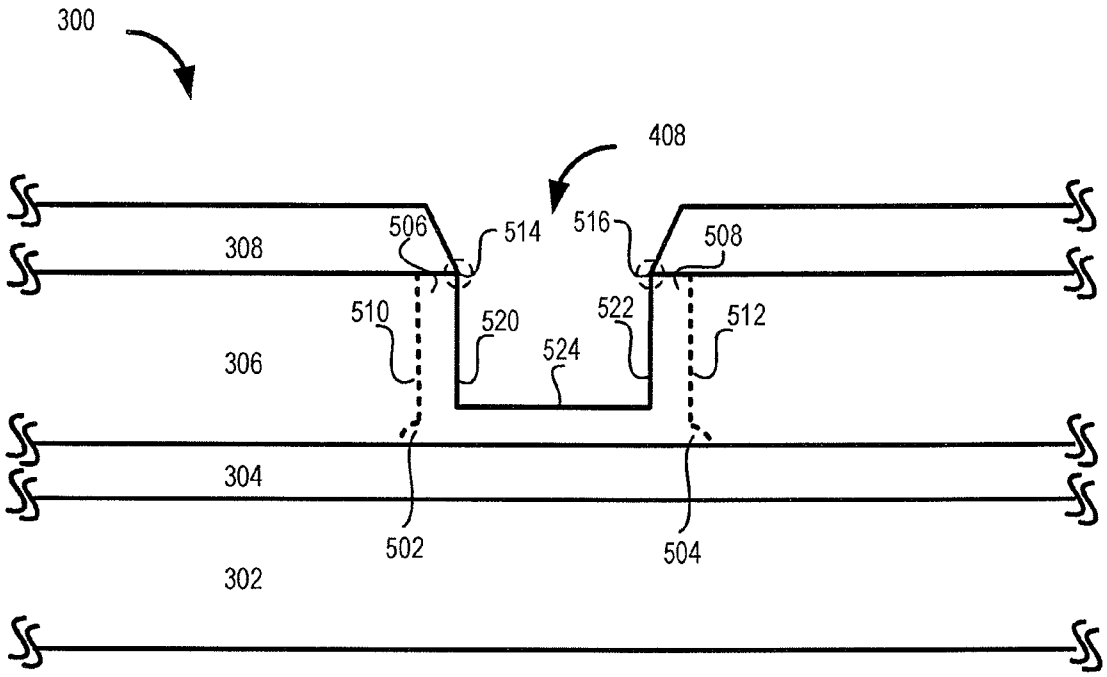

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FIGURE 5

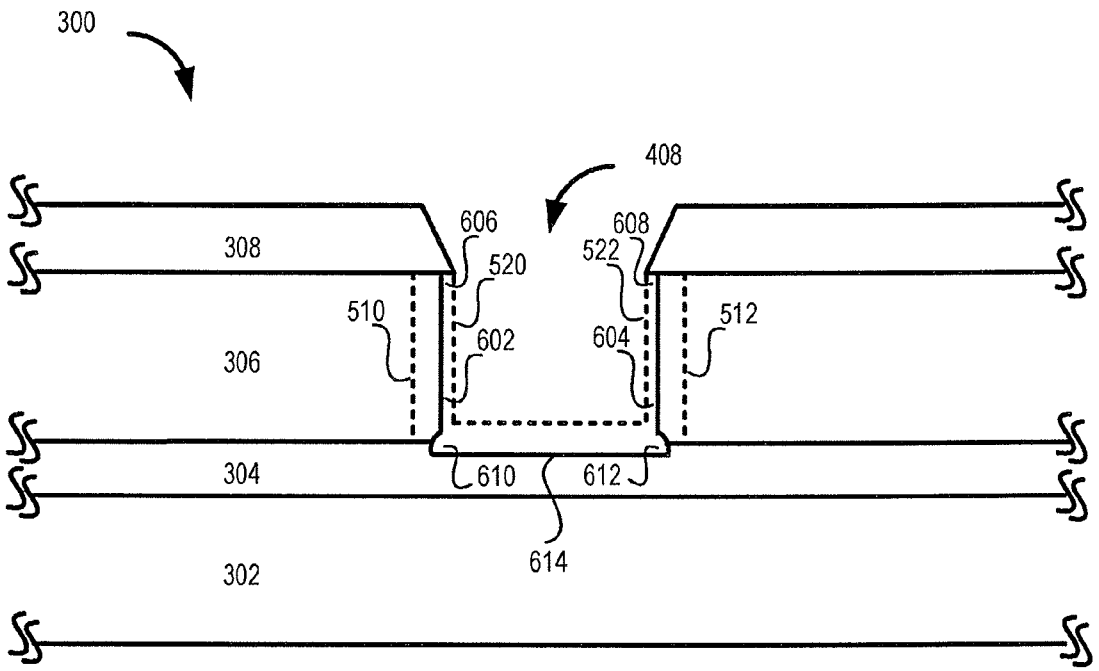

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FIGURE 6

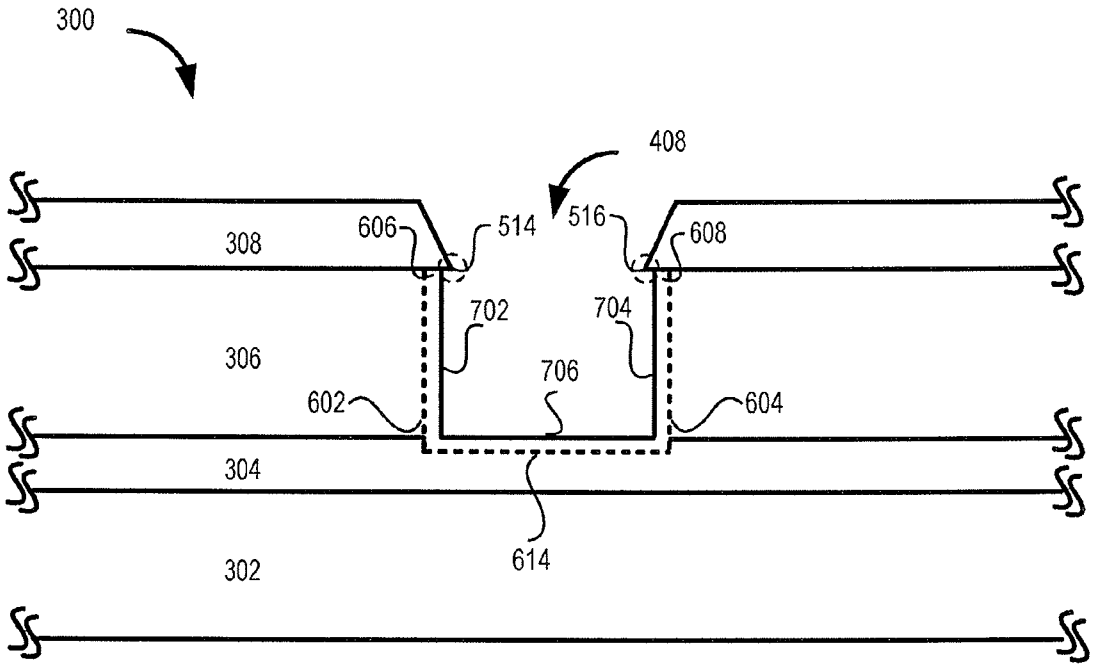


FIGURE 7

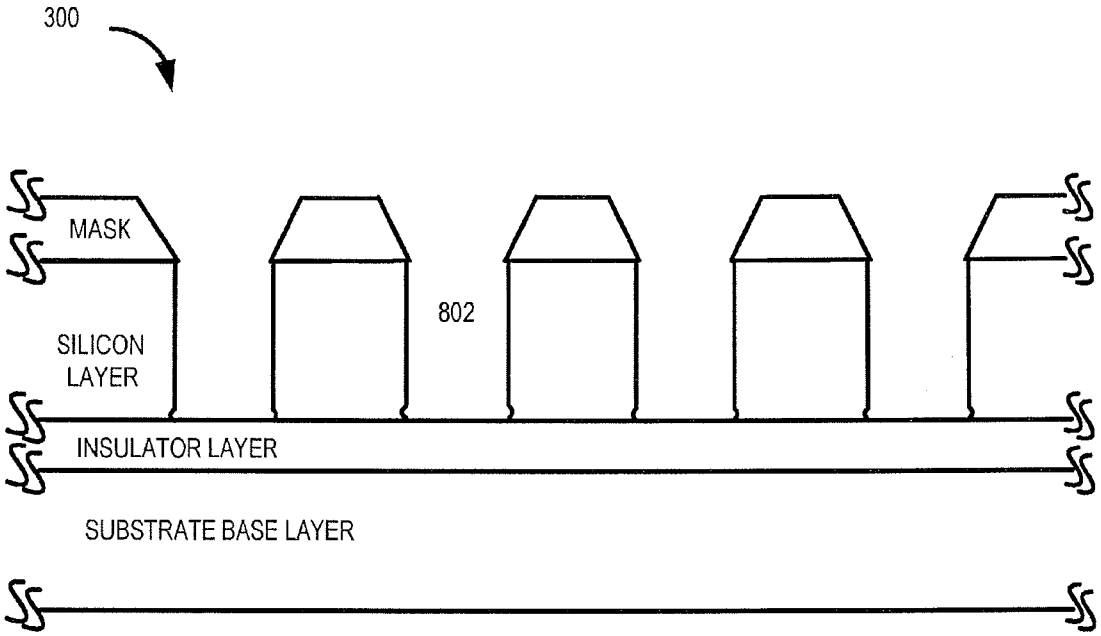

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MASK
802
SILICON
LAYER
INSULATOR LAYER
SUBSTRATE BASE LAYER

FIGURE 8A

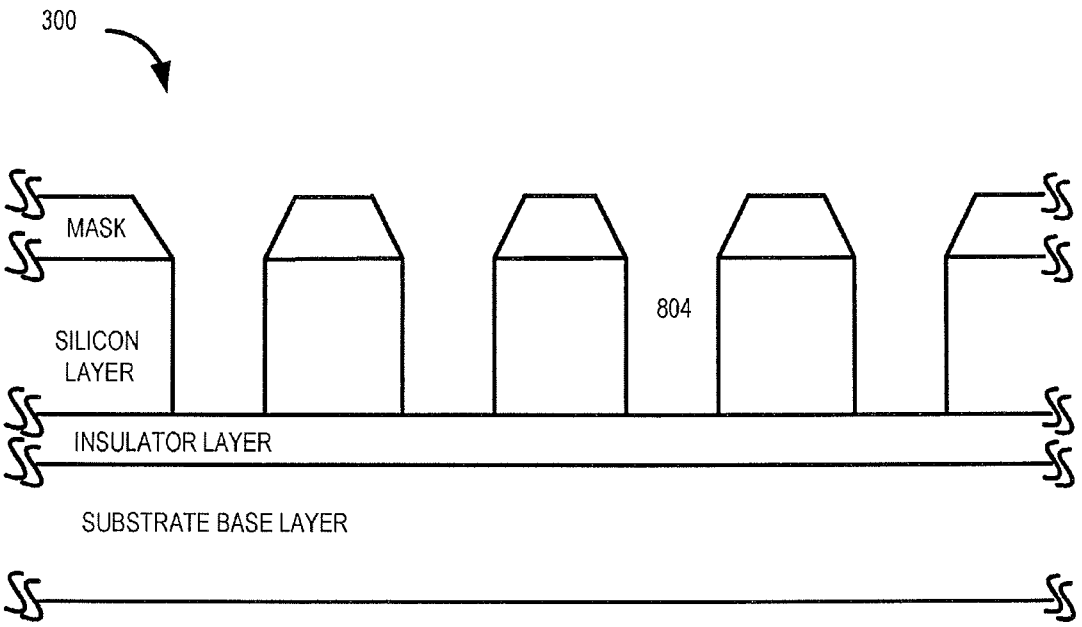

300
MASK
804
SILICON
LAYER
INSULATOR LAYER
SUBSTRATE BASE LAYER

FIGURE 8B