

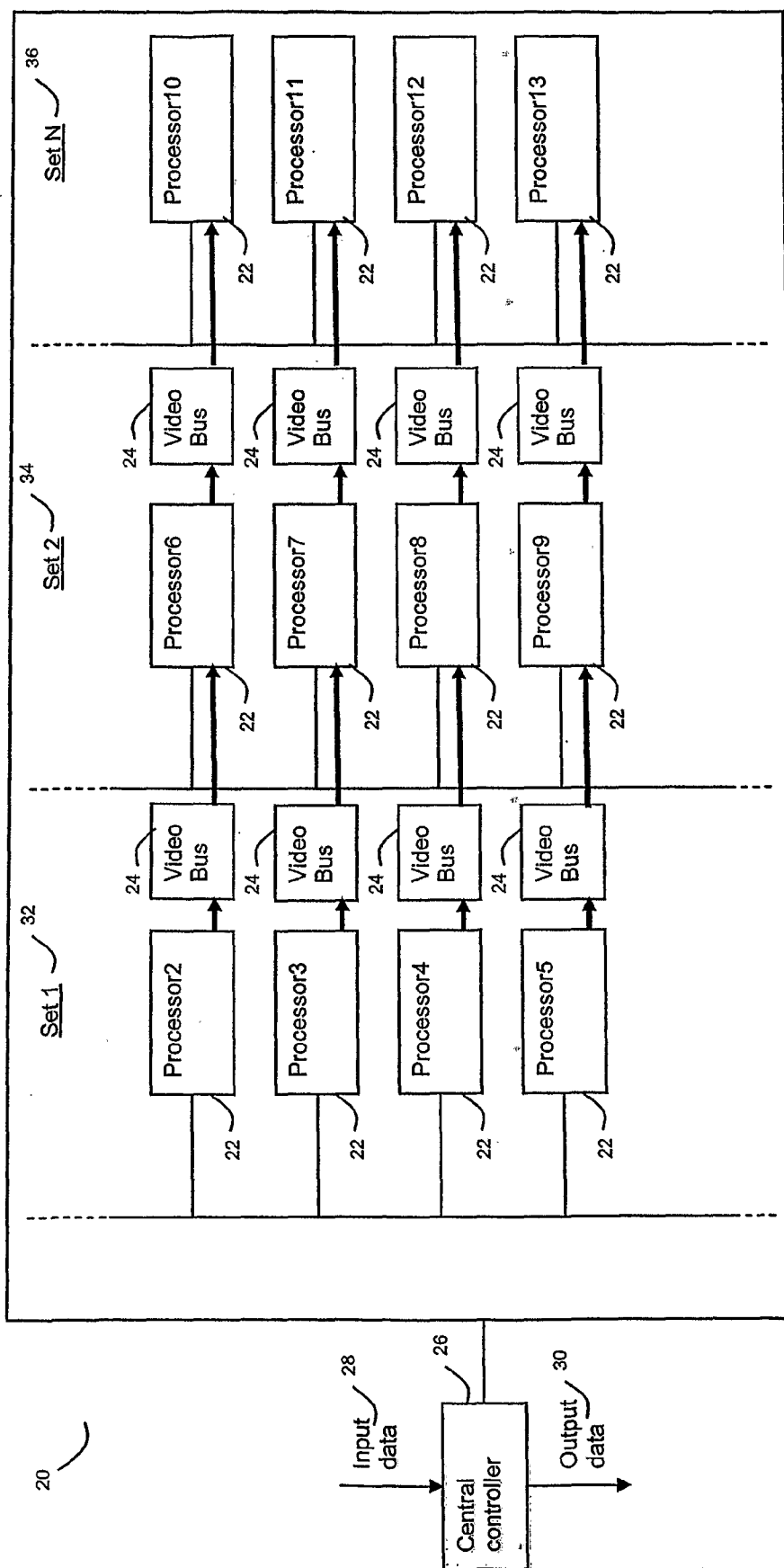


Figure 1

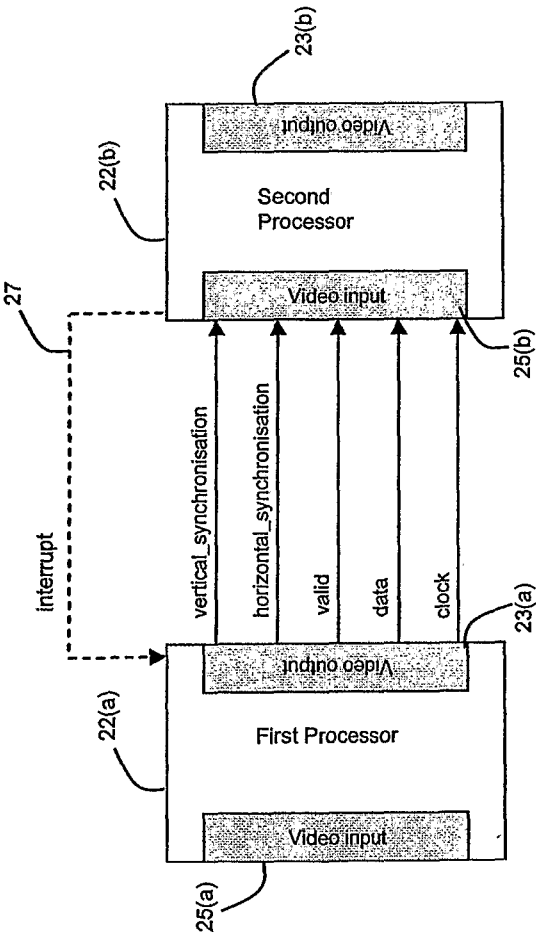


Figure 2

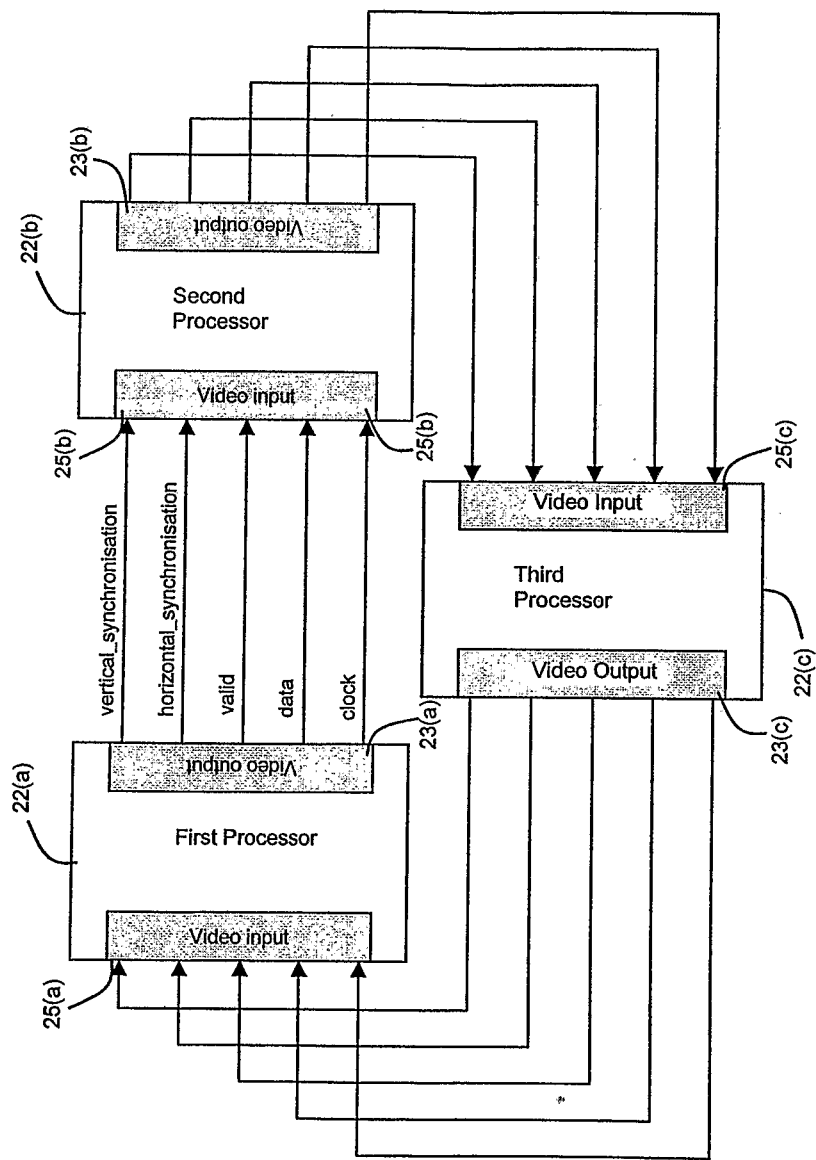


Figure 3

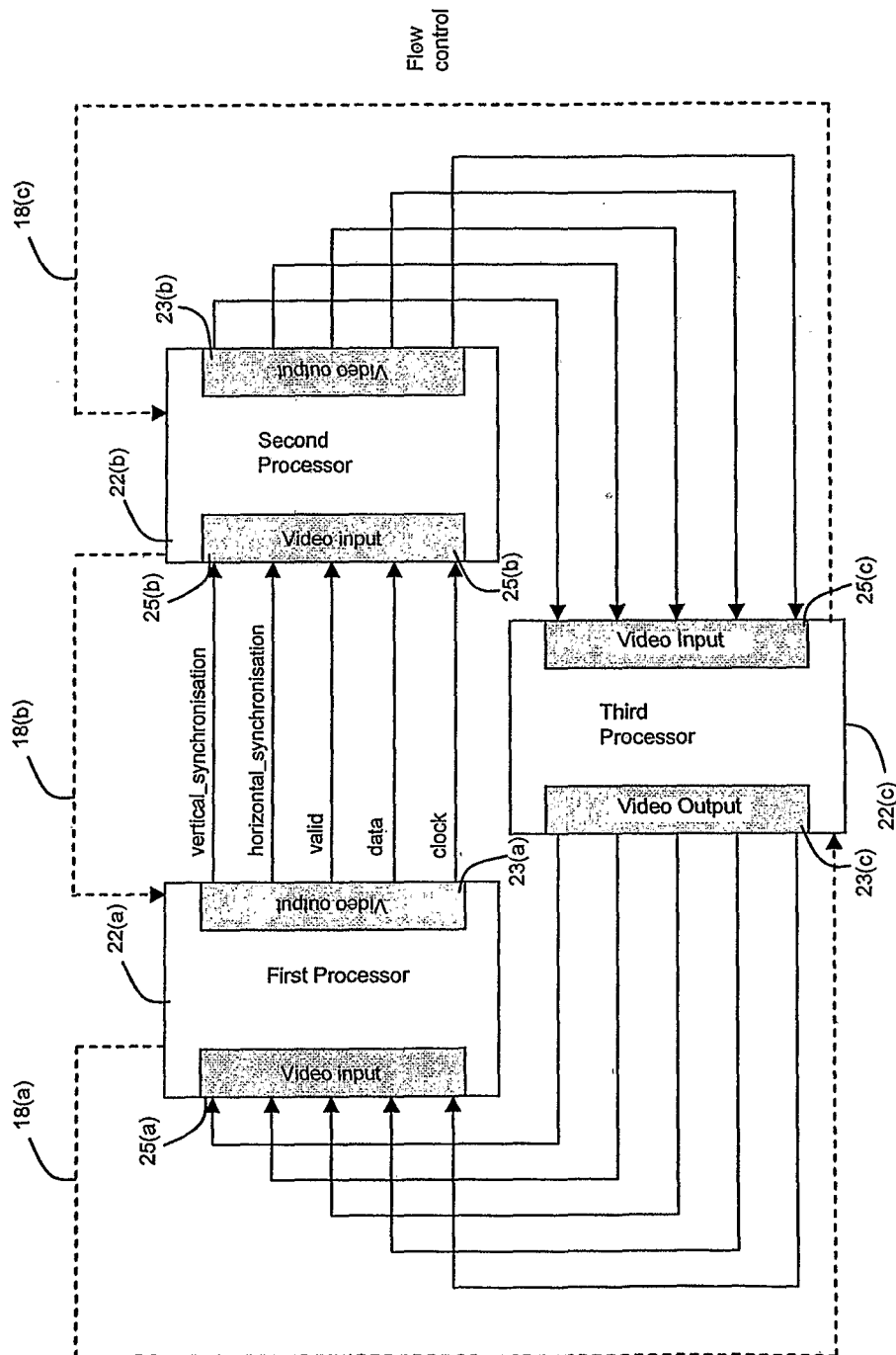


Figure 4

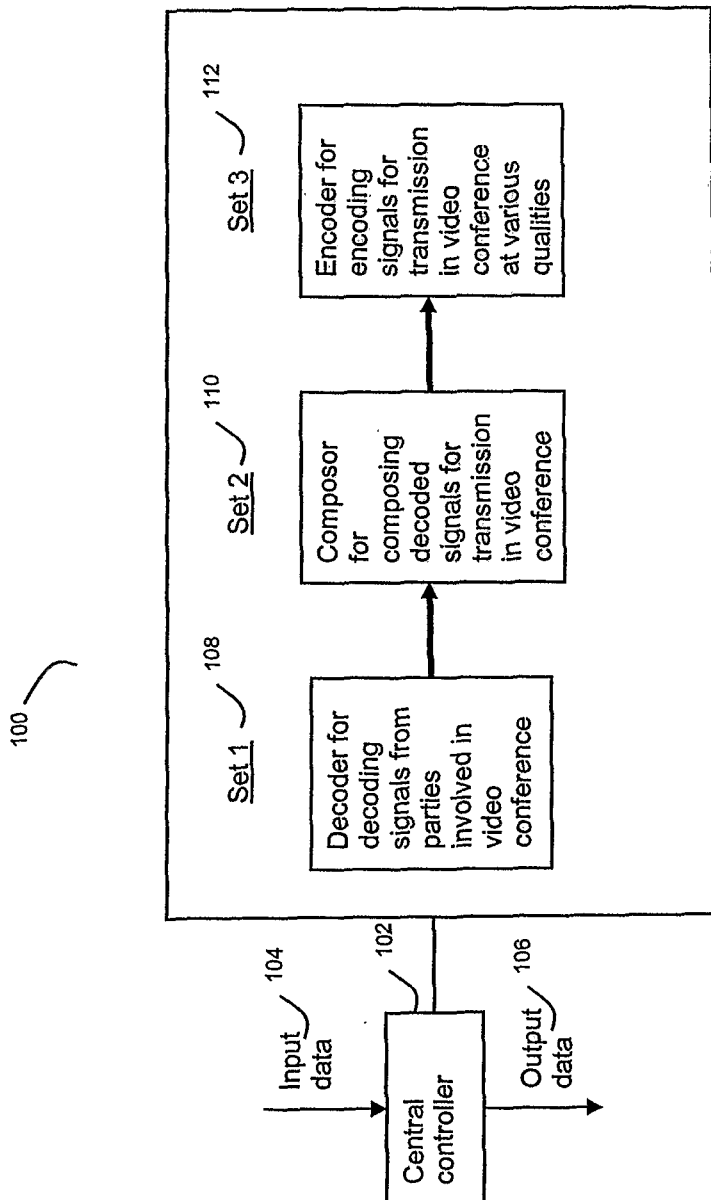


Figure 5

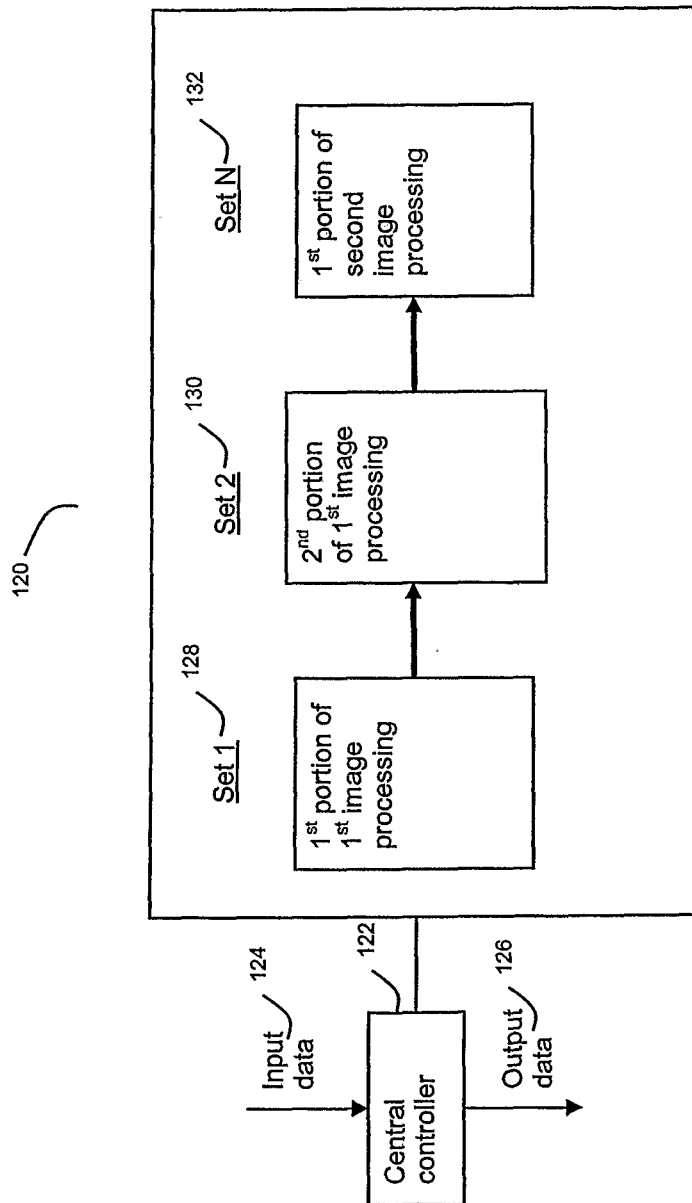


Figure 6

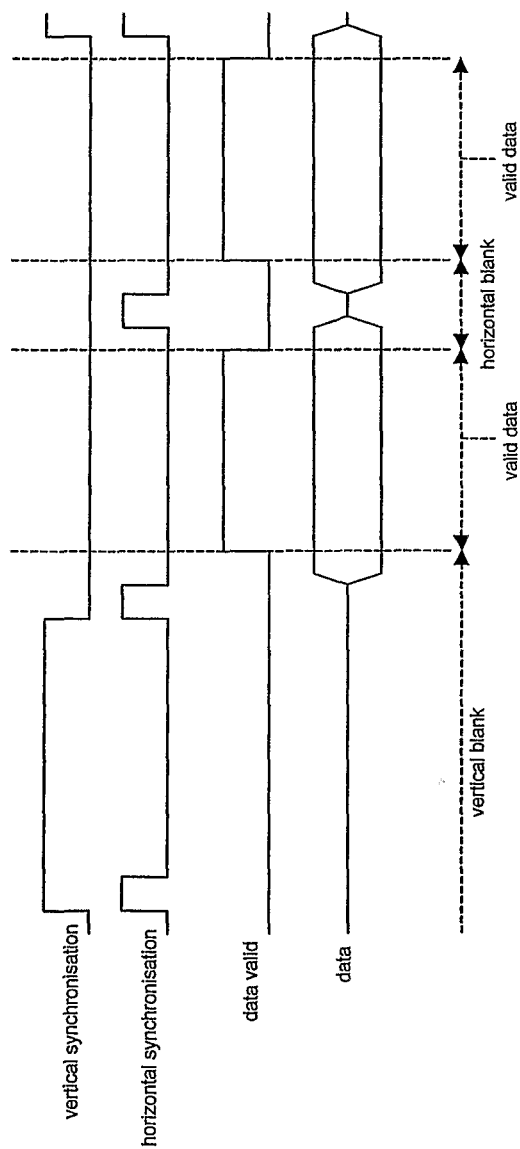


Figure 7

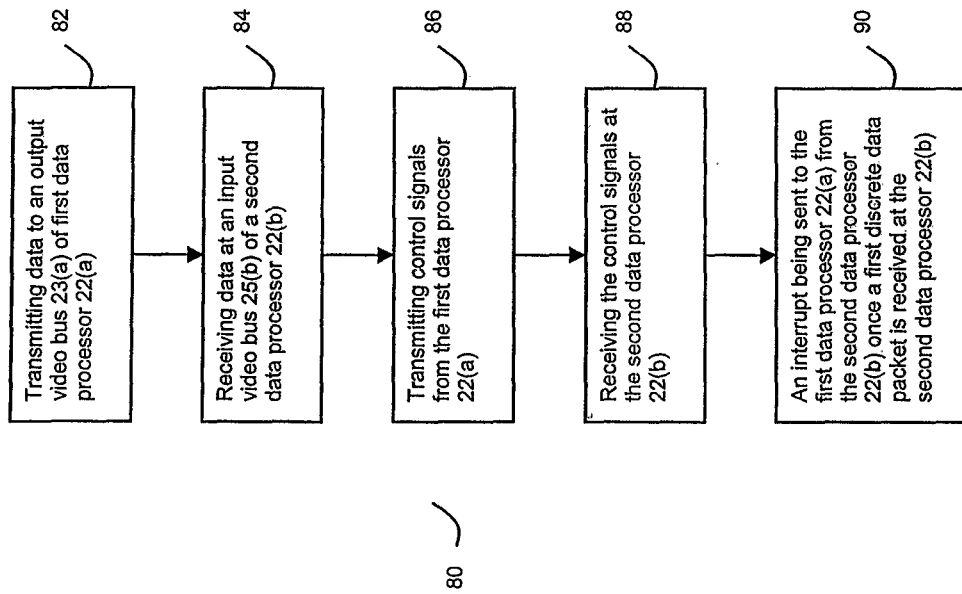


Figure 8

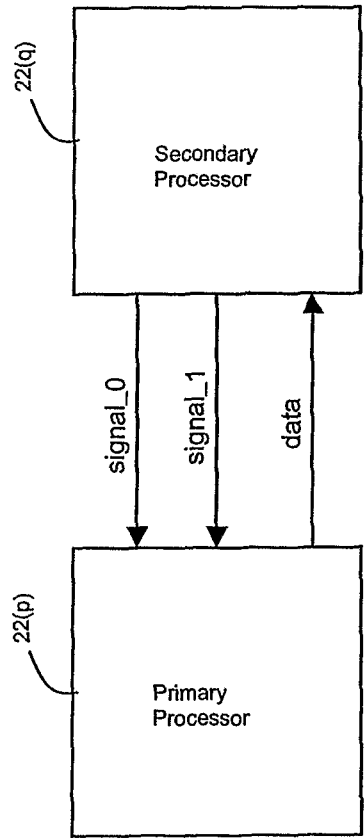


Figure 9

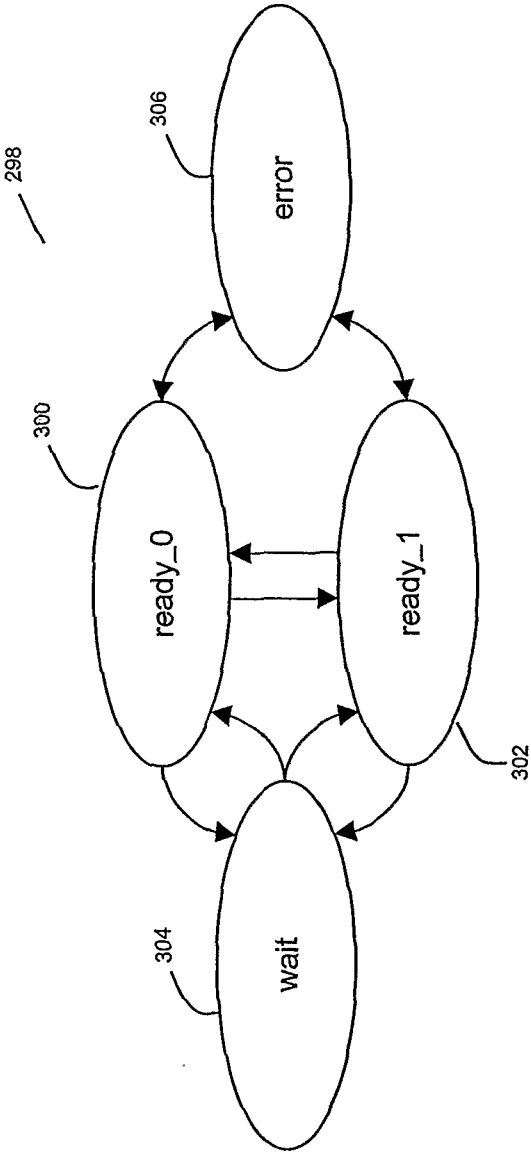


Figure 10

state	signal_0	signal_1
wait	0	0
ready_0	0	1
ready_1	1	0
error	1	1

Figure 11

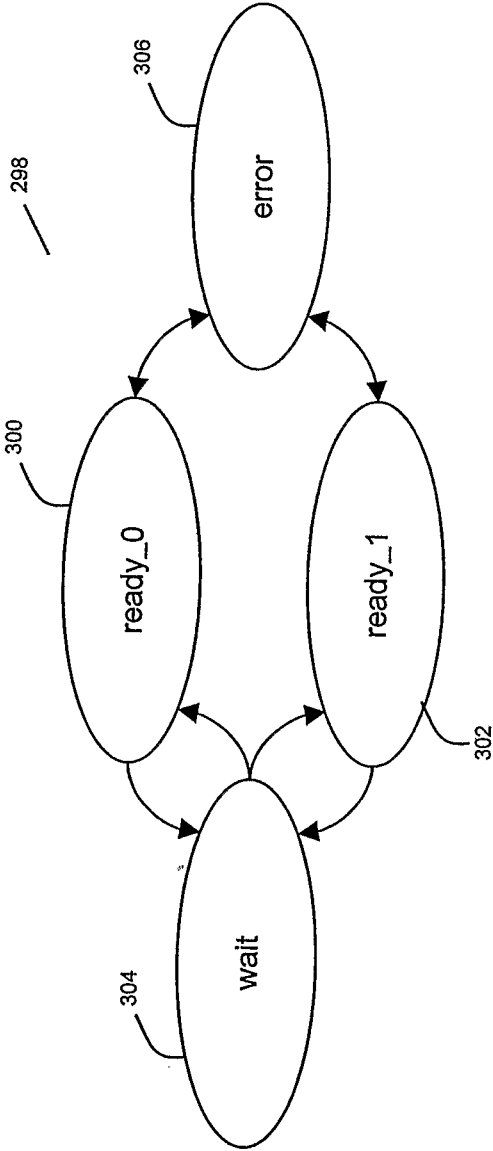


Figure 12

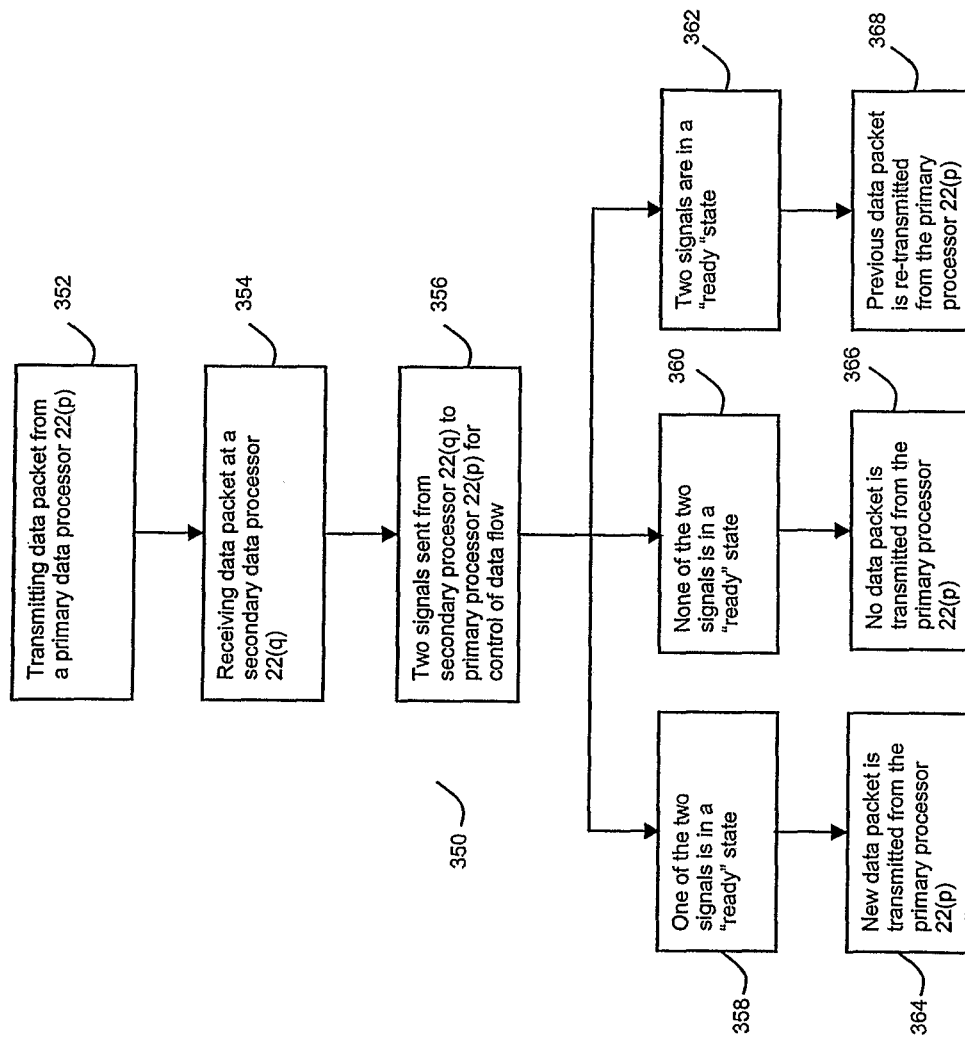


Figure 13