

ELECTRONIC TIMEPIECE

This invention relates to electronic timepieces.

The term "voice" used in this specification refers to any audible sound such as, for example, human voice, music or imitation sound.

5 Recently, multifunction electronic timepieces such as electronic timepieces with alarm or timer functions have been developed. However, the warning sound made by such electronic timepieces when the actual time and a preset time coincide is determined by the manufacturer and cannot be changed by the user.

10 Further, there is the disadvantage that the user must remember and recognise what the sound means.

 In order to eliminate these disadvantages, an electronic timepiece with a voice memory has been developed. With such an electronic timepiece, the user's voice is recorded in the

15 electronic timepiece and delivered or played back as a voice sound at the proper time. Such an electronic timepiece requires signals to start recording, but it has proved troublesome for users to generate these signals by switching operations. Moreover, there is a time delay between supplying the signals and the start

20 of recording and this results in a silent or blank recording so that a memory in which the sound is recorded and whose capacity is relatively small, may be wasted.

 According to the present invention there is provided an electronic timepiece including: an oscillator circuit for generating

25 a clock signal; a frequency divider circuit connected to receive

the clock signal and to form timing signals; semiconductor recording means for performing reading and writing operations, under the control of one of the timing signals, of data relating to an external audible sound; output means for converting data read from the recording means into an audible sound; a level detector for detecting the amplitude of the external audible sound to be recorded; and a start control circuit to control the writing operation of the recording means in dependence upon the output of the level detector.

10 In one embodiment the level detector is an operational amplifier and the start control circuit is a set-reset latch.

In another embodiment the level detector comprises a NAND gate and the start control circuit is a set-reset latch.

In a further embodiment the level detector comprises a Schmitt trigger circuit and the start control circuit is a flip-flop circuit.

15 The electronic timepiece preferably includes means for converting the external audible sound into a digital data signal for storage in the recording means, the output means including a synthesizing circuit for synthesizing an audible sound from the data read from the recording means.

20 The recording means may have at least two memory regions, a memory control circuit being arranged to write data in the first of said memory regions before the start control circuit operates and to write the data in a second of said memory regions after the start control circuit has operated.

25 The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of one embodiment of an electronic timepiece according to the present invention;

Figure 2 consists of Figures 2(a) to 2(c) which illustrate various embodiments of an auto-start circuit of the electronic timepiece of Figure 1, and Figure 2(d) which is a timing chart to illustrate the operation of the auto-start circuit;

Figure 3(a) shows part of another embodiment of an electronic timepiece according to the present invention, and Figure 3 (b) is a timing chart illustrating the operation thereof;

Figure 4(a) shows part of a further embodiment of an electronic timepiece according to the present invention, and Figure 4(b) is a timing chart illustrating the operation thereof; and

Figure 5 consists of Figures 5(a) which is a block diagram of a recorder of the electronic timepiece of Figure 1 and Figure 5(b) which shows a divided form of RAM memory thereof.

Throughout the drawings like parts have been designated by the same reference numerals.

Referring to Figure 1, there is illustrated one embodiment of an electronic timepiece according to the present invention. The electronic timepiece comprises an oscillator circuit 1 for generating a standard clock signal, a frequency divider circuit 2 connected to receive the standard clock signal and to form desired timing signals, functional circuits F_1 to F_n such as, for example, a timekeeping circuit and a display circuit, and a microphone 3 which is also used as a speaker. The microphone 3 is connected

with an input/output switching circuit 5 through an amplifier 4. A code circuit 6 receives a voice signal VOICE and converts it from an analogue signal into a corresponding digital data signal. The data or coded signal from the code circuit 6 is stored sequentially in a recorder 7. The code circuit 6 and the recorder 7 operate when a record auto-start signal AST becomes logic 1. The recorder 7 is mainly composed of semiconductor memory such as RAM or a shift register, and read and write operations are performed under the control of one of the timing signals from the divider circuit 2. A voice synthesizing circuit 8 synthesizes an analogue voice signal from the digital signal which is read out from the recorder 7. An auto-start circuit 9 comprises a level detector to detect a predetermined recording level of the voice signal and a start control circuit to make the signal AST logic 1 in response to the output of the level detector. The auto-start circuit 9 drives the code circuit 6 and the recorder 7 when the level of the voice signal exceeds the predetermined recording level. $\bar{R}$ indicates a reset signal. The auto-start circuit is reset when the signal AST is logic 0. A switching control circuit 10 forms signals required to control each function of the electronic timepiece in response to operation of switches S_1 to S_n .

Figure 2 consists of Figures 2(a) to 2(c) which illustrate various embodiments of the auto-start circuit 9 of Figure 1 and Figure 2(d) which is a timing chart illustrating the operation of the auto-start circuit at the time of starting recording.



The auto-start circuit shown in Figure 2(a) has a standard voltage generating circuit 11 for generating a standard voltage V_c , a level detector 12 which consists of an operation amplifier producing a signal of logic 0 when the voice signal is higher than the standard voltage V_c , and NAND gates 13 forming a set-reset latch, the output of the level detector 12 being the set signal. The latch operates as the start control circuit as shown by the timing chart of Figure 2(d).

Figure 2(b) shows an embodiment of the auto-start circuit 9 using only a multi-input NAND gate 14 as the level detector, the inputs being connected together to increase the number of P-MOSFETs switched on in parallel thereby to increase the logic threshold voltage V_{th} to the standard voltage V_c . The output of the NAND gate 14 is inverted when the voice signal exceeds the standard voltage V_c . The timing of this auto-start circuit is the same as the timing of the auto-start circuit of Figure 2(a) as illustrated in Figure 2(d). Instead of the NAND gate 14, it is possible to use a multi-input NOR gate or an inverter operating on the difference between the threshold voltage of P-MOSFETs and N-MOSFETs as the level detector.

Figure 2(c) shows a further embodiment of the auto-start circuit 9 using a Schmitt trigger circuit formed by two inverters 15 and two resistors R_f , R_g , as the level detector. The constants of the elements forming this Schmitt trigger circuit are so chosen that the threshold voltage is the standard voltage V_c when the

input changes from logic 0 to logic 1, and signal $\overline{CL}$ becomes logic 0 when the voice signal traverses the standard voltage V_c from the V_{SS} side. A flip-flop circuit 16 operates as the start control circuit, a D input signal appearing at terminal Q on the fall of the signal $\overline{CL}$. A transmission gate 17 is switched OFF and P-MOSFET 18 is switched ON when the signal $AST(=Q)$ becomes logic 1 to separate or disconnect the Schmitt trigger circuit from the voice signal and to connect the input of the Schmitt trigger circuit with V_{DD} . This is so as not to exert the influence of the input impedance of the Schmitt trigger circuit on the voice signal after start of recording. The transmission gate 17 may be omitted if the resistors R_s and R_f are suitably chosen. The timing chart of this auto-start circuit is also illustrated by Figure 2(d).

Figure 3(a) shows part of another embodiment of an electronic timepiece according to the present invention and Figure 3(b) shows a timing chart at the time of start of recording. In this embodiment delta modulation (ΔM) is used as the method of memorising the voice signal. A comparator 31 compares amplitude level of the output of a D/A converter 32 with that of the voice signal. The output of the comparator becomes logic 1 if the voice signal is relatively large, while it becomes logic 0 if the voice signal is relatively small. A control circuit 33 controls data (D_1 to D_n) provided to the converter so that the output level of the converter approaches the amplitude level of the voice signal as far as possible.

In this circuit an initial state is determined by a reset

signal $\overline{R}$ which is the same as that shown in Figures 1 and 2.

Data to determine the output of the converter 32 at the standard voltage V_c is produced as long as the signal AST is logic 0 and operation begins when the signal AST becomes logic 1. A data

5 converting circuit 34 converts data obtained from the comparator 31 into a form which is easily stored in a memory 35. When utilizing, for example, a shift register as the memory 35, the data converting circuit proves unnecessary. An address counter 36 for the memory operates when an output signal $\overline{\text{Reset}}$ of a AND gate 37 becomes
10 logic 1. Thus to operate, both the signal AST and the reset signal $\overline{R}$ must be logic 1 simultaneously. A flip-flop circuit 38 produces a signal applied to terminal D at terminal Q on fall of the signal $\overline{CL}$. Therefore, the level of the voice signal becomes higher than the standard voltage V_c of the converter after the reset signal $\overline{R}$ becomes
15 logic 1, and as soon as the output of the comparator 31 becomes logic 1, the signal AST (=Q) changes to logic 1 to start recording. The comparator 31, the converter 32 and the control circuit 33 together form a level detector and the flip-flop circuit 38 and the AND gate 37 form a start control circuit.

20 Figure 4(a) illustrates a further embodiment of an electronic timepiece according to the present invention and Figure 4(b) is a timing chart illustrating the operation thereof. The electronic timepiece shown in Figure 4(a) also uses delta modulation as the electronic timepiece shown in Figure 3(a) does and like parts in
25 Figures 3(a) and 4(a) have been designated by the same reference

numerals.

A D/A converter control circuit 41 controls data D_1 to D_n provided to the converter 32 so that the output level thereof approaches the amplitude level of the voice signal as closely as possible. The control circuit 41 establishes an initial value during the period when the reset signal $\bar{R}$ is logic 0, and delivers data to make the output of the converter approximately one-half that of the power source. A level detector 42 reads out data from the converter control circuit to the converter, detects from the data what state the output of the converter is in to establish the value of the standard voltage $\pm V_c$ and delivers a trigger signal TRG to the flip-flop circuit 38. The trigger signal TRG is logic 1 when the output of the converter is between $-V_c$ and $+V_c$ and logic 0 when it is above this range. The way in which the converter follows the voice signal as shown in Figures 3(b) and 4(b) is not limited to that described, but variations may be made depending upon the construction of the control circuit.

Figure 5(a) is a block diagram of the recorder 7 of the electronic timepiece of Figure 1 and Figure 5(b) shows one divided form of a RAM memory thereof. Referring first to Figure 5(a), the recorder 7 has a RAM memory 51, a read/write switching circuit and data transformation circuit 52 for transforming data obtained from the code circuit 6 into a signal suitable for being written in the memory and for transforming data read from the memory into a signal suitable for being transferred to the voice synthesizing

circuit 8. A control circuit 53 performs supervisory control of the recorder 7 as a whole. This control circuit includes a circuit for switching memory regions and especially controls addressing. When a signal AST is applied, the address at that point is transferred to an address latch 54. The address latch 54 memorizes the transferred address and returns it to the control circuit 53 when reproducing the voice sound.

Figure 5(b) shows a form of the memory 51 divided into three regions, I, II, III, A0 to A9 being addresses. In this embodiment the first region I is formed of 128 words which correspond to address 000H - 03FH, the second region is formed of 128 words which correspond to address 040H-07FH, the third region III corresponds to the remaining address 080H-3FFH.

When recording, either the first region I or the second region II is selected by the control circuit 53. For instance in the case of selecting the first region I, data which is obtained from the code circuit 6 is stored sequentially in order of address e.g. 00H → 001H → 002H... and when coming to the final address 03FH of the first region I, the data is continued to be written by turning back to the first address of the region I, e.g. 03FH → 000H → 001H... When the data is written to the point P, the signal AST from the auto-start circuit 9 is fed to the control circuit 53 which writes the address XXXH (hereinafter referred to as a record auto-start address) to the address latch 54. Then data is written in the third region III from 080H to 3FFH. After that,

recording is completed by finishing writing. If the recording is started again after the earlier recording is finished, the second region II is selected this time to perform the same recording operation as above. In this way, the regions I and II are switched cyclically.

When reading, the region selected at the time of recording is selected by the control circuit 53 and record auto-start address XXXH memorised in the address latch is set in the control circuit. If the region I is now selected, the control circuit reads out data in order of address that XXXH+001 → XXXH+002 → ... → 03FH → 000H → ... → XXXH → 080H → 081H → ... 3FFH. The data is transformed by the circuit 22, transferred to the voice signal synthesizing circuit and delivered as an audible sound. The memory is addressed from XXXH+001 (next to XXXH) to XXXH by making a round in the region I and transferring to region III.

In the case of selecting the region II, the control circuit controls addresses as follows: XXXH+001H → XXXH+002H → ... → 07FH → 040H → ... → XXXH → 080H → 081H → ... → 3FFH. According to this address order, the foregoing reading operation is performed.

Thus it becomes possible to record the voice by the above writing and reading operation before the record auto-start circuit operates. Therefore the known difficulty that the beginning of the audible sound is broken due to the auto-start function is overcome by simply controlling addressing of the memory so that the auto-start

function is utilised profitably. It will be appreciated that the capacity of the memory regions I, II and III can be freely established in accordance with practical requirements.

- 5 The embodiments of the present invention described above are relatively simple and starting of recording is automatic simultaneously with the start of talking without any complicated switching operations being performed by the user. Thus it is possible to avoid wasting memory capacity which is limited. Further, it becomes possible to memorise only the length of silent
10. or blank time between audible sound without actually producing a blank recording and to synthesize the blank recording from the blank time so reducing by considerable extent the capacity needed for the memory.



-12-

CLAIMS

1. An electronic timepiece including: an oscillator circuit for generating a clock signal; a frequency divider circuit connected to receive the clock signal and to form timing signals; semiconductor recording means for performing reading and writing operations under the control of one of the timing signals, of data relating to an external audible sound; output means for converting data read from the recording means into an audible sound; a level detector for detecting the amplitude of the external audible sound to be recorded; and a start control circuit to control the writing operation of the recording means in dependence upon the output of the level detector.
2. An electronic timepiece as claimed in claim 1 in which the level detector is an operational amplifier and the start control circuit is a set-reset latch.
3. An electronic timepiece as claimed in claim 1 in which the level detector comprises a NAND gate and the start control circuit is a set-reset latch.
4. An electronic timepiece as claimed in claim 1 in which the level detector comprises a Schmitt trigger circuit and the start control circuit is a flip-flop circuit.
5. An electronic timepiece as claimed in any preceding claim including means for converting the external audible sound into a digital data signal for storage in the recording means, the output means including a synthesizing circuit for synthesizing an audible sound from the data read from the recording means.



-13-

6. An electronic timepiece as claimed in any preceding claim, in which the recording means has at least two memory regions, a memory control circuit being arranged to write data in the first of said memory regions before the start control circuit operates and to write the data in a second of said memory regions after the start control circuit has operated.
7. An electronic timepiece substantially as herein described with reference to and as shown in the accompanying drawings.