Claims

What is claimed:

1. A semiconductor device, comprising:

a separation carrier including a temporary base material;

a conductive layer including a plurality of trace lines each in direct contact with the separation carrier and comprising a first terminating end of the trace line with a width equal to a width of the trace line and a contact pad with a width greater than the width of the trace line located at an opposite terminating end of the trace line from the first terminating end of the trace line, wherein the contact pads are offset to reduce pitch between adjacent trace lines;

a semiconductor die including a plurality of contact pads disposed over the first terminating ends of the trace lines;

a plurality of bumps in direct contact with the contact pads of the semiconductor die and the first terminating ends of the trace lines, wherein a width of the bump is greater than the width of the trace line and the bumps overlap a side surface of the trace lines and a terminating side surface of the first terminating ends; and

an encapsulant deposited over the semiconductor die.

2. The semiconductor device of claim 1, further including a plurality of conductive pillars formed over the contact pads of the semiconductor die.

3. The semiconductor device of claim 1, further including an insulating layer contacting the semiconductor die and trace lines.

4. The semiconductor device of claim 3, wherein the insulating layer includes a no-flow underfill material.

5. A semiconductor device, comprising:

a separation carrier including a temporary base material;

a plurality of trace lines formed in contact with the separation carrier and including a first terminating end of the trace line with a width equal to a width of the trace line and a contact pad with a width greater than the width of the trace line located at an opposite terminating end of the trace line from the first terminating end of the trace line;

a semiconductor die disposed over the trace lines;

a plurality of bumps contacting the semiconductor die and the first terminating ends of the trace lines including a terminating side surface of the first terminating ends; and

an encapsulant deposited over the semiconductor die.

6. The semiconductor device of claim 5, further including a plurality of conductive pillars formed over the semiconductor die.

7. The semiconductor device of claim 5, further including an insulating layer contacting the semiconductor die and trace lines.

8. The semiconductor device of claim 5, further including a masking layer over the trace lines with an opening in the masking layer over the first terminating ends of the trace lines.

9. The semiconductor device of claim 1, wherein the encapsulant is deposited over and around the semiconductor die to contact the trace lines.

10. The semiconductor device of claim 5, wherein the contact pads are offset to reduce pitch between adjacent trace lines.

11. The semiconductor device of claim 5, wherein the encapsulant is deposited over and around the semiconductor die to contact the trace lines.