

SOURCE VOLTAGE CONTROL CIRCUIT

The present invention relates to a source voltage control circuit.

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Recently, semiconductor devices have become more and more integrated, so that in a semiconductor device of submicron order, the reduction in device area causes a corresponding increase in the voltage applied thereto, thus affecting the reliability of the device considerably.

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For example, in a MOS (Metal Oxide Semiconductor) transistor, often used for highly integrated semiconductor memory devices, although the external source voltage is maintained at constant value such as 5V, the channel length becomes shortened to less than $1\mu\text{m}$, therefore the drain voltage is increased. Subsequently the punch-through phenomenon occurs, in which the depletion layer near the drain extends to the source region. This phenomenon increases the leakage current between the source and drain, so as to badly affect the operation of a fine MOS transistor of submicron order.

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In addition, the internal field intensity, increased according to the increase of the drain voltage, appears in a depletion layer near the drain, so that some of the carriers get an additional energy, resulting in a hot carrier effect, which involves a change of the threshold value caused by the carriers penetrating the gate oxide layer, an increase in the substrate current caused by impinging ionization and deterioration of the device, etc.

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In order to prevent the reliability of the semiconductor device from being degraded by the punch-through and hot carrier effects, the source

voltage of 5V presently used as the standard source voltage or external source voltage must be dropped to 3.3V.

However, because the change of the voltage level of a system is two
5 to three years slower than the change of a memory chip area, there is required, at the intermediate stage of the change, a source voltage control circuit for dropping the external source voltage to obtain the internal source voltage.

10 Referring to Figure 1 for illustrating a conventional source voltage control circuit, the circuit includes a first and second single-ended N-channel input differential amplifiers 20 and 30 respectively with external input voltages V1 and V2, a feedback circuit 40 with inputs receiving the outputs of the first and second differential amplifiers 20 and 30 and a first output applied to the
15 other input terminals of the first and second differential amplifiers 20 and 30, and a third differential amplifier 50 with a positive input terminal connected to a first output node 47 of the feedback circuit 40 and a negative input terminal connected to the output 51 thereof.

20 The first and second differential amplifiers 20, 30 include first NMOS transistors 23, 34 with the gates respectively connected to the input voltages V1 and V2, second NMOS transistors 24, 33 with the gates commonly connected to the second output node 48 of the feedback circuit 40, separate current sources 25, 35 respectively connected between the sources of the first
25 and second NMOS transistors 23 and 24, 33 and 34 and a ground voltage terminal, first and second PMOS transistors 21 and 22, 31 and 32 connected to an external source voltage terminal, and output nodes 26, 36 between the first PMOS transistors 21, 32 and the first NMOS transistors 23, 34.

The feedback circuit 40 includes a third and fourth PMOS transistors 41 and 42 with the channels connected between the external source voltage terminal and a first output node 47 and the gates respectively connected to the outputs of the first and second differential amplifiers 20 and 30, a first resistor 45 connected between the first output node 47 and a second output node 48 commonly connected to the gates of the second NMOS transistors 24, 33 of the first and second differential amplifiers 20 and 30, and a second resistor 46 connected between the second output node 48 and ground voltage terminal. The feedback circuit 40 produces a reference voltage V_{ref} at the first output node 47 between the second PMOS transistors 41, 42 and the first resistor 45, and feeds back the voltage divided by the first and second resistors 45 and 46 to the other inputs of the first and second differential amplifiers 20 and 30.

The third differential amplifier 50 receives the reference voltage V_{ref} from the feedback circuit 40 through the positive input, thus producing an internal source voltage that is equal to the reference voltage V_{ref} .

Figure 2 is a graph for illustrating the internal source voltage against the external source voltage for a conventional source voltage control circuit.

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The horizontal axis represents the external source voltage, and the vertical axis the internal source voltage. There is shown the internal source voltage "c" according to the change of the two input voltages a and b. For descriptive convenience, the external source voltage is divided into three intervals which include the first interval 60 below 3.3V, the second interval 61 from 3.3V to 6.6V, and the third interval 62 over 6.6V.

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The operation of the conventional source voltage control circuit will now be described with reference to Figures 1 and 2. The first and second differential amplifiers 20 and 30 receive the externally applied voltages V1 and V2 respectively through the gates of the first NMOS transistors 23 and 34, and the voltage $R2/(R1+R2) \times V_{ref}$ divided by the first and second resistors 45 and 46 through the gates of the second NMOS transistors 24, 33. Thus, the NMOS transistor which receives a higher voltage is more turned-on, producing a "low" or "high" output state at the output nodes 26, 36.

10 The outputs at the output nodes 26, 36 control the current-passing capability of the third and fourth PMOS transistors 41, 42, so as to produce a desired reference voltage V_{ref} at the first output node 47.

When the external source voltage is within the first interval 60 below 3.3V, one input voltage V1 of the first differential amplifier 20 is greater than one input voltage V2 of the second differential amplifier 30 as shown in Figure 2. Thus, until the other input voltage $R2/(R1+R2) \times V_{ref}$ becomes equal to the input voltage V1, the first NMOS transistor 23 of the first differential amplifier 20 is turned on, so as to turn on the third PMOS transistor 41 of the feedback circuit 40. Thus, the reference voltage V_{ref} from the first output node 47 is increased in proportion to the externally applied source voltage.

25 Meanwhile, when the external source voltage is within the second interval 61 of 3.3V to 6.6V, the one input voltage V1 of the first differential amplifier 30 is greater than the one input Voltage V2 of the second differential voltage 30. Thus, until the other input voltage $R2/(R1+R2) \times V_{ref}$ of the first and second differential amplifier 20, 30 becomes equal to the one input

voltage V_1 of the first differential amplifier 20, the first differential amplifier 20 keeps on operating. Hence, the reference voltage V_{ref} may be obtained from the expression $(R_1 + R_2/R_2) \cdot V_1$. In this case, because the voltage V_1 is constant, the reference voltage V_{ref} becomes to have a constant value
5 regardless of the increase of the external source voltage. Thus, the internal source voltage $V_{int} V_{cc}$ has a constant value of 3.3V.

When the external source voltage is within the third interval 62 over 6.6V, the one input voltage V_2 of the second differential amplifier 30
10 becomes greater than the one input voltage V_1 of the first differential amplifier 20. Thus, until the other input voltage $R_2/(R_1 + R_2) \times V_{ref}$ of the first and second differential amplifier 20, 30 becomes to equal the one input voltage V_2 of the second differential amplifier 30, the second differential amplifier 30 keeps on operating as the main differential amplifier. In this
15 case, the reference voltage V_{ref} is proportional to V_2 so as to be increased with a constant slope according to the increase of V_2 .

As described above, it is very important to increase the internal source voltage for the reliability of a semiconductor device when the external voltage gets over a specified value (6.6V), and the limit of the internal source voltage
20 depends on the whole characteristics of the semiconductor memory device. Hence, the slope of the internal source voltage should be readily adjusted when the external source voltage gets over a specified value.

25 However, in order to adjust the slope of the internal source voltage according to the conventional source voltage control circuit, it is necessary to change both of the input voltages V_1 and V_2 of the first and second

differential amplifiers 20 and 30 and the first and second resistors 45 and 46 of the feedback circuit 40, thereby resulting in difficulty.

Furthermore, the current consumed by the reference voltage generating circuit 10 of the conventional source voltage control circuit during the stand-by is the sum of the current flowing through the first and second resistors 45 and 46 of the feedback circuit 40 and the current resulting from the input voltages V1 and V2 of the first and second differential amplifiers 20 and 30. Hence, although the stand-by current of a semiconductor memory device should be maintained very small, it becomes very large because the conventional reference voltage generating circuit itself includes a differential amplifier.

It is an object of the present invention to provide a source voltage control circuit for readily adjusting the slope of the internal source voltage response when the external source voltage gets over a specified value.

It is another object of the present invention to provide a source voltage control circuit for minimizing the stand-by current.

According to a first aspect of the present invention, a source voltage control circuit is provided comprising:

reference voltage generating means connected to an external source voltage terminal for generating a constant reference voltage;

source voltage level sensing means connected to said external source voltage terminal for increasing an internal source voltage in proportion to an increase in said external source voltage when said external source voltage is equal to or greater than a given voltage;

first differential amplifying means with two inputs receiving respectively the outputs of said reference voltage generating means and of said internal source voltage controlled by a first control signal and the output of said source voltage level sensing means; and

5 second differential amplifying means with two inputs receiving the outputs of said reference voltage generating means and said internal source voltage controlled by a second control signal.

According to a second aspect of the invention, there is provided a
10 source voltage control circuit comprising:

reference voltage generating means comprising: a first NMOS transistor and diode-connected PMOS transistor with the channels connected in series between external source voltage terminal and ground voltage terminal; an output node connected to the gate of said first NMOS transistor; and a driving
15 PMOS transistor with the channel connected between said external source voltage terminal and output node and the gate connected to the gate of said PMOS transistor:

first differential amplifying means comprising: a first single-ended
20 N-channel input differential amplifier with two inputs receiving the reference voltage of said output node and internal source voltage; a PMOS transistor with the channel connected between said external source voltage terminal and the output node of said first differential amplifier and the gate connected to a first control signal; a first and second current pass transistors, with the
25 channels connected in series between said output node and said ground voltage terminal and the gates respectively connected to the external source voltage dropped by a given value and said first control signal; and a driving transistor with the channel connected between said external source voltage terminal and

said internal source voltage terminal and the gate connected to said output node; and

second differential amplifying means comprising: a second single-ended
5 N-channel input differential amplifier with two input receiving said reference voltage and said internal source voltage; an NMOS transistor with the channel connected between said external source voltage terminal and the output node of said second differential amplifier and the gate connected to said second control signal; and a driving transistor with the gate connected to said output
10 node and the channel connected between said external source voltage terminal and said internal source voltage terminal.

According to a third aspect of the invention, there is provided a source voltage control circuit comprising:

15 reference voltage generating means:

plurality of differential amplifying means for active operation and a differential amplifying means for stand-by operation connected between an output node of said reference voltage generating means and internal source
20 voltage terminals respectively; and

gating means with the channels respectively connected between the adjacent ones of said internal voltage terminals and the gates connected to a first control signal.

25 The present invention will now be described more specifically with reference to the drawings attached only by way of example.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example only, to the accompanying diagrammatic drawings, in which:

5 Figure 1 is a circuit diagram of a conventional circuit having a reference voltage and an external source voltage;

Figure 2 is a graph illustrating reference voltage against external source voltage, for the circuit shown in Figure 1;

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Figure 3 is a circuit diagram embodying the present invention;

Figure 4 is a graph illustrating an internal source voltage against an external source voltage for the circuit shown in Figure 3;

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Figure 5 is a timing diagram for the circuit shown in Figure 3; and

Figure 6 is a further embodiment of the present invention.

20 A source voltage control circuit is shown in Figure 3, having a reference voltage generating circuit 70, a source voltage level sensing circuit 90, a first differential amplifying circuit 110 and a second differential amplifying circuit 130. The first differential amplifying circuit 110 receives two inputs consisting of the output voltage V_{ref} of the reference voltage
25 generating circuit 70 and the internal source voltage $Int\ V_{cc}$, controlled by a first control signal 125 and the source voltage level sensing circuit 90. The output of the first differential amplifying circuit 110 is connected to an internal source voltage terminal 122. The second differential amplifying

circuit 130 receives two inputs consisting of the output voltage of the reference voltage generating circuit 70 and the internal source voltage, controlled by a second control signal 145. The output of the second differential amplifying circuit is connected to the internal source voltage
5 terminal 122.

The reference voltage generating circuit 70 includes a plurality of transistors. The channels of a first NMOS transistor 73 and first PMOS transistor 74 are connected in series between the external source voltage
10 terminal and a control node 71. Between the control node 71 and ground voltage terminal is connected, in parallel, a resistor 80 and second diode-connected PMOS transistor 81. There is provided a driving PMOS transistor 75 with the channel connected between the external source voltage terminal and the output node 72 and the gate connected to the control node
15 71. There are also provided a plurality of third to sixth diode-connected PMOS transistors 76- 79 connected in series between the output node 72 and the ground voltage terminal. The gate of the first NMOS transistor 73 is connected to the output node 72, and the gate of the first PMOS transistor 74 to the control node 71.

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The reference voltage generating circuit 70 always generates a constant reference voltage V_{ref} by controlling the gate voltage of the driving PMOS transistor 75 according to the voltage of the control node 71. The output node 72 is connected to the gate of the first NMOS transistor 73 so as to feed back
25 the reference voltage V_{ref} . Thus, the voltage of the control node 71 is controlled according to the changes of the reference voltage which in turn is caused by the changes of the parameters such as temperature, etc., so that the current pass capability of the driving PMOS transistor 75 may be adjusted.

The driving PMOS transistor 75 serves to charge the output node 72. The second PMOS transistor 81 serves as a pull-down transistor with a gate connected to the ground voltage terminal. Thus, when the external source voltage exceeds the threshold voltage of the first NMOS transistor 73 and the first and second PMOS transistor 74 and 81, the second PMOS transistor 81 is turned on to have the characteristics of a resistor.

The source voltage level sensing circuit 90 includes a first group of diode-connected NMOS transistors 92-96 connected in series between the external source voltage terminal and a sensing node 91. A resistor 102 is connected between the sensing node 91 and the ground voltage terminal. There are provided a second group of diode-connected NMOS transistors 97, 98 connected in series to the sensing node 91. There is also provided a second NMOS transistor 99 with the channel connected between the NMOS transistor 98 and the ground voltage terminal and the gate connected to the first control signal 125. A third NMOS transistor 100 has the gate and drain connected to the sensing node 91. A fourth NMOS transistor 101 has the channel connected between the source of the third NMOS transistor 100 and the ground voltage terminal and the gate connected to the first control signal 125.

The first group of diode-connected NMOS transistors 92-96 serve to detect the external source voltage level so as to drop the external source voltage by the threshold voltage proportional to the number of the NMOS transistors. The dropped external source voltage is applied to the sensing node 91.

The first differential amplifying circuit 110 includes a first single-ended N-channel input differential amplifier 105 consisting of a seventh and eighth PMOS transistors 113 and 114 and a fifth to seventh NMOS transistors 115, 116 and 117. There is also provided a ninth PMOS transistor 120 with the channel connected between the output node 111 of the first differential amplifier 105 and the external source voltage terminal and the gate connected to the first control signal 125. An eighth and ninth NMOS transistors 118 and 119 are connected in series between the output node 111 and the ground voltage terminal with the gates respectively connected to the sensing node 91 of the source voltage level sensing circuit 90 and the first control signal 125. A tenth PMOS transistor 121 is provided with the gate connected to the output node 111 and the channel connected between the external source voltage terminal and internal source voltage terminal 122.

The gate of the seventh NMOS transistor 117 is supplied with the first control signal 125. The two inputs of the first differential amplifier 105 are the gate of the fifth NMOS transistor 115 connected to the output node 72 of the reference voltage generating circuit 70 and the gate of the sixth NMOS transistor 116 connected to the internal source voltage terminal 122.

The second differential amplifying circuit 130 includes a second single-ended N-channel input differential amplifier 138 consisting of an eleventh and twelfth PMOS transistors 132 and 133 and a tenth to twelfth NMOS transistors 135, 136 and 137. There is also provided a thirteenth NMOS transistor 139 with the channel connected between the external source voltage terminal and the output node 131 of the second differential amplifier 138 and the gate connected to a second control signal 145. A thirteenth PMOS transistor 140 is also provided with the channel connected between the

external source voltage terminal and the internal source voltage terminal 122 and the gate connected to the output node 131.

5 The second differential amplifier 138 has two inputs consisting of the gate of the tenth NMOS transistor 135 connected to the output node 72 of the reference voltage generating circuit 70 and the gate of the eleventh NMOS transistor 136 connected to the internal source voltage terminal 122. The gate of the twelfth NMOS transistor 137 and the gate of the tenth NMOS transistor 135 are commonly connected to the output node 72 of the reference voltage
10 generating circuit 70.

Referring to Figure 4, there is shown a graph for illustrating the reference voltage against the changes of the externally applied source voltage. The horizontal axis represents the external source voltage and the vertical axis
15 the internal source voltage. The reference letters a, b, c indicate the internal source voltages having different slopes from each other, while d indicates the stand-by internal source voltage which is at the same time the reference voltage of the reference voltage generating circuit.

20 With reference to the desired value 3.3V and a specified value 7V of the internal voltage, the external source voltage is divided into three intervals of which the first interval 150 is below 3.3V, the second interval 151 is from 3.3V to 7V and the third interval 152 is over 7V.

25 In Figure 5, A shows a timing diagram for an external chip selection signal, B a timing diagram for the first control signal applied to the first differential amplifying circuit and C a timing diagram for the second control signal applied to the second differential amplifying circuit.

When the external chip selection signal A is in its "low" state, the first control signal B is placed in its "high" state so as to enable the first differential amplifying circuit 110, so that the source voltage control circuit gets into the active period 155. On the other hand, when the external chip selection signal A is in its "high" state, the second control signal C is placed in its "low" state, so as to enable the second differential amplifying circuit 130, so that the source voltage control circuit gets into the stand-by period 156.

10 The operation of the source voltage control circuit embodying the present invention, will now be described in detail with reference to Figures 3, 4 and 5.

When the external source voltage is within the first interval 150, namely, smaller than the desired value 3.3V, the gate of the driving PMOS transistor 75 makes a complete connection with ground, by way of the resistor 80 of the reference voltage generating circuit 70. Accordingly, the driving PMOS transistor 75 is completely turned on, so that the reference voltage V_{ref} of the output node 72 depends on the external source voltage V_{cc} .

20 If the external source voltage gradually increases and gets into the second interval 151, the gate voltage of the driving PMOS transistor 75 is increased by the current flowing through the resistor 80 and second PMOS transistor 81. Accordingly, the current pass capability of the driving PMOS transistor 75 is lowered, so that the reference voltage V_{ref} of the output node 72 maintains a constant value of 3.3V, regardless of the increase of the external voltage.

Namely, as the external source voltage increases over 3.3V, the current pass capability of the driving PMOS transistor 75 is correspondingly lowered, so that the reference voltage V_{ref} of the output node 72 maintains a constant value of 3.3V as shown in Figure 4(d).

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On the other hand, if the reference voltage V_{ref} suffers a variation due to temperature or other parameters, the variation is fed back from the output node 72 to the gate of the first NMOS transistor 73, and again negatively fed back through the first PMOS transistor 74 to the driving PMOS transistor 75, thus minimizing the variation of the reference voltage V_{ref} .

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Namely, when the reference voltage is increased over the desired value, the high voltage applied to the gate of the first NMOS transistor 73 causes the first NMOS transistor 73 to be more turned on. Accordingly, the voltage applied to the control node 71 is increased so as to lower the current pass capability of the driving PMOS transistor 75, so that the reference voltage of the output node 72 maintains a constant value.

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Likewise, the same operating principle is applied to the case when the reference voltage is decreased below the desired value. The constant reference voltage of the output node 72 serves as first input of the first and second differential amplifying circuit 110, 130, and in the active operation, the first control signal 125 in its "high" state causes the first differential amplifying circuit 110 to be operated. In the stand-by operation, the second control signal 145 in its "low" state causes the second differential amplifying circuit 130 to be operated.

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In active operation, as the first control signal 125 enters its "high" state, the seventh NMOS transistor 117 of the first differential amplifier 105 is turned on, so as to enable said first differential amplifier 105. On the other hand, the ninth PMOS transistor 120 is turned off by the first control signal 125 in its "high" state, so as to turn on the first differential amplifying circuit 110.

If the external source voltage is within the first interval 150 of Figure 4, the fifth NMOS transistor 115 of the first differential amplifier 105 is more and more turned on in proportion to the increase of the reference voltage of the output node 72. Accordingly, the voltage level of the output node 111 of the first differential amplifier 105 is gradually lowered so as to increase the current pass capability of the tenth PMOS transistor 121, so that there is obtained the internal voltage in proportion to the external source voltage applied to the source of the tenth PMOS transistor 121.

Further, if the external source voltage is within the second interval 151 of Figure 4, a constant reference voltage is applied to the gate of the fifth NMOS transistor 115 of the first differential amplifier 105, so that the current flowing through the fifth and sixth NMOS transistors 115 and 116 is maintained constant. Thus, a constant voltage is applied to the gate of the tenth PMOS transistor 121, so that even if the external source voltage is increased, the constant current pass capability causes the stable internal voltage.

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Although the semiconductor memory device should keep a stable internal source voltage in a normal mode, regardless of the external source voltage variation, it is necessary to increase the internal source voltage in

order to test the reliability of the semiconductor device over a specified value of the external source voltage.

5 In the present embodiment, when the external source voltage exceeds 7V, the internal source voltage is caused to increase. When the external source voltage is within the third interval 152 of Figure 4 exceeding 7V, the voltage of the sensing node 91 of the source voltage level sensing circuit 90 has a value high enough to turn on the eighth NMOS transistor 118 connected to the sensing node 91.

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Hence, the current at the output node 111 of the first differential amplifier 105 flows into the fifth NMOS transistor 115 as well as the eighth and ninth NMOS transistors 118 and 119, so that the tenth PMOS transistor 121 with the gate connected to the output node 111 is more and more turned on. Thus, the internal voltage terminal 122 has the linearly increased source voltage.

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Meanwhile, if the slope of the internal voltage is to be adjusted over a specified value of the external voltage in the light of the characteristics of each of the semiconductor memory chips, it is only required to change the size of the eighth NMOS transistor 118 whose current pass capability depends on the voltage of the sensing node 91, thereby much facilitating the adjustment compared to the conventional source voltage control circuit.

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25 In the second differential amplifying circuit 130, the second control signal 145, disabled into its "high" state, causes the thirteenth NMOS transistor 139 to be turned on. Consequently, the output node 131 of the second differential amplifier 138 is freely charged with $V_{CC}-V_{TN}$ (V_{TN} being

the threshold voltage of the NMOS transistor), so that the thirteenth PMOS transistor 140 is maintained turned off. Thus, the possibility of the internal source voltage, caused by the operation of the first differential amplifying circuit 110, being fed back through the thirteenth PMOS transistor 140 to the second differential amplifying circuit 130 is prevented. Here, the second differential amplifying circuit 130 has a very small size compared to the first amplifying circuit 110 in order to minimize the stand-by current, and has a very slow response speed of a few microsecond.

10 If the internal source voltage is increased due to a certain factor, the sixth NMOS transistor 116 of the first differential amplifying circuit 110 is turned on, so that the output of the output node 111 enters it "high" state. Accordingly, the tenth PMOS transistor 121 is turned off, thus preventing the internal source voltage from increasing further. Meanwhile, the second differential amplifying circuit 130 requires a certain delay time to be completely turned on, because the response speed of the eleventh NMOS transistor 136 is slow. At this time, if there does not exist the thirteenth NMOS transistor 139, the output of the output node 131 is maintained in its "low" state during the delay time, so as to turn on the thirteenth PMOS transistor 140. Therefore, the phenomenon may occur that the internal source voltage increases according to an increase of the external source voltage.

25 However, the inventive circuit introduces the thirteenth NMOS transistor 139 to be turned on in the active operation to turn off the thirteenth PMOS transistor 140. Thus, only the first differential amplifying circuit 110 is operated in the active operation.

Next, in the stand-by operation of the source voltage control circuit, the second control signal 145 of the chip selection buffer is changed from its "high" state to its "low" state, so that the thirteenth NMOS transistor 139 of the second differential amplifying circuit 130 is turned off. Accordingly, when the external source voltage is within the second interval in the active operation, the second differential amplifying circuit becomes to have the same structure as the first differential amplifying circuit 110, thus maintaining a stable internal voltage based on the same operating principle. Furthermore, even if the external source voltage exceeds a specified value 7V, the current pass capability of the thirteenth PMOS transistor 140 is always maintained constant because there is no other current pass circuit such as the eighth NMOS transistor 118 of the first differential amplifying circuit 110. Therefore, even if the external source voltage continues to increase over a specified value (7V), the internal voltage is maintained at a stable voltage of 3.3V.

Meanwhile, in the first differential amplifying circuit 110, as the first control signal 125 of the chip selection buffer is disabled into "low" state, the ninth PMOS transistor 120 is turned on. Thus, the external source voltage V_{cc} is directly applied to the gate of the tenth PMOS transistor 121 thereby turning off the first differential amplifying circuit 110.

Moreover, as shown in Figure 5, passing from the active period 155 to the stand-by period 156, the first control signal A directly passes from its "low" state into its "high" state, but the second control signal B passes from its "high" state through a given delay time T_d into its "low" state. Thus, even while all the signals within the semiconductor memory device are disabled, the first differential amplifying circuit 110 is operated during the delay time

Td, so as to prevent the dropping of the internal voltage due to the stand-by current. Therefore, a stable operation both in the stand-by operation and in the active operation, is obtained.

5 Referring to Figure 6, there is shown a block diagram for illustrating the reference voltage generating circuit, and the first and second differential amplifying circuits, according to the present invention. The same reference numerals as in Figure 3 are used for the same parts. The first and second differential amplifying circuits are respectively used for the active and
10 stand-by operations.

There are provided a first, second, third differential amplifying circuit 110, 150, 160 for the active operation and a differential amplifying circuit 130 for the stand-by operation, each being connected between the output node 72
15 of the reference voltage generating circuit 70 and the internal source voltage terminals 122, 231, 241, respectively. A first PMOS transistor 251 is provided with its channel connected between the internal source voltage terminals 122 and 231 and its gate connected to the first control signal 125. A second PMOS transistor 252 is provided with the channel connected
20 between the internal source voltage terminals 231 and 241 and the gate connected to the first control signal 125.

The output terminal of the differential amplifying circuit 130 for the stand-by operation is connected to the internal source voltage terminal 122 of
25 the first differential amplifying circuit 110 for the active operation.

In a conventional memory device, in order to prevent noises and to improve the reliability, there is often provided a source voltage control circuit,

wherein the differential amplifiers are separated according to each of the internal source lines. However, a problem with this type of circuit is that the stand-by current increases as the number of the stand-by differential amplifiers increases.

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In the present invention, the first and second PMOS transistors 251 and 252 with the gates connected to the first control signal 125 of the chip selection buffer are employed to connect each of the internal source lines in order to prevent noises and to improve the reliability.

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Thus, in the active operation, the first and second PMOS transistors 251 and 252 are turned off by the first control signal 125 of "high" state, so that the internal source lines are separated from each other. In the stand-by operation, the first control signal 125 is changed into its "low" state, to turn on the first and second PMOS transistors 251 and 252, thereby connecting the internal source lines with each other. Therefore, in the active operation, the internal source lines are separated from each other so as to prevent noises and to improve reliability, while in the stand-by operation said lines are connected to the internal source lines with each other so as to minimize the stand-by current.

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As described above, according to the inventive source voltage control circuit, an NMOS transistor 118 with the gate connected to the sensing node 91 of the source voltage level sensing circuit 90 is connected to the output node 111 of the first differential amplifier 110 with an input receiving the reference voltage V_{ref} , so that in the case that the external source voltage over a specified value is applied, the current pass capability of the NMOS transistor is increased so as to linearly increase the internal source voltage.

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Hence, in order to adjust the slope of the internal source voltage over a specified external source voltage, it is necessary to change one input voltages of the two differential amplifiers and the first and second resistors in the conventional circuit, but the inventive circuit only requires the size of the NMOS transistor to be adjusted. Thus, the slope of the internal voltage may be very easily adjusted.

Further, the conventional source voltage control circuit requires the reference voltage generating circuit to include a differential amplifier which consumes a large current, but the reference voltage generating circuit of the inventive circuit is not a differential amplifier and is always made to have a constant voltage, thereby considerably reducing the stand-by current.

In addition, the inventive circuit negatively feeds back the reference voltage to the reference voltage generating circuit, thus minimizing the variation of the reference voltage due to temperature or other parameters.

Moreover, according to the present invention, the internal source lines are connected by PMOS transistors, so that the internal source lines can be separated from each other in the active operation, and are all connected with each other in the stand-by operation. Accordingly, the noises of the semiconductor are prevented, the reliability thereof improved, and the stand-by current minimized.

The foregoing description shows only a preferred embodiment of the present invention. Various modifications are apparent to those skilled in the art without departing from the scope of the present invention which is only

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limited by the appended claims. Therefore, the embodiment shown and described is only illustrative, not restrictive.

CLAIMS

1. A source voltage control circuit comprising:
 - reference voltage generating means connected to an external source
 - 5 voltage terminal for generating a constant reference voltage;
 - source voltage level sensing means connected to said external source voltage terminal for increasing an internal source voltage in proportion to an increase in said external source voltage when said external source voltage is equal to or greater than a given voltage;
 - 10 first differential amplifying means with two inputs receiving respectively the outputs of said reference voltage generating means and of said internal source voltage controlled by a first control signal and the output of said source voltage level sensing means; and
 - second differential amplifying means with two inputs receiving the
 - 15 outputs of said reference voltage generating means and said internal source voltage controlled by a second control signal.
2. A source voltage circuit control circuit as claimed in Claim 1, wherein said reference voltage generating means comprises:
 - 20 a first NMOS transistor and diode-connected PMOS transistor connected in series between said external source voltage and a control node;
 - a resistor and pull-down PMOS transistor connected in parallel between said control node and ground voltage terminal;
 - an output node connected to the gate of said first NMOS transistor; and
 - 25 a driving PMOS transistor with the channel connected between said external source voltage terminal and said output node and the gate connected to said control node.



3. A source voltage control circuit as claimed in Claim 2, wherein said reference voltage generating means further comprises a current path means including a plurality of diode-connected PMOS transistors connected between said output node and ground voltage terminal.

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4. A source voltage control circuit as claimed in Claim 1, wherein said source voltage level sensing means comprises:

voltage drop means connected in series between said external source voltage terminal and a sensing node:

10 a resistor connected between said sensing node and ground voltage terminal;

diode-connected NMOS transistors connected in series to said sensing node;

15 a second NMOS transistor with the channel connected between said transistor and ground voltage terminal and the gate connected to said first control signal;

a third diode-connected NMOS transistor connected to said sensing node; and

20 a fourth NMOS transistor with the channel connected between the source of said third NMOS transistor and ground voltage terminal and the gate connected to said first control signal.

5. A source voltage control circuit as claimed in Claim 1, wherein said first differential amplifying means comprises:

25 a first single-ended N-channel input differential amplifier with two inputs receiving the voltage of the output node of said reference voltage generating means and said internal source voltage;



a fifth PMOS transistor with the channel connected between said external voltage terminal and the output node of said first differential amplifier and the gate connected to said first control signal;

an eighth and ninth NMOS transistors with the channels connected in series between said output node and ground voltage terminal and the gates respectively connected to said sensing node and said first control signal; and

a sixth PMOS transistor with the channel connected between said external source voltage terminal and said internal source voltage terminal and the gate connected to said output node.

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6. A source voltage control circuit as claimed in Claim 5, wherein said first differential amplifier is controlled by said first control signal.

7. A source voltage control circuit as claimed in Claim 1, wherein said second differential amplifying means comprises:

a second single-ended N-channel input differential amplifier with two input receiving the voltage of the output node of said reference voltage generating means and said internal source voltage;

a thirteenth NMOS transistor with the channel connected between said external source voltage terminal and the output node of said second differential amplifier and the gate connected to said second control signal; and

a ninth PMOS transistor with the gate connected to said output node and the channel connected between said external source voltage terminal and internal source voltage terminal.

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8. A source voltage control circuit as claimed in Claim 7, wherein said second differential amplifier is controlled by the output of said reference voltage generating means.



9. A source voltage control circuit as claimed in Claim 1, wherein said first differential amplifying means is enabled by said first control signal of "high" state so as to perform active operation, while said second differential amplifying means is enabled by said second control signal of "low" state so as to perform stand-by operation.

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10. A source voltage control circuit as claimed in Claim 9, wherein said source voltage control circuit is changed from the active mode to the stand-by mode after a given delay time of said first control signal.

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11. A source voltage control circuit comprising:

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reference voltage generating means comprising: a first NMOS transistor and diode-connected PMOS transistor with the channels connected in series between external source voltage terminal and ground voltage terminal; an output node connected to the gate of said first NMOS transistor; and a driving PMOS transistor with the channel connected between said external source voltage terminal and output node and the gate connected to the gate of said PMOS transistor;

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first differential amplifying means comprising: a first single-ended N-channel input differential amplifier with two inputs receiving the reference voltage of said output node and internal source voltage; a PMOS transistor with the channel connected between said external source voltage terminal and the output node of said first differential amplifier and the gate connected to a first control signal; a first and second current pass transistors, with the channels connected in series between said output node and said ground voltage terminal and the gates respectively connected to the external source voltage dropped by a given value and said first control signal; and a driving transistor

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with the channel connected between said external source voltage terminal and said internal source voltage terminal and the gate connected to said output node; and

5 second differential amplifying means comprising: a second single-ended N-channel input differential amplifier with two input receiving said reference voltage and said internal source voltage; an NMOS transistor with the channel connected between said external source voltage terminal and the output node of said second differential amplifier and the gate connected to said second
10 control signal; and a driving transistor with the gate connected to said output node and the channel connected between said external source voltage terminal and said internal source voltage terminal.

12. A source voltage control circuit as claimed in Claim 11, wherein
15 said reference voltage generating means further comprises:

 a resistor and pull-down PMOS transistor connected in parallel between the drain of said PMOS transistor and said ground voltage terminal; and
 current path means between said output node and said ground voltage
terminal.

20 13. A source voltage control circuit as claimed in Claim 12, wherein said current path means comprises a plurality of diode- connected PMOS transistors.

25 14. A source voltage control circuit as claimed in Claim 11, further comprising a source voltage level sensing means connected between the gate of said first current path transistor and said external source voltage terminal.



15. A source voltage control circuit as claimed in Claim 14, wherein said source voltage level sensing means comprises:

a plurality of diode-connected NMOS transistors connected in series between said external source voltage terminal and a sensing node;

5 a resistor connected between said sensing node and said ground voltage terminal;

diode-connected NMOS transistors connected in series to said sensing node;

10 an NMOS transistor with the channel connected between said transistor and said ground voltage terminal and the gate connected to said first control signal;

a diode-connected NMOS transistor connected in series between said sensing node and said ground voltage terminal; and

15 an NMOS transistor with the gate connected to said first control signal.

16. A source voltage control circuit as claimed in Claim 11, wherein said first and second current path transistors are NMOS type.

20 17. A source voltage control circuit as claimed in Claim 16, wherein the driving transistors of said first and second differential amplifying means are PMOS.

25 18. A source voltage control circuit as claimed in Claim 17, wherein the internal voltage slope at said internal source voltage terminal is controlled by adjusting the size of said first current path transistor when said external source voltage is equal to or greater than a specified value.



19. A source voltage control circuit as claimed in Claim 11, wherein said first differential amplifying means is enabled by said first control signal of "high" state so as to perform active operation, while said second differential amplifying means is enabled by said second control signal of "low" state so as to perform stand-by operation.

20. A source voltage control circuit as claimed in Claim 19, wherein said source voltage control circuit is changed from the active mode to the stand-by mode after a given delay time of said first control signal.

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21. A source voltage control circuit as claimed in Claim 20, wherein said first differential amplifying means is disabled when said driving transistor performs the stand-by operation.

22. A source voltage control circuit as claimed in Claim 20, wherein said second differential amplifying means is disabled when said driving transistor performs the active operation.

23. A source voltage control circuit comprising:
reference voltage generating means;
plurality of differential amplifying means for active operation and a differential amplifying means for stand-by operation connected between an output node of said reference voltage generating means and internal source voltage terminals respectively; and

gating means with the channels respectively connected between the adjacent ones of said internal voltage terminals and the gates connected to a first control signal.



24. A source voltage control circuit as claimed in Claim 23, wherein said gating means are PMOS transistors.

5 25. A source voltage control circuit as claimed in Claim 24, wherein said gating means are turned off in active mode and turned on in stand-by mode.

26. A source voltage control circuit substantially as herein described with reference to Figure 3.

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