WHAT IS CLAIMED IS:

1. A reference voltage circuit comprising:

a first current bias circuit comprising a first node;

a second current bias circuit comprising a plurality of NMOS transistors and a second node, wherein the plurality of NMOS transistors comprises a first NMOS transistor and a second NMOS transistor, the first NMOS transistor is connected to the first node, and at least two of the plurality of NMOS transistors are connected to the second node and configured to perform a sub-threshold operation based on a first voltage of the first node so that a second voltage is generated at the second node; and

an amplifier configured to output a reference voltage having same value as the second voltage.

2. The reference voltage circuit of claim 1, wherein the first current bias circuit is configured to generate the first voltage of the first node based on a first current having a complementary to absolute temperature (CTAT) characteristic.

3. The reference voltage circuit of claim 1 or claim 2, wherein the first current bias circuit comprises a PNP bipolar transistor comprising an emitter, a base, and a collector, wherein the emitter is connected to the first node and the base and the collector are connected to a ground voltage, and

wherein a base-emitter voltage of the PNP bipolar transistor is provided as the first voltage of the first node.

4. The reference voltage circuit of any one of claims 1 to 3, wherein the first current bias circuit comprises a diode comprising an anode, to which the first node is connected, and a cathode, to which a ground voltage is connected, and

wherein a forward direction voltage of the diode is provided as the first voltage of the first node.

5. The reference voltage circuit of any one of claims 1 to 4, wherein the amplifier is further configured to generate an output current having a same value as a current flowing in the first current bias circuit.

6. The reference voltage circuit of any one of claims 1 to 5, wherein a first current path comprises the second node, and

wherein the amplifier comprises a second current path comprising a third node, which is symmetrical to the second node and which is an output node of the reference voltage circuit and outputs the reference voltage.

7. The reference voltage circuit of any one of claims 1 to 6, wherein the second current bias circuit is configured to generate the second voltage based on a current having a proportional to absolute temperature (PTAT) characteristic.

8. The reference voltage circuit of any one of claims 1 to 7, wherein the first NMOS transistor comprises a first NMOS transistor gate, to which the first node is connected, a first NMOS transistor drain, to which a power voltage is connected, and a first NMOS transistor source, and

wherein the second NMOS transistor comprises a second NMOS transistor gate, a second NMOS transistor drain, and a second NMOS transistor source, to which a ground voltage is connected, wherein the first NMOS transistor source is connected to the second NMOS transistor gate and the second NMOS transistor drain.

9. The reference voltage circuit of claim 8, wherein a connection node between the first NMOS transistor and the second NMOS transistor is the second node and outputs the second voltage.

10. The reference voltage circuit of claim 8 or claim 9, wherein the second current bias circuit further comprises:

a third NMOS transistor comprising a third NMOS transistor gate, to which the second NMOS transistor gate and the second NMOS transistor drain, a third NMOS transistor drain are connected, to which the power voltage is connected, and a third NMOS transistor source, and

a fourth NMOS transistor comprising a fourth NMOS transistor gate and a fourth NMOS transistor drain, and a fourth NMOS transistor source, to which the ground voltage is connected, wherein the third NMOS transistor source is connected to the fourth NMOS transistor gate and the fourth NMOS transistor drain.

11. The reference voltage circuit of claim 10, wherein the second node is between the third NMOS transistor and the fourth NMOS transistor.

12. The reference voltage circuit of claim 10 or claim 11, wherein the second current

bias circuit further comprises:

a fifth NMOS transistor comprising a fifth NMOS transistor gate, to which the fourth NMOS transistor gate and the fourth NMOS transistor drain are connected, a fifth NMOS transistor drain, to which the amplifier is connected, and a fifth NMOS transistor source; and

a sixth NMOS transistor comprising a sixth NMOS transistor gate and a sixth NMOS transistor drain, and a sixth NMOS transistor source to which the ground voltage is connected, wherein the fifth NMOS transistor source is connected to the sixth NMOS transistor gate and the sixth NMOS transistor drain, and

wherein the second node is between the fifth NMOS transistor and the sixth NMOS transistor.

13. A terminal device comprising:

a communicator configured to receive a first signal via a wireless communication network and transmit a second signal corresponding to the first signal via the wireless communication network; and

a reference voltage circuit configured to be driven by a power voltage, generate a reference voltage and apply the reference voltage to the communicator,

wherein the reference voltage circuit comprises:

a first current bias circuit comprising a first node;

a second current bias circuit comprising a plurality of NMOS transistors and a second node, wherein the plurality of NMOS transistors comprises a first NMOS transistor and a second NMOS transistor, the first NMOS transistor is connected to the first node, and at least two of the plurality of NMOS transistors are connected to the second node and configured to perform a sub-threshold operation according to a first voltage of the first node to generate a

second voltage at the second node; and

an amplifier configured to output the reference voltage having a same value as the second voltage.

14. The terminal device of claim 13, further comprising a power supply configured to supply the power voltage.

15. The terminal device of claim 13 or claim 14, wherein the terminal device is configured to be physically implanted in a structure or a living subject.

16. The terminal device of any one of claims 13 to 15, wherein the first current bias circuit is configured to generate the first voltage based on a first current having a complementary to absolute temperature (CTAT) characteristic, and

wherein the second current bias circuit is configured to generate the second voltage based on a second current having a proportional to absolute temperature (PTAT) characteristic.

17. The terminal device of any one of claims 13 to 16, wherein the amplifier is further configured to generate an output current having a same value as a current flowing in the first current bias circuit.

18. An operating method of a terminal device, the operating method comprising:

receiving a first signal with respect to the terminal device;

performing a sub-threshold operation of at least two NMOS transistors connected between a power voltage and a ground voltage to generate a reference voltage;

generating a second signal corresponding to the first signal based on the reference voltage; and

transmitting the second signal.

19. The operating method of claim 18, wherein the generating of the reference voltage comprises:

generating a first voltage based on a first current having a complementary to absolute temperature (CTAT) characteristic;

generating a second voltage according to the sub-threshold operation of the at least two NMOS transistors based on a second current having a proportional to absolute temperature (PTAT) characteristic; and

generating the reference voltage based on the first voltage and the second voltage.

20. The operating method of claim 18 or claim 19, further comprising receiving the power voltage from a power supply.