

Power amplifier stage of the voltage follower type.

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The invention relates to a power amplifier stage of the voltage follower type which receives an input voltage signal and supplies an output signal, which stage comprises at the output a first MOS power transistor whose source is coupled to a common mode line in series with a second MOS power transistor whose drain is coupled to a positive supply line, which two transistors are of the same conductivity type and whose common junction point supplies said output signal of the stage, which stage further comprises a first amplifier supplying a first control signal applied to the gate of the first MOS power transistor, and a second amplifier supplying a second control signal applied to the gate of the second MOS power transistor, which first and second amplifier each receive the input signal at a respective first input, with which signal the output signal of the stage, applied to a respective second input, is compared.

A power amplifier stage with a voltage gain equal to 1 is known from the document EP-A-0 492 374, whose envisaged application is the reproduction of acoustic signals.

MOS power transistors are also quite suitable for forming the output of the power amplifier stage in an application specifically designed for motor control, because of their robustness in the presence of an inductive charge. However, this type of transistor has a high gate capacitance, currently of the order of about a hundred pF, so that the control of these transistors renders it necessary to use an amplifier capable of charging and discharging this gate capacitance in a time span compatible with the desired specifications.

It is equally desirable for this same application that the conductive state of the MOS output transistors should be controlled in a very emphatic manner, *i.e.* the resistance to current passage should be as low as possible, for example R_{on} below 1 Ohm.

Under these circumstances, a rigorous time management of the conductive and blocked states of these two power transistors must be ensured so as to avoid a risk of destruction of these transistors, which would be the case if the two power transistors were conductive simultaneously even for a short moment.

Finally, a power amplifier stage of the voltage follower type should also

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comply with a current consumption requirement, which must be as low as possible when the stage is idle, *i.e.* when the input voltage is equal to the output voltage of the stage. By contrast, major currents must be possible at the output for transitory states during which the amplifier is out of balance, in response to input/output imbalance voltages as small as 100 or
5 200 mV, and with a response time which should comply with the requirements of the application.

The known amplifier stage complies only partly with these requirements since it has been specially designed for avoiding crossover distortion and not for minimizing the idle current consumption. In the known amplifier stage, in fact, the capability of reacting
10 rapidly at the output in response to a variation in the input voltage is directly connected to the value of the idle current. This idle current, accordingly, cannot be chosen to be as low as desired.

It is thus one of the aims of the invention to provide a perfected power amplifier stage which to a large extent eliminates the drawbacks of the known circuit with a
15 view to its application to a motor supply.

According to the present invention, an amplifier stage of the type described in the opening paragraph is for this purpose characterized in that, in order to exclude a simultaneous conduction of the two MOS power transistors, each of the amplifiers is provided with an inhibiting input and is arranged so as to supply a gate control signal
20 equal to the common mode voltage when said inhibiting input is brought to this same common mode voltage, and in that the stage comprises two switching transistors of the MOS field effect type each having its source coupled to the common mode line, a first switching transistor having its gate coupled to the gate of the first MOS power transistor and its drain connected to the inhibiting input of the second amplifier, and a second switching transistor
25 whose gate receives a signal derived from the gate voltage of the second MOS power transistor and whose drain is connected to the inhibiting input of the first amplifier.

Thus, when one or the other of the two MOS power transistors is in a highly conducting state, the other transistor will be blocked by the effect of one of the switching transistors. The possibility of the power transistors being destroyed through
30 simultaneous conduction, even during a short, transitory period, is thus avoided. The amplifier stage according to the invention is capable of ensuring at its output a very precise following of the voltage of the input signal when this voltage does not vary or varies slightly.



When on the other hand the input signal varies rapidly, involving a switching of the state of the MOS power transistors, this switching, controlled by the switching transistors, is realised while ensuring a delay in entering of the conductive state of one of the MOS power transistors equal to the switching-off time of the other transistor.

5 This delay may be fixed in practice to a value which is sufficiently low for not becoming disadvantageous in the case of a motor supply, for example a delay of the order of 1 μ s.

Preferably, the first and the second amplifier each supply gate control signals by means of a pair of complementary bipolar transistors whose collectors are
10 interconnected.

This configuration of transistors is highly satisfactory for efficiently ensuring the charging and discharging of the gates of the MOS power transistors.

It will be readily observed that the first MOS power transistor connected to the common mode line has a gate which has a moderate voltage variation, between a zero
15 voltage (earth) up to a gate-source voltage which ensures the conduction of the transistor. As for the second MOS power transistor, however, its gate may be brought to a voltage which varies between wide limits because it has been mounted in follower arrangement. Since the source of the second switching transistor is connected to the common mode line, its gate may be directly connected to the gate of the second MOS power transistor, which imposes
20 particular requirements on the voltage sustaining capability of said second switching transistor.

Nevertheless, an advantageous embodiment of the invention is characterized in that, of the pair of complementary bipolar output transistors of the second amplifier, that transistor whose emitter is fed with a positive voltage has its collector
25 connected to the collector of the other transistor of the pair *via* a cascode stage, and in that the connection point between the collector of this other transistor and the cascode stage forms the inhibiting input of the second amplifier.

This cascode stage is preferably realised with an MOS transistor. Said inhibiting input of the second amplifier renders it well possible to earth the gate of the
30 second MOS power transistor practically in the same manner as if the inhibiting input were connected to the gate itself of this transistor. The advantage of the interposed cascode stage is that the inhibiting input has a less voltage excursion lower than that of the gate of the second MOS power transistor, which implies that in an advantageous embodiment this



inhibiting input also forms an output for the signal to be applied to the gate of the second switching transistor. The gate of this second switching transistor thus receives a signal which is derived from the gate voltage of the second MOS power transistor by clipping, which renders it possible to use a second switching transistor of a standard type on whose gate the
5 voltage variation remains limited.

To ensure a switching of the amplifiers by a voltage rather than a current control, the inhibiting input of the first amplifier, is provided close to the input of this amplifier where the current to be derived is low. Thus, according to a preferred embodiment, the power amplifier stage in which the first amplifier comprises at the input a differential
10 pair of bipolar transistors whose connection point of the united emitters is fed with a constant current from the positive supply line and whose bases are coupled to the respective inputs of said first amplifier, is characterized according to the invention in that the collector of one of the transistors of said differential input pair forms an inhibiting input for this first amplifier. The collector in question is coupled to the common mode line (earth) *via* a load which may
15 be an input diode of a current mirror. The collector in question on the one hand passes a low current, at most equal to the constant current which supplies this differential pair, and on the other hand has a low voltage variation so that this electrode forms a particularly advantageous inhibiting input for the first amplifier.

Preferably, the power amplifier stage according to the invention comprises
20 in addition a generator of the voltage-doubling type for providing an additional positive supply voltage higher than the supply voltage mentioned earlier, which additional voltage is used for supplying the second amplifier.

The power amplifier stage is thus capable of providing an output voltage whose variation can range practically from the common mode voltage to the normal positive
25 supply voltage. The surplus voltage provided by the additional positive supply then renders possible a suitable polarization of the gate of the second MOS power transistor.

It is important in this case to limit the current level delivered by the additional positive supply. The power amplifier stage according to the invention advantageously comprises in its second amplifier limitation means for the current consumed
30 from the additional positive supply, which means are arranged so as to limit said consumed current to a multiple of the current value supplied by a reference current source, which multiple is established from the ratio of the emitter surfaces of a current mirror, while the current limitation means are completed by two further current mirrors.



The amplifier stage according to the invention is preferably used in association with another identical stage, which assembly is connected so as to form a bridge-type motor supply unit.

The following description given with reference to the annexed drawings, by way of example without being limited thereto, will render it clear in what the invention consists and how it may be realised.

Fig. 1 is a general diagram of an amplifier stage according to the invention,

Fig. 2 shows the electrical circuit of a portion of the stage of Fig. 1 in an embodiment of the invention, and

Fig. 3 shows current curves relating to the circuit portion shown in Fig. 2,

Fig. 4 is the circuit diagram of another portion of the stage of Fig. 1, in a first embodiment, and

Fig. 5 is the circuit diagram of this same portion, but in another embodiment which includes current limitation means for the positive supply line, and

Figs. 6 and 7 give current curves relating to the circuit of Fig. 5.

Fig. 1 shows a power amplifier stage in highly diagrammatic form, which stage is of the voltage follower type and receives an input signal V_i , while delivering an output signal V_o , in particular for the supply of a motor M . This stage comprises a first amplifier A_1 which supplies a first control signal V_1 to the gate of a first MOS power transistor M_1 . The amplifier stage also comprises a second amplifier A_2 which supplies a control signal V_2 to the gate of a second MOS power transistor M_2 . The transistors M_1 and M_2 are arranged in series between a common mode line 1 (earth) having a voltage V_e , and a positive supply line 2 having a voltage V_c . The two transistors M_1 and M_2 are of the same, N-channel type, while the source of transistor M_1 is coupled to the common mode line 1, its drain coupled to the source of transistor M_2 , which connection forms the output of the amplifier stage supplying the output signal V_o at terminal 11, and the drain of transistor M_2 is coupled to the positive supply line 2. The input signal V_i is applied to an input terminal 13 coupled to a first input 15 of the first amplifier A_1 as well as to a first input 17 of the second amplifier A_2 . These two amplifiers receive at a second input, at the input 18 of the first amplifier as well as at the input 19 of the second amplifier, respectively, the output signal V_o with which the input signal V_i is compared.



According to the invention, a simultaneous conduction of the two MOS power transistors M1 and M2 is avoided by means of two switching transistors, SW1 and SW2, which are of the MOS field effect type and whose sources are each connected to the common mode line 1.

5 The first switching transistor SW1 has its gate connected to the gate of transistor M1 and its drain connected to an inhibiting input 20 of the second amplifier A2. The amplifier A2 is so arranged that, when its inhibiting input 20 is brought to the voltage V_e (earth), this amplifier A2 supplies a gate control signal V2 which is equal to the voltage V_e , or very close thereto, *i.e.* it drives the transistor M2 into a non-conducting state.

10 A similar mechanism is achieved by means of the second switching transistor SW2 whose gate is coupled to the gate of the transistor M2, or to a voltage which is derived from the voltage of this gate, as it will be seen further below, and whose drain is coupled to an inhibiting input 22 of the amplifier A1.

Similarly, when the inhibiting input 22 is brought to the voltage V_e (earth), the amplifier A1 supplies a control signal V1 which is again substantially equal to the voltage V_e so that the transistor M1 is rendered non-conducting.

Owing to this arrangement, only one of the two MOS power transistors, M1 or M2, can be conducting at any given moment, with its gate control voltage being different from 0 while inhibiting the control voltage at the output of the other amplifier. All risks of short-circuits between the positive supply line 2 and the common mode line 1 are thus avoided, which short-circuits would cause irreparable damage to the power amplifier stage, especially the destruction of either of the output transistors of this stage.

Fig. 2 shows the circuit diagram of an embodiment of one of the amplifiers, such as the amplifier A1 of Fig. 1. The first MOS power transistor M1 and the output terminal 11 of the amplifier stage carrying the output voltage V_o are also shown in this Figure.

25 The input 15 of the amplifier carries the voltage V_i . This input voltage is compared with the output voltage V_o by means of a differential pair of PNP transistors T1, T2 whose united emitters are supplied by a current source S1 which delivers a current I1 from a positive supply voltage V_c . The transistor T2 is connected as a diode, while the transistor T1 has its collector coupled to the common mode line 1 via the input branch of a current mirror T3, T4 with NPN transistors. The input transistor T3 of this current mirror is connected as a diode, while the output transistor T4 provides a current which is identical to



that provided by the transistor T1, which current is drawn from a PNP transistor T5 which is connected as a diode. The transistor T5 has its base coupled to the base of two other PNP transistors T6 and T7. The transistor T5 has its emitter coupled to the positive supply line 2 via an emitter resistance R1, whereas the transistors T6 and T7 have emitters directly
5 connected to the supply line 2.

The assembly of the transistors T5, T6, T7 forms a current amplifier, the currents delivered by the transistors T6 and T7 being equal since these two transistors are mounted as a current mirror. The collector of the transistor T7 is connected to the collector of a NPN transistor T8 whose emitter is connected to the common mode line 1. This
10 transistor pair T7, T8 forms the output of the amplifier, supplying a control voltage V1 to the gate of the MOS power transistor M1. The base of the transistor T8 is connected on the one hand to a current source S2 which supplies a current I2. On the other hand, it is connected to the collector of an NPN transistor T9 which forms part of an assembly formed by two NPN transistors T10, T11 arranged as diodes and coupled to the collector of the PNP
15 transistor T6, which assembly in addition comprises a resistor R2 connecting the base of the transistor T9 to the common mode line 1, which base is also connected to the emitter of the transistor T11.

This assembly, and especially the value of the resistor R2, are provided in order that the currents supplied by the transistors T7 and T8 are equal when the voltage
20 difference ($V_i - V_o$) is close to zero, which represents the equilibrium state of the amplifier.

If the voltage of the input signal V_i is momentarily higher than the output voltage V_o , the current supplied by transistor T1 is lower than its nominal current (in the equilibrium state), and the same holds for the current absorbed by the transistor T4 at the output of the current mirror T3, T4. Under these conditions, the current supplied by the
25 transistors T6 and T7 is lower than the nominal idle value. The transistor T9 is practically blocked, as is the transistor T10. The entire current I2 from the current source S2 thus supplies the base of the transistor T8, which supplies its maximum current.

If, on the other hand, the voltage of the input signal V_i is lower temporarily than the output voltage V_o , the input transistor T1 of the pair T1, T2 supplies a
30 current higher than its nominal current, which is amplified by the assembly formed by the resistor R1, transistors T5, T6, T7, whereupon the transistors T6 and T7 both supply a current which is substantially amplified owing to the voltage drop in the emitter resistance R1. The substantial current supplied by the transistor T6 causes via the transistor T11



arranged as a diode a voltage drop in the resistor R2 which is high enough compared with the emitter/base voltage of the transistor T9, so that this transistor conducts and absorbs the major portion of the current I2 provided by the current source S2. Thus the transistor T8 substantially does not carry a current when the output transistor T7 is conducting.

5 The advantage of a circuit as described with reference to Fig. 2, realised mainly with bipolar transistors, is that the amplifier is capable of providing at the output a control signal V1 for the gate of the MOS power transistor M1 in the form of a charging or discharging current for the gate capacitance of this transistor, which may have a comparatively high value (a few milliamps) in the case of a transitory imbalance of the
10 amplifier. When this amplifier returns to its equilibrium state, the output voltage Vo very closely approximating the input voltage Vi then, the equal currents supplied by the transistor T7 and absorbed by the transistor T8 at the output of the amplifier are very low and may be reduced to a value below, for example, 50 μ A.

 As for this amplifier A1, it will be noted that the control voltage V1
15 applied to the gate of transistor M1 necessitates a comparatively small variation between a zero voltage and a gate-source voltage which is sufficient for rendering the transistor M1 strongly conducting. Under these circumstances, it is particularly simple to use the control voltage V1 present at the gate of transistor M1 also as a gate voltage for the switching transistor SW1 (not shown in Fig. 2), whose simultaneous conduction accompanying the
20 conduction of transistor M1 will cause the blocking of the second amplifier A2, as shown in Fig. 1.

 An inhibiting input of the amplifier A1 must be provided such that the amplifier A1 drives the power transistor M1 into non-conduction when this input is connected to earth. Advantageously, such an inhibiting input visible with reference numeral
25 22 in the Figure is connected to the connection point between the collector of transistor T1 and the collector of transistor T3 of the mirror T3, T4. When this input 22 is earthed, the current supplied by the transistor T1 is derived outside the current mirror T3, T4 so that the transistor T4 no longer passes current, and neither do the transistors T5, T6 and T7. As was seen above, the transistor T9 passes substantially no current, so that all of the current I2
30 from the current source S2 is introduced as a base current for transistor T8. This current supplies a gate discharging current for the power transistor M1, as long as this gate is charged, while the transistor T8 enters the saturated state when the gate of transistor M1 has been completely discharged.

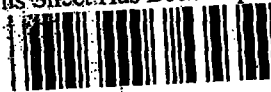


Fig. 3 shows the transient shapes of the currents: $I(T4)$, passed by the transistor T4, $I(T7)$ passed by the transistor T7, and $I(T8)$ passed by the transistor T8, as a function of the voltage imbalance between the input voltage V_i and the output voltage V_o . The logarithmic scale used for the currents in the Figure shows that the action on the gate of the MOS power transistor M1 is very strong in the case of an imbalance of the input voltage, whereas in the idle state the amplifier supplies no more than approximately $40 \mu A$ at the output by way of the transistors T7 and T8, in a practical example.

Fig. 4 is a circuit diagram of an embodiment of the amplifier A2 in Fig.

1. In this Fig. 4, the second MOS power transistor M2 is again shown, to which the amplifier stage shown supplies the gate control signal V_2 . The amplifier A2 controlling the transistor M2 is constructed mainly on the same principle as the amplifier A1 shown in Fig. 2.

Elements having the same function have been given the same reference numerals as those in the preceding Figures. In Fig. 4, the NPN transistor T18 performs substantially the same function as transistor T8 in Fig. 2 whose base is supplied by a current source S2 supplying a current I_2 . In the present embodiment, the collector of transistor T18 is coupled to the collector of a PNP transistor T17 via a cascode stage realised by means of an MOS transistor M18 whose gate is polarized with a reference voltage V_{ref} . The control voltage V_2 for the gate of transistor M2 is thus derived from the interconnection point of the collector of transistor T17 and the drain of transistor M18. Since the output voltage V_o of the amplifier stage is connected to the source of the power transistor M2, this output voltage V_o can reach the level of the positive supply voltage V_{c1} , provided its gate control voltage V_2 can rise beyond this positive voltage V_{c1} . This is why the amplifier A2 is shown as being positively supplied with a voltage V_{c2} , higher than V_{c1} , which is produced by a voltage-doubling circuit 16 of a classical type, starting from the voltage V_{c1} .

In an embodiment, the voltage V_{c1} is equal to 12 V while the voltage V_{c2} is of the order of 18 V. The assembly formed by transistors T9, T10, T11 and resistor R2, designed to control the base current of transistor T18, performs the same function as the assembly described above with reference to Fig. 2 in relation to the control of the base current of transistor T8. The signal V_i applied to the input terminal 17 of amplifier A2 is compared with the output signal V_o by means of two pairs of transistors. The signals V_i and V_o are brought respectively to the emitters of a first pair of NPN transistors T12, T13, while the joint bases of these transistors T12, T13 are supplied by a current source S11 delivering



a current I_{11} . In addition, the transistor T12 is connected as a diode through a connection between base and collector.

A second pair of transistors T14, T16 of the PNP type constitutes a comparator assembly symmetrical with the preceding two transistors, wherein the transistor T16 is connected as a diode and supplied by a current source S3 delivering a current I_3 towards the common mode line 1. Finally, the comparator formed by the transistors T12, T13, T14, T16 forms an amplifier for the current passed by the transistors T13, T14 when the input voltage V_i is higher than the output voltage V_o , the currents passed by the transistors T13 and T14 in the means time remaining identical to one another.

When the input voltage V_i is lower than the output voltage V_o , the transistors T13 and T14 are driven into a state close to the blocked state in which these transistors supply a current which is very much lower than the idle current of the stage in the equilibrium state as obtained when V_o is equal to V_i . The transistor T14 plays the same part as the transistor T6 in the diagram of Fig. 2. When the current of T14 rises above the nominal idle current, the transistor T18 is driven into non-conduction through absorption of the current from current source S2 by the transistor T9. In the same manner, the transistor T13 passes a current which is amplified by the assembly of a transistor T15 mounted as a diode and having an emitter resistance R11 coupled in parallel with the transistor T17, which in conjunction with the transistor T18 forms the pair of output transistors. When the current passed by the transistor T13 rises, obviously, the current passed by the transistor T17 rises even more quickly. The transient current supplied by the transistors T17 and T18 can be comparatively strong, as in the preceding assembly, *i.e.* of the order of a few milliamps, whereas the idle current of these two transistors is controlled, for example, at $40 \mu A$ when the amplifier is in equilibrium (input voltage equal to output voltage).

As is shown in Fig. 4, a resistance R5 is arranged in parallel between the emitters of the transistors T14 and T16. This resistance R5 is optional, it has a high value of, for example, 50 KOhms, and is intended for avoiding that the connection between the emitter of transistor T13 and the emitter of transistor T14 becomes floating in the case of a strong imbalance of the amplifier.

The amplification characteristics of the amplifier A2 are substantially identical to those of the amplifier A1 described with reference to Fig. 2.

The control voltage V_2 for the gate of the MOS power transistor M2 varies between wide limits, here from a zero voltage up to practically the voltage V_{cc} ,



allowing for the saturation voltage of transistor T17. The gate connection of the power transistor M2 may thus form an output for controlling the second switching transistor SW2 (not shown in Fig. 4) as well as an input terminal for the inhibiting command of this amplifier A2 since the transistor M2 will be blocked by its gate being connected to earth. In the assembly shown in Fig. 4, however, the connection between the source of transistor M18 and the collector of transistor T18 forms a preferred output, indicated as a terminal 21, for the control of the second switching transistor SW2. In fact, the voltage obtained at terminal 21 is derived from the gate voltage of transistor M2, realised apart from clipping by the cascode transistor M18. It fixes a maximum voltage for the output voltage of terminal 21 equal to the reference voltage V_{ref} minus the threshold voltage of this transistor. Since the voltage at terminal 21 shows a smaller variation than the gate voltage of transistor M2, this terminal 21 thus forms an advantageous control for the second switching transistor SW2 which may now be of a normal type which does not necessitate a voltage sustaining capability as high as the voltage which may be present at the gate of transistor M2.

The collector of transistor T18 may also form an input terminal 20 for the inhibiting command of amplifier A2. In fact, when terminal 20 is connected to earth, the cascode transistor M18 is necessarily conducting so that the current supplied by the transistor T17 is by-passed towards earth. The transistor M2 is blocked thereby.

When the amplifier A2 is supplied with a positive supply voltage V_{c2} higher than the normal supply voltage V_{c1} of the circuit, as is shown in Fig. 4, it is advantageous to fix a limit for the current passed by the transistor T17 as well as for the currents supplied by the transistors T13 and T15.

For this purpose, Fig. 5 shows a second embodiment of the amplifier A2 which comprises a modification which renders such a current limitation possible. According to this embodiment, the portion relating to the control of transistor T18 remains identical to that shown in Fig. 4, while the circuit modification concerns the control portion for transistor T17. The means rendering possible a limitation of the current in transistors T17 and T15 are substantially formed by a first pair of PNP transistors T20, T21 which are mounted as a current mirror, a second pair of PNP transistors T24, T25 which are mounted as a current mirror, and a third pair of NPN transistors T22, T23 which are mounted as a current mirror, with a divider ratio from n to 1 between its input and its output.

To supply the pair of transistors T12, T13 with current, a reference current source S5, set for the common mode voltage V_e , supplies a reference current I_5 in



the current mirror T20, T21. The collector current of transistor T13 is variable and depends on the degree of imbalance between the input voltage V_i and the output voltage V_o . This current is written I_y in the Figure. A known fraction, written I_z , of this current I_y , which follows from the surface area ratio between the transistors T22, T23, is absorbed at the input of the current mirror T24, T25. The same current I_z is finally supplied to the current source S5. The current written I_x supplied by the current mirror T20, T21, finally, is equal to the difference between the current I_5 and the current I_z . The other part of current I_y passed by the transistor T13, which part is equal to $n \cdot I_z$ owing to the dimensional ratio in the current mirror T22, T23, is applied to the input of the amplifier assembly T15, T17, which amplifier assembly has already been discussed with reference to Fig. 4.

The current $n \cdot I_z$ taken up at the input of the assembly T15, T17 may be readily evaluated:

$$I_z = I_y / (n+1) \text{ and } n \cdot I_z = n \cdot I_y / (n+1) \quad (1)$$

owing to the division of the current I_y in the current mirror T22, T23.

However, I_z is subtracted from I_5 at the input of current mirror T20, T21, so that:

$$I_x = I_5 - I_z \quad (2)$$

When the amplifier is in total unbalance, the entire current I_x is introduced into the base of transistor T13, so that then:

$$I_y = \beta I_x \quad (3)$$

with β = the current gain of an NPN transistor.

By combining the equations (1) and (3), it follows that a limit value of I_z is:

$$I_z = \beta \cdot I_x / (n+1) = (\beta I_5 - \beta I_z) / (n+1)$$

$$I_z = I_5 \cdot \frac{\beta}{\beta + n + 1}$$

and the current $n I_z$ absorbed by T23 in T15 is at most:

$$n I_z = I_5 \cdot \frac{n \beta}{\beta + n + 1}$$

When the gain β is great compared with n , the current $n \cdot I_z$ tends towards:

$$n I_z \approx n \cdot I_5$$

Given a ratio $n = 10$, for example, a gain β of 100 and a reference current I_5 of $10 \mu A$, it follows that the limitation current $n I_z$ taken up by the transistor T23



is of the order of 90 to 100 μA .

Taking into account the value chosen for the emitter resistance R11, it is possible to know exactly the maximum current which can be passed by the transistor T17 in case of a very strong imbalance of the amplifier A2.

5 When the gate of transistor M2 is fully charged by the transistor T17, it will enter the saturated state and the collector can no longer supply current. The current consumed with the amplifier held in imbalance would then be reduced to the current supplied by the transistor T23, *i.e.* a current approximately 20 times smaller than the maximum charging current of transistor T17 when it is not saturated that is, in a transition state.

10 It is apparent that the current limiter circuit as described with reference to Fig. 5 is particularly effective. It allows to fix a limit for the currents consumed at the additional positive supply voltage V_{c2} , which limit is then independent of the gain of the transistors and of the variation in gain with temperature, which was not the case with the circuit shown in Fig. 4.

15 Fig. 6 shows the graphs of the currents I_x , passed by transistor T12, $n.I_z$ passed by transistor T23, $I(T17)$ passed by transistor T17, and $I(T18)$ passed by transistor T18, as a function of a transient imbalance in voltage ($V_i - V_o$). A logarithmic current scale is used. The curves in Fig. 6 show the high current amplification rate when the amplifier is in a transitory state of imbalance.

20 Fig. 7 shows with curve I_A the total current drawn from the additional positive supply V_{c2} as a function of the voltage difference ($V_i - V_o$) in permanent operation, and especially when the transistor T17 is saturated. For comparison, broken-line curve I_B is identical to curve $I(T17)$ in Fig. 6. It is clearly visible that the current limiter described with reference to Fig. 5 is particularly effective in the case of a static imbalance of the amplifier,
25 although it also renders possible a strong charging current in transient operation.

It is possible to apply minor modifications compared with the examples described above in the realisation of the power amplifier stage without departing from the scope of the invention as claimed hereinafter.

Claims:

1. A power amplifier stage of the voltage follower type which receives an input voltage signal (V_i) and supplies an output signal (V_o), which stage comprises at the output a first MOS power transistor (M1) whose source is coupled to a common mode line (1) in series with a second MOS power transistor (M2) whose drain is coupled to a positive supply line (2), which two transistors are of the same conductivity type and whose common junction point supplies said output signal of the stage, which stage further comprises a first amplifier (A1) supplying a first control signal (V_1) applied to the gate of the first MOS power transistor, and a second amplifier (A2) supplying a second control signal (V_2) applied to the gate of the second MOS power transistor, which first and second amplifier each receive the input signal (V_i) at a respective first input, with which signal (V_o) the output signal of the stage, applied to a respective second input, is compared, characterized in that, in order to exclude a simultaneous conduction of the two MOS power transistors (M1, M2), each of the amplifiers (A1, A2) is provided with an inhibiting input (22, 20) and is arranged so as to supply a gate control signal equal to the common mode voltage (V_e) when said inhibiting input is brought to this same common mode voltage, and in that the stage comprises two switching transistors of the MOS field effect type each having its source coupled to the common mode line (1), a first switching transistor (SW1) having its gate coupled to the gate of the first MOS power transistor (M1) and its drain connected to the inhibiting input of the second amplifier (A2), and a second switching transistor (SW2) whose gate receives a signal derived from the gate voltage of the second MOS power transistor (M2) and whose drain is connected to the inhibiting input of the first amplifier (A1).
2. A power amplifier stage as claimed in Claim 1, characterized in that the first and the second amplifier each supply gate control signals by means of a pair of complementary bipolar transistors (T7, T8; T17, T18) whose collectors are interconnected.
3. A power amplifier stage as claimed in Claim 2, characterized in that, of the pair of complementary bipolar output transistors of the second amplifier (A2), that transistor (T17) whose emitter is fed with a positive voltage has its collector connected to the



collector of the other transistor (T18) of the pair *via* a cascode stage (M18), and in that the connection point between the collector of this other transistor and the cascode stage forms the inhibiting input (20) of the second amplifier.

4. A power amplifier stage as claimed in Claim 3, characterized in that the
5 inhibiting input (20) of the second amplifier (A2) also forms an output for the signal applied to the gate of the second switching transistor (SW2).

5. A power amplifier stage as claimed in any one of the Claims 1 to 4, characterized in that the gate connection of the second MOS power transistor (M2) forms the inhibiting input of the second amplifier (A2).

10 6. A power amplifier stage as claimed in any one of the Claims 1 to 5, in which the first amplifier (A1) comprises at the input a differential pair of bipolar transistors (T1, T2) whose connection point of the united emitters is fed with a constant current (I1) from the positive supply line and whose bases are coupled to the respective inputs of said first amplifier, characterized in that the collector of one of the transistors (T1) of said
15 differential pair at the input forms the inhibiting input (22) for this first amplifier.

7. A power amplifier stage as claimed in any one of the Claims 2 to 6, characterized in that it comprises a generator (16) of the voltage-doubling type for providing an additional positive supply voltage (Vc2) higher than the supply voltage mentioned earlier, which additional voltage is used for supplying the second amplifier (A2).

20 8. A power amplifier stage as claimed in Claim 7, characterized in that the second amplifier (A2) comprises limitation means for the current consumed from the additional positive supply (Vc2), which means limit said consumed current to a multiple of the current value supplied by a reference current source (S5), which multiple is established from the ratio of the emitter surfaces of a current mirror (T22-T23), while said current
25 limitation means are completed by two further current mirrors (T20-T21, T24-T25).