INTEGRATION OF BIPOLAR AND CMOS DEVICES FOR SUB-0.1 MICROMETER TRANSISTORS

ABSTRACT OF THE DISCLOSURE

Form a semiconductor device with dielectric, isolation structures in a top surface of a silicon semiconductor substrate, separating the substrate into emitter, NMOS and PMOS areas. Form a gate oxide layer above the isolation structures on the top surface of the silicon semiconductor substrate. Form a conductive polysilicon layer above the thin silicon oxide layer. Mask the NMOS and PMOS regions of the substrate with an emitter mask having a window over the emitter area of the substrate. Ion implant emitter dopant into a portion of the conductive polysilicon layer over the emitter area of the substrate through the window in the emitter mask. Strip the emitter mask. Anneal the substrate including the thin silicon oxide layer, and the polysilicon layer to drive the dopant into an emitter region in the emitter area in the substrate. Form doped source/drain regions and a base in the emitter area of the substrate.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)