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IMPROVEMENTS RELATING TO FREQUENCY SYNTHESISERS

FIELD OF THE INVENTION

5 This invention relates to sigma-delta modulators and particularly but not solely to radio frequency synthesisers which use these modulators in fractional division. More particularly the invention relates to modulator systems which are able to provide an extended range of fractional division ratios and reduced emission of spurious frequencies.

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BACKGROUND TO THE INVENTION

Radio communication devices employ frequency synthesisers in various ways to control transmission and reception of signals. A synthesiser generally includes a reference oscillator which generates a stable reference frequency signal and is used to determine the output of a frequency controlled oscillator which in turn generates a variable RF output signal. This output signal is generally coupled to an antenna of the communication device by way of one or more mixers which modulate or demodulate the signal for transmission or reception respectively. The synthesiser is programmed by a control unit such as a digital processor to produce the controlled oscillator signal at a range of frequencies as required by the device. Frequency synthesisers are also often used in power amplification systems for radio transmitters.

25 Indirect frequency synthesisers use one or more phase lock loops (PLLs) to generate the variable output signal from the frequency controlled oscillator. The phase lock loop contains a phase discriminator which generates an output according to the phase difference between the reference signal and a feedback signal. The feedback signal is generally produced by dividing the frequency of the output from the controlled oscillator. Output from the phase discriminator is applied to a loop filter which provides a control signal for the controlled oscillator. Voltage rather than current controlled oscillators are normally used. In general terms, a feedback loop of this kind attempts to match the frequency of the controlled oscillator to a multiple of the reference frequency and stabilise with a predetermined phase difference between the reference and feedback signals.

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Frequency division of the output from the frequency controlled oscillator can be implemented in various ways to enable a relatively low frequency reference to determine a wide range of variable RF output frequencies. Integer division techniques are acceptable in many circumstances. However, fractional techniques are becoming common and allow the synthesiser to achieve almost arbitrarily fine frequency resolution. These techniques modulate the instantaneous integer divide ratio of the feedback to the phase discriminator to produce average non-integer division ratios. The non-integer values have an integer part IP with value N, and a fractional part FP with a value typically in the range $\{0,1\}$. Cyclic variation of the division value generally produces spurious frequencies and additional phase noise in the synthesised output signal. Various cancellation schemes such as phase interpolation have been employed to reduce the fractional spurs and noise but generally require an increase in complexity and cost of the synthesiser to achieve significant reduction in the amplitude of the spurs.

Fractional-N synthesisers which use sigma-delta modulation to reduce phase noise and spurs resulting from non-integer division values are well known, as described in US 4,609,881 for example. This modulation technique arose as a development in analog-to-digital conversion and has since been widely used in electronic communication devices for a range of purposes. It involves feedback to improve the effective resolution of a coarse quantiser and allows shaping of the noise which arises from quantisation. In general terms, input is fed to the quantiser via an integrator with the quantised output being fed back and subtracted from the input. The output of the modulator therefore contains the original signal plus the first difference of the quantisation error. A first order process of this kind may be implemented wholly or partly using digital signals. A detailed discussion of sigma-delta techniques can be found in *Delta-Sigma Data Converters*, IEEE Press 1997.

Higher order sigma-delta modulators generally use two or more integrators each receiving feedback from the output to improve the overall noise performance. A cascade is also sometimes used whereby the output of two or more modulators is combined in a way which cancels the noise that they individually produce. In a cascade of two first order modulators for example, output from the integrator of the first modulator is fed to the second modulator. The output of the second is differentiated and subtracted from the output of the first to provide a net signal. This

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leaves the noise as the second difference of the quantisation error of the second modulator, in a form similar to that of a second order modulator. Multi-level quantisers have also been used to improve the stability of higher order and cascaded modulators.

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SUMMARY OF THE INVENTION

10 It is an object of the present invention to provide for improved performance of fractional-N frequency synthesisers. The improvements are particularly directed to increased flexibility in the selection of fractional division values and decreased output of spurious frequencies or noise. In general these improvements are enabled by a sigma-delta modulator having a quantiser with logic control in the output and/or feedback stages.

15 Accordingly in one aspect, the invention may broadly be said to consist in a frequency synthesiser comprising: a synthesiser loop including a programmable frequency divider, and a controller which determines average fractional division values for the divider, wherein each division value comprises selected integer and fractional parts, and the selected fractional part varies over a range other than $\{0,1\}$.

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In a second aspect the invention may also be said to consist in a frequency synthesiser comprising: a synthesiser loop including a programmable divider, a divider control means which provides a signal to the divider to cause fractional division and thereby produce a required output frequency from the loop, wherein the control means includes at least one digital modulator having an adder, a latch coupled between an output and input of the adder, and an output logic stage which carries out a logical operation on one or more bits which are output by the adder.

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30 In a third aspect the invention may further be said to consist in a frequency synthesiser comprising: a synthesiser loop including a programmable divider, a divider control means which provides a signal to the divider to cause fractional division and thereby produce a required output frequency from the loop, wherein the control means includes at least one digital modulator having an adder, a latch coupled between an output and input of the adder, and a feedback logic stage which carries out a logical operation on one or more bits which are output by the adder.

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In a fourth aspect the invention may be said to consist in a digital modulator comprising: an adder which receives a control signal and an error signal as inputs and produces a multi-bit output by addition of the inputs, an output logic stage which receives an input derived from at least one bit of the output of the adder and carries out a logical operation on that input to produce a modulator output signal, and a feedback path including a latch which combines at least two groups of bits from the output of the adder to produce the error signal.

In a further aspect the invention may be said to consist in a modulator arrangement comprising: two or more modulators each having an adder, a latch coupled between an output and an input of the adder, and an output logic stage, wherein the modulators are connected so that output of the latch in each modulator is coupled to an input of the adder in a subsequent modulator, if any, and the output of the logic stage in each modulator is coupled to a common combination stage to produce an output for the arrangement.

BRIEF DESCRIPTION OF DRAWINGS

Preferred embodiments of the invention will be described with respect to the accompanying drawings, of which:

Figure 1 schematically shows a frequency synthesiser having a frequency divider which is programmable with integer division values,

Figure 2 shows a frequency synthesiser in which the divider is modulated for fractional division,

Figures 3a, 3b respectively show a conventional accumulator performing as a sigma-delta modulator and a corresponding quantiser transfer function,

Figures 4a, 4b respectively show the Z-transform model of an ideal sigma-delta modulator and a transfer function corresponding to an ideal two-level quantiser,

Figure 4c shows a Z-transform model equivalent to that of Figure 4a for comparison with Figure 6,

Figure 4d is a further model indicating how dither signals may be added to a sigma-delta modulator to reduce limit cycles,

Figure 5 shows a three stage sigma-delta modulator formed by a cascade of first order modulators such as shown in Figure 3a,

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Figure 6 is an accumulator circuit with logic stages forming an improved first order sigma-delta modulator according to the invention,

Figures 7a, 7b, 7c demonstrate two, four and eight-level transfer functions which may be implemented by the quantiser in Figure 6,

5 Figure 8 is a table showing how the logic stages of the modulator in Figure 6 can be implemented to form a two-level quantiser,

Figures 9a, 9b are tables showing how the logic stages of the modulator in Figure 6 may be implemented to form a four-level quantiser,

10 Figure 10 indicates fractional division values produced by a modulator having a quantiser with a four-level transfer function such as shown in Figures 9a, 9b,

Figure 11 shows a three stage modulator formed by a cascade of first order modulators according to Figure 6 each possibly having different quantiser levels,

15 Figure 12 is a table indicating scale factors required for input and output to the individual modulators in Figure 11 when the quantisers have different output levels,

Figure 13 is a table summarising properties of modulators for a range of possible multi-level quantisers,

Figures 14a, 14b respectively show sample output from the multi-stage modulator systems of Figures 5, 11,

20 Figure 15 is an alternative modulator based on Figure 6 in which feedback from the quantiser is dithered, and

Figure 16 is a table indicating a possible implementation of the quantiser.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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Referring to these figures it will be appreciated that a frequency synthesiser according to the invention or more particularly a sigma-delta modulator can be constructed in various ways within the scope of the claims. The preferred embodiments are described by way of example only. The known components of synthesiser and modulator devices will be understood by a skilled person and a detailed explanation of their function need not be given.

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Figure 1 shows a simple frequency synthesiser using a phase lock loop (PLL) 10 as a feedback control system. The loop contains a phase discriminator 11, a filter 12, reference oscillator 13 and a voltage controlled oscillator (VCO) 14. A

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programmable frequency divider 15 is included in a feedback path 16 from the VCO to the phase discriminator. The discriminator acts to compare the frequency f_r of the signal from the reference oscillator with the frequency f_o of the signal from the VCO after division by an integer value N in the divider. If the phase of the reference
 5 signal leads that of the divided VCO signal then the output of the discriminator is effectively a frequency down signal which serves to decrease the frequency of the VCO. If the phase of the reference signal lags that of the divided VCO signal then the output of the discriminator is a frequency up signal which increases the frequency of the VCO. In normal operation the loop stabilises so that the signals
 10 input to the discriminator have zero phase difference and the output of the VCO forms the output of the synthesiser with $f_o = N f_r$. A controller 17 sets N within a range of discrete integer values.

Figure 2 shows a conventional fractional- N frequency synthesiser in which the
 15 controller 17 varies the instantaneous value of N by way of a modulator 20. This creates a range of non-integer division values which are available from a dual modulus divider 25 in the feedback loop 10. The division value is periodically altered from N to $N+1$ during a cycle determined by a controller 27. In this example the modulator simply involves a K -bit accumulator which receives a control word
 20 k from the controller on line 21. Each output pulse from the divider clocks the accumulator on line 22 and adds the input word to the accumulator contents. If the contents exceed 2^K then an overflow signal is generated on line 23 and causes a single division by $N+1$ rather than N in the divider. For a constant input word the accumulator will overflow on every $2^K/k$ clock pulses. This creates an average
 25 division value having an integer part $IP = N$ and a fractional part $FP = k/2^K < 1$ which are determined by the controller. In normal operation the loop stabilises so that the signals input to the discriminator has an average phase difference equal to zero and the output of the VCO forms the output of the synthesiser with $f_o = (N + k/2^K) f_r$.

Figure 3a shows the accumulator of Figure 2 in more detail. An adder 30 has two
 30 inputs one of which receives the control word k from the controller 27 on line 21. The second input receives the output signal c of the adder through latch 31. An overflow signal from the adder is passed to the divider on line 23 while the latch is
 35 clocked by output from the divider on line 22. The accumulator acts as a first order

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sigma-delta modulator in which the overflow signal represents quantisation Q of the output signal c of the adder. Figure 3b demonstrates a quantiser transfer function $Q(c)$ which is not symmetrical about zero.

- 5 Figure 4a gives the Z-transform model of an ideal first order sigma-delta modulator by way of comparison with the modulator of Figure 3a. The input k is fed to a two-level quantiser 40 by way of an integrator represented by sum function 41 and delay 42. Output Y of the modulator is fed back through delay 43 and subtracted from the input by sum function 44. Output of the integrator is represented as a signal u
- 10 approximately comparable with the signal c at the second input of the accumulator in Figure 3a. Figure 4b demonstrates the ideal two-level quantiser transfer function $Q(u)$ which is symmetrical about zero. Figure 4c is a model equivalent to that of Figure 4a which is mentioned later in relation to Figure 6.
- 15 Figure 4d indicates how a dither signal may be added in a modulator arrangement. Dithering is a known process in which typically a random or at least pseudo-random sequence is added to a digital data stream to reduce the likelihood that any cyclical pattern will develop. The mean value of the sequence is zero so there is no overall effect on the output. In the present case a cyclical output from the modulator will
- 20 be passed to the frequency divider and cause spurious frequencies in the output of the synthesiser. If required in a particular implementation a dither sequence d may be added either at the input to adder 44 through an extra sum function 48 or at the input to quantiser 40 by way of sum function 49. This randomises the quantisation noise signal e more effectively. The sequence d must normally be pre-filtered to
- 25 preserve noise shaping by the modulator, preferably by a transformation $(1-z^{-1})$.

Figure 5 shows a three stage modulator 50 formed by a conventional cascade of first order modulators 51, 52, 53 such as the accumulator shown in Figure 3a. A control word X produces a relatively complex signal Y which may be provided for the divider 25 in Figure 2 to determine the average division value of the feedback loop

30 10. The contents of each modulator stage forms an error signal which is provided as an input to the next stage while each output is passed through a pair of respective delay elements 54. A selection of outputs from the modulators and delay elements is passed to a combination stage 55. These outputs are selected and combined so

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that the signal Y contains a higher order correction for quantisation errors. Each modulator and each delay circuit is clocked by the output of the divider.

Fractional-N division by way of an accumulator overflow arrangement as shown in Figure 2 leads to spurious frequencies in the output of the VCO 14. These spurs are offset from the output frequency f_0 by $nf_k/2^K$ where $n = 0, 1, 2, 3, \dots$. For large values of n the spurs fall outside the bandwidth of the loop 10 and are attenuated by the filter 12. Additional circuitry is normally required to reduce those spurs which lie within the bandwidth and this increases the complexity and cost of the synthesiser. Division modulated by output from the cascade in Figure 5 is free of fractional spurs for most control words X. However, the signal Y now takes a range of integer values and the divider 25 must be capable of performing multiple modulus division in the loop. In both cases the fractional part FP of the average division value is limited to lie in the range $\{0,1\}$ for any given integer part IP.

Figure 6 shows a preferred modulator 60 according to the invention which may be used to extend the range of the fractional part FP of the average division value in a frequency synthesiser. A control word X produces an output Y which may be used to modulate the divider 25 in Figure 2. All signals in this figure are digital and are in two's complement format. An n-bit adder 61 has two inputs one of which receives the control word. The second input receives an error signal e derived from output of the adder after various feedback processes applied to groups of most and least significant bits. An output logic stage 62 receives a group t of msbs from the adder 61 and operates on the bits during a quantisation process which produces the modulator output. A feedback logic stage 63 also receives the group t from adder 61 and operates on the bits in a feedback process which determines overload and stability performance of the modulator. An m-bit adder 64 receives a group of m msbs from the adder 61 and a group of m bits from the feedback logic stage 63. A latch 65 receives a group of n-m lsbs from the adder 61 and a group of m bits from the adder 64 to form the error signal. Latch 65 receives a clock signal which moves the modulator from one state to the next through addition processes in each of the adders 61 and 64.

The output and feedback logic stages 62 and 63 in Figure 6 may be provided in various ways. A dedicated Boolean operation on the bit group t is one approach.

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Alternatively either stage might be a multiplexer from which the value of bit group t selects the output. The output values of the multiplexers may be set in hardware or held in registers for example.

5 A dither signal is readily added to the modulator in Figure 6 if required, either at the input to adder 61 with control word X , at the output from the adder 61, or as part of the feedback logic stage 63 as described below. A dither signal will generally increase the amplitude of the signal to which it is added. Given the increased fractional range of the present modulator an extra adder equivalent to sum function
10 48 in Figure 4d would be necessary to add a dither signal before the input of adder 61. An extra adder equivalent to function 49 would be required for addition at the output of adder 61.

15 Figures 7a, 7b, 7c demonstrate ideal transfer functions $Q(u)$ for two, four and eight level quantisers respectively, each of which may be implemented by the modulator 60 of Figure 6. Each function produces a multiple level output signal f according to where the input signal u lies within one of a series of decision regions defined by points d . In general the range of possible decision regions and corresponding levels in the output signal is determined by the number of bits in group t from the adder 61.
20 One, two and three bit groups provide two, four and eight levels of quantisation respectively, for example. That these implementations are possible is indicated by a comparison of modulator 60 with the model of an ideal sigma-delta modulator in Figure 4c. Adder 61 performs the sum function 44. Output stage 62 forms the quantiser 40. A digital-to-analog function implicit in the feedback of Figure 4c is
25 performed by feedback logic stage 63 in order to allow this comparison. Adder 64 performs the sum function 46. Latch 65 performs the delay function 47. The properties of the quantiser 40 are determined by an appropriate selection of parameters within the output logic stage 62.

30 Figure 8 is a table outlining a selection of parameters for the output and feedback logic stages which will implement an ideal two-level quantiser in the modulator of Figure 6. In this table $B=2^n$ where n is the length of adder 61 and group t contains a single bit. Column (i) contains possible values of t which are required to produce the two levels. Columns (ii) and (iii) give the corresponding decision regions in
35 alternative decimal and binary forms. Columns (iv) and (v) set out functionality of

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the output logic stage 62 which in this simple case acts as an inverter. A more complex mapping of a multiple bit group t to quantiser output bits is required for higher levels. Columns (vi), (vii), (viii) set out functionality of the feedback logic stage 63. Column (vi) contains bits which determine the feedback ratio and can be
 5 chosen with some freedom. Columns (vii) and (viii) give the ratios for outputs according to column (v) in binary and decimal forms.

Figures 9a, 9b are tables outlining alternative selections of parameters for the output and feedback logic stages which will implement an ideal four-level quantiser in the
 10 modulator of Figure 6. The fractional part FP of the division value in this example ranges over $\{-1.5, 1.5\}$ as shown in Figure 10. Figure 9a is an example indicating a selection for decision regions which give optimum noise performance. Figure 9b is an example indicating a selection having fewer bits for optimum hardware efficiency. In each table the left hand portion represents decision regions for input
 15 to the quantiser, the middle portion represents n -bit output by the adder 61, and the right hand portion shows feedback ratios f and output signals Y . In general for any implementation the choice of feedback ratios affects overload performance and therefore noise shaping properties of the modulator for particular values of the control word X . A high overload point allows a wide range of control values but
 20 degrades the performance requiring a balance of considerations.

Figure 10 demonstrates a range of fractional division values which may be produced in a synthesiser by a modulator such as outlined in Figures 9a, 9b when implementing a four level quantiser. In this example the value of FP ranges over $\{-$
 25 $1.5, 1.5\}$ about an integer part IP which is shown with three successive values: $N-1$, N , $N+1$. The corresponding values of FP are: 1.25, 0.25 and -1.25, so that the sum of IP and FP equals $N + 0.25$ in each case. It can be seen that this average division value can be achieved in three different ways by an appropriate selection of FP for any one of the three different values of IP. Still greater ranges of FP are possible
 30 using other parameters in the output logic stage 62 of the modulator. Values of IP and FP may be selected with greater flexibility than possible in conventional synthesisers where the value of FP is generally limited to $\{0,1\}$ at best. The extended range for FP provides an advantage in situations where a change in frequency of the synthesiser would conventionally require a change in both the
 35 integer and fractional parts of the average division ratio. Changes in frequency

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within the broader range possible for the value of FP can now be accommodated by a change in the fractional part alone. Less information regarding frequency changes need be programmed in the controller 17 of a frequency synthesiser incorporating the preferred modulator.

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Figure 11 shows a three stage modulator 110 formed by a cascade of first order modulators 111, 112, 113 such as that shown in Figure 6. Overall the control word k produces a complex signal Y which may be provided for the divider 25 in Figure 2 to determine the fractional part FP of the average division value in the feedback
10 loop 10. Each modulator may have a different quantisation function, and in this example they are seen to have 1, 2, 3 bit outputs respectively. This arrangement is generally similar to that of Figure 5 except that scaling functions must now be included so that the output levels of the respective quantisers are combined correctly. The example is simplified in that the modulators are each assumed to have an n-bit
15 adder 61. Output of modulators 111, 112, 113 are scaled by S12, S22, S32 respectively before passage through the delay elements 114 to the combination stage 115. The inputs of modulators 112, 113 may also be scaled by S21, S31. In general the scaling is dependent on the capacity of the adder 61, the first quantisation step and the overload point of each modulator.

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Figure 12 is a table outlining a selection of scale factors for possible implementations of the modulators in Figure 11, assuming that the adders 61 shown in Figure 6 all have equal length. Overall resolution of the arrangement is determined by the first stage which must have sufficiently high capacity. Capacity
25 of the later stages can be reduced without substantial loss of noise shaping ability. A preferred arrangement is shown in the fourth row of the table, where a modulator having a quantiser with 4-levels is followed by two each with 2-levels. Scaling by a power of 2 is straightforward in binary signals and by careful design can be done without additional hardware.

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Figure 13 is a table outlining some properties of a small number of possible multi-level modulators of the kind shown in Figure 6. The table includes an indication of the range of possible output levels in a third order modulator such as shown in Figure 11 when formed by an arrangement of first order modulators having identical
35 properties. Ranges of up to $\{-3.5, 3.5\}$ in the fractional part of the division ratio

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which can be achieved in a frequency synthesiser are indicated, by way of example. Still higher ranges are possible with other implementations. This table includes modulators having both even and odd numbers of quantisation levels and with a linear relationship between decision regions and feedback levels. Non-linear relationships can also be created if required to avoid output of particular spurs.

Figures 14a, 14b are output samples for the modulator arrangements in Figures 5, 11 respectively. Rows I, II, III in each case represent output from each of the three first order modulators 51, 52, 53 and 111, 112, 113 before input to the respective delay elements 54, 114. Row IV in each case represents output from the combination stages 55, 115. A limit cycle in the output of the first modulator stage is indicated and causes fractional spurs.

Figure 15 shows a further preferred modulator 150 formed from the modulator 60 of Figure 6 by addition of a dither signal in the feedback process. The dither signal is preferably pre-filtered as mentioned in relation to Figure 4d to avoid a noise floor. Only a finite number of feedback signals are generated by the logic stage 63 and a new stage 153 is readily formed by combining the dither signal d as an additional input. As before a group of t msbs is received from adder 61. An m bit output from the logic stage is selected from a set of predetermined coefficients according to the values S and D. The output of adder 64 now a quantisation error signal with a dither signal to reduce the likelihood that a limit cycle will develop for a particular control word X. A cascade of modulators such as shown in Figure 11 may include one or more dithered stages.

Figure 16 is a table indicating a possible range of coefficients for the feedback logic stage 153 when the modulator 150 implements a two level quantiser function. F is the coefficient value which would be passed to adder 64 in the absence of dither. L represents the value added in response to the dither signal d. The value of L is limited to avoid overload and an increase in background noise.

A modulator according to the present invention can be used in a variety of electronic systems other than frequency synthesisers. In digital-to-analog conversion for example. It is possible to use the modulator in various cascade arrangements such

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as shown in Figure 11. It is also possible to form a higher order system by nesting a number of modulators and providing suitable feedback.

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CLAIMS:

1. A frequency synthesiser comprising:
a phase lock loop including a programmable frequency divider, and
5 a controller which determines average fractional division values for the divider,
wherein each division value comprises selected integer and fractional parts,
and
the selected fractional part varies over a range other than $\{0,1\}$.
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2. A synthesiser according to claim 1 wherein the range of the fractional part is substantially symmetrical about $\{0\}$.
3. A synthesiser according to claim 1 wherein the range of the selected
15 fractional part is greater than $\{-0.5, 0.5\}$.
4. A frequency synthesiser comprising:
a phase lock loop including a programmable divider, and
a divider control means which provides a signal to the divider to cause
20 fractional division and thereby produce a required output frequency from the loop,
wherein the control means includes at least one digital modulator having an adder, a latch coupled between an output and input of the adder, and an output logic stage which carries out a logical operation on one or more bits which are output by
25 the adder.
5. A synthesiser according to claim 4 wherein:
the signal from the control means includes a fractional control signal produced by the digital modulator and an integer control signal, and
30 in response to the fractional control signal the divider carries out a division process which produces a divide ratio having a fractional part which is selectable over a range other than $\{0,1\}$.

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6. A synthesiser according to claim 4 wherein:
the digital modulator includes a feedback logic stage which carries out a logical operation on the one or more bits which are output by the adder.

5 7. A synthesiser according to claim 6 wherein:
the latch is coupled to both the output of the adder and to the feedback logic stage to produce an input for the adder.

8. A frequency synthesiser comprising:
10 a phase locked loop including a programmable divider, and
a divider control means which provides a signal to the divider to cause fractional division and thereby produce a required output frequency from the loop,
wherein the control means includes at least one digital modulator having an adder, a latch between an output and an input of the adder, and a feedback logic
15 stage which carries out a logical operation on one or more bits which are output by the adder.

9. A synthesiser according to claim 8 wherein:
the operation carried out by the feedback logic stage includes dithering by
20 multiplexing the one or more bits output by the adder with a signal derived from a pseudo-random sequence.

10. A synthesiser according to claim 8 wherein:
the digital modulator includes an output logic stage which carries out a
25 logical operation on the one or more bits which are output by the adder.

11. A synthesiser according to claim 9 wherein:
the output logic stage provides a fractional control signal for the divider to produce a division value having a fractional part which is selectable over a range
30 other than {0,1}.

12. A synthesiser according to claim 8 wherein:
the latch is coupled to both the output of the adder and the feedback logic stage to produce an input for the adder.

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13. A digital modulator comprising:

an adder which receives a control signal and a feedback signal as inputs and produces a multi-bit output by addition of the inputs,

5 an output logic stage which receives an input derived from at least one bit of the output of the adder and carries out a logical operation on that input to produce a modulator output signal, and

a feedback path including a latch which receives at least one group of bits derived from the output of the adder to produce the feedback signal.

10 14. A modulator according to claim 13 wherein:

the feedback path includes a feedback logic stage which receives an input derived from at least one bit of the output of the adder and carries out a logical operation on that input to produce an output which is used to derive at least part of the feedback signal.

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15. A modulator according to claim 13 wherein:

the feedback path includes a second adder which receives an input of at least one bit from the output of the first adder and an input of at least one corresponding bit from the feedback logic stage and produces an output which forms part of the feedback signal.

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16. A modulator according to claim 13 wherein:

the latch receives an input of at least one bit of the output of the adder and an input derived from the output of the feedback logic stage and produces the feedback signal for input to the adder.

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17. A modulator according to claim 13 wherein:

the output logic stage functions as a multi-level quantiser.

30 18. A modulator according to claim 14 wherein:

the feedback logic stage combines a dither signal with output received from the adder.

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19. A modulator arrangement comprising:
two or more modulators each having an adder, a latch coupled between an
output and an input of the adder, and an output logic stage,
wherein the modulators are connected so that output of the latch in each
5 modulator is coupled to an input of the adder in a subsequent modulator, if any, and
the output of the logic stage in each modulator is coupled to a common
combination stage to produce an output for the arrangement.
20. An arrangement according to claim 19 wherein:
10 at least two of the output logic stages have a different number of digital
output levels and are coupled to the combination stage through a scaling element.
21. An arrangement according to claim 19 wherein:
the adders of at least two successive modulators are of different lengths and
15 the latch of the first successive modulator is coupled to an input of the second
successive modulator through a scaling element.
22. An arrangement according to claim 19 wherein:
the output of the logic stage in each modulator is coupled to the combination
20 stage through one or more delay elements.