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ABSTRACT

A METHOD TO FORM AN AIR-GAP UNDER THE EDGES OF A GATE ELECTRODE BY USING DISPOSABLE SPACER/LINER

A method of fabricating an air-gap spacer of a semiconductor device, comprising the following steps. A semiconductor substrate having at least a pair of STIs defining an active region is provided. A gate electrode is formed on the substrate within the active region. The gate electrode having an underlying gate dielectric layer. A liner oxide layer is formed over the structure, covering the sidewalls of the gate dielectric layer, the gate electrode, and over the top surface of the gate electrode. A liner nitride layer is formed over the liner oxide layer. A thick oxide layer is formed over the structure. The thick oxide, liner nitride, and liner oxide layers are planarized level with the top surface of the gate electrode, and exposing the liner oxide layer at either side of the gate electrode. The planarized thick oxide layer is removed with a portion of the liner oxide layer and a portion of the gate dielectric layer under the gate electrode to form a cross-section inverted T-shaped opening on either side of the gate electrode. A gate spacer oxide layer is formed over the structure at least as thick as the gate electrode, wherein the gate spacer oxide layer partially fills the inverted T-shaped opening from the top down and wherein air gap spacers are formed proximate the bottom of the inverted T-shaped opening. The gate spacer oxide, liner nitride, and liner oxide layers are etched to form gate spacers proximate the gate electrode. The gate spacers having an underlying etched liner nitride layer and liner oxide layer.

FIGURE 2

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