MULTIPLE-GATE TRANSISTORS WITH IMPROVED GATE CONTROL

ABSTRACT OF THE DISCLOSURE

A method for fabricating a multiple-gate device including the steps of providing a substrate of a semi-conducting layer on an insulator stack which includes an insulator layer overlying an etch-stop layer; patterning a semi-conducting layer forming a semiconductor fin; etching the insulator layer at the base of the fin forming an undercut; depositing a gate dielectric layer overlying the fin; depositing an electrically conductive layer over the gate dielectric layer; etching the electrically conductive layer forming a gate straddling across the two sidewall surfaces and the top surface of the fin; and forming a source region and a drain region in the fin.

FIG. 5E