

Silicon wafer for semiconductor and manufacturing method thereof

Detailed Description of the Invention:

Field of the Invention

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The present invention relates to a silicon wafer obtained by performing heat treatment of a silicon wafer (hereinafter, referred to as "substrate") that has not undergone heat treatment in a stage in which the latter silicon wafer has just been sliced from a silicon single crystal ingot in a semiconductor wafer manufacturing technical field, and in particular to a silicon wafer with high quality that does not include crystal defects in a semiconductor device forming region by suppressing occurrences of slip dislocation and warpage and a manufacturing method thereof.

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Background of the Invention

A silicon wafer used as a substrate for a semiconductor device or the like is manufactured by slicing a silicon single crystal ingot to perform heat treatment, mirror polishing, or the like to the sliced ingot. As a manufacturing method of such a silicon single crystal ingot, for example, there is the Czochralski method (CZ method). The CZ method occupies most part of manufacture of a silicon single crystal ingot because of such a reason that it is easy to obtain a single crystal ingot with a large diameter or control of defects is relatively easy.

A silicon single crystal (CZ-Si) pulled by the CZ method includes crystal defects called "grown-in defects". The CZ-Si takes in oxygen among lattices in a supersaturated state, but such supersaturated oxygen (oxygen precipitation) causes induction of fine defects called "BMDs" (Bulk Micro Defects) in a heat treatment (anneal) conducted thereafter.

In order to form a semiconductor device on a silicon wafer, it is required that no crystal defect is present in a semiconductor device

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forming region. This is because, when crystal defects are present in a surface on which a circuit should be formed, a circuit break or the like is caused from the defect portion. Meanwhile, it is required that the silicon wafer includes BMDs in a proper amount
5 therein. The BMDs serve to getter metal impurities or the like. Metal impurities cause semiconductor device malfunctions.

In order to satisfy the above requirements, a technique for performing high-temperature anneal to a silicon wafer to induce BMDs
10 in the silicon wafer to form an IG (intrinsic gettering) layer and diminishing grown-in defects present in a surface of the silicon wafer to form a DZ (denuded zone) layer where crystal defects are reduced without limit is used.

As a specific example, a method for performing high-temperature anneal to a nitrogen-added substrate or a substrate added with not only nitrogen but also hydrogen to reduce grown-in defects on a surface of the substrate and form BMD including nitrogen as core inside the substrate has been proposed (JP-A-10-98047 and
20 JP-A-2000-281491).

However, oxygen concentrations in DZ layers formed on a surface and a back surface of a silicon wafer in the above-mentioned high-temperature anneal process are extremely lowered due to
25 external diffusion of oxygen during heat treatment. As a result, since restraint of dislocation defect extension on the wafer surface and back surface lowers considerably, slips (dislocation defects) easily extend from fine flaws on the surface and the back surface introduced in the anneal process into a bulk, which results in such
30 a problem that strength of the silicon wafer lowers due to extension of such slip dislocation. For example, when a silicon wafer is annealed in a state that it is supported by heat treatment ports or the like, slip dislocations often extend from the supported portions around the back face of the wafer. There is such a case
35 that slip dislocation extends from a silicon wafer edge portion.

When the strength of the silicon wafer lowers, there is a concern that such a situation that a wafer is damaged or broken during manufacturing step occurs. However, the DZ layer is inevitable for semiconductor device formation, and a silicon wafer that has a DZ layer and is excellent in strength property has been required.

In a conventional art described in JP-A-10-98047 or JP-A-2000-281491, attention was not paid to strength lowering of a silicon wafer, and a silicon wafer manufactured by such a method could not avoid extension of slip dislocation.

Meanwhile, in order to prevent occurrence of such slip dislocation, a method for generating BMDs at a high density has been proposed.

Specifically, a silicon wafer manufacturing method where oxygen precipitation nuclei with sizes of 20nm or less in an amount of 1×10^{10} atoms/cm³ or more are formed in the BMD layer by applying rapid temperature rising/falling heat treatment to a substrate sliced from a silicon signal crystal ingot at a temperature of 500 to 1200°C within a range of 1 to 600 minutes under atmosphere of mixed gas of nitrogen gas and inert gas or mixed gas of ammonia gas and inert gas has been proposed (JP-A-2006-40980). A silicon wafer where BMDs with a high concentration of (1×10^{10} atoms/cm³ to 1×10^{12} atoms/cm³) have been generated by repeating heat treatment steps several times has been also proposed (JP-A-08-213403).

However, since a diameter of a silicon wafer is increased and a rapid temperature rising/falling heat treatment utilizing a Rapid Thermal Annealer (RTA) is frequently used in recent years, besides occurrence of slip dislocation, warpage occurred in a wafer becomes problematic.

An illustrative diagram of slips and warpage introduced by the RTA heat treatment is shown in Fig. 1. Slips are introduced from a

contacting point between a wafer back surface and a wafer holding portion. The introduced slips extend in a 110 direction, which causes wafer damage or breaking in some cases. The warpage is a phenomenon where a wafer is deformed due to heat strain during the RTA heat treatment. In a wafer of 100 plane, for example, a mountain-shaped portion and a valley-shaped portion appear, as shown in Fig. 1. A warpage of a silicon wafer in a stage of shipping is equal to or less than 10 μ m. However, such a case that a difference in height between the mountain and the valley reaches several tens μ m when a silicon wafer is applied with heat treatment such as RTA occurs. When the warpage becomes large, a semiconductor device pattern cannot be exposed on a wafer surface, which causes lowering in semiconductor device yield. Besides slip, high-density dislocation is present inside a silicon wafer where a large warpage has occurred. It is considered that these cause the warpage.

The problem of the warpage becomes significant when a wafer diameter becomes equal to or more than 200mm, and it is impossible to avoid the problem by only simply regulating the BMD concentration to a high concentration like the above.

A demand for a silicon wafer with high quality that does not include crystal defects in a semiconductor device forming region while suppressing occurrences of slip dislocation and warpage in a device manufacturing process and a manufacturing technique thereof is increasing under such a technical background.

Disclosure of the Invention

Problem to be solved

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It is an object of the present invention to provide a silicon wafer with high quality where both slip dislocation and warpage are suppressed to be considerably small, which is suitable for diameter enlargement, and a manufacturing method thereof.

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Means for solving the problem

The present inventors have carried out extensive studies about a relationship among BMD size distribution, slip dislocation, and warpage for making it possible to manufacture an excellent silicon wafer satisfying the above demand. As a result, the present inventors have clarified an optimal BMD size distribution for preventing both slip dislocation and warpage and have reached the present invention.

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The present invention relates to the following (1) to (10).

(1) A silicon wafer wherein a density of BMDs with sizes of 20nm to 40nm of BMDs present at a deep position which is spaced from a surface of a silicon wafer by a distance equal to or more than 20 μ m is in a range of $5 \times 10^{11}/\text{cm}^3$ to $5 \times 10^{13}/\text{cm}^3$, and a density of BMDs with sizes of 300nm or more is equal to or less than $1 \times 10^7/\text{cm}^3$.

(2) The silicon wafer described in the above (1), including nitrogen.

(3) The silicon wafer described in the above (1) or (2), including hydrogen.

(4) A manufacturing method of a silicon wafer described in any one of the above (1) to (3), comprising growing a silicon single crystal ingot while maintaining a cooling rate in a range in which a center temperature of crystal during silicon single crystal growth changes from 1000°C to 900°C in 5°C/min or more; and after applying heat treatment to a substrate sliced from the ingot at a temperature of 400°C to 850°C for 30 minutes to 4 hours, applying heat treatment to the substrate at a temperature of 1100°C to 1250°C for 10 minutes to 2 hours under atmosphere of rare gas having an impurity concentration of 0.5% or less at a volume ratio or under non-oxidizing atmosphere where a thickness of an oxidized film after heat treatment is suppressed to 2nm or less as a high-temperature anneal step.

(5) The manufacturing method of the silicon wafer described in the above (4), wherein an oxygen concentration of the substrate just after being sliced from a crystal is in a range of 7×10^{17} atoms/ cm^3 to 9×10^{17} atoms/ cm^3 .

(6) The manufacturing method of the silicon wafer described in the above (4) or (5), wherein a nitrogen concentration of the substrate just after being sliced from a crystal falls in a range of 1×10^{13} atoms/cm³ to 8×10^{15} atoms/cm³.

5 (7) The manufacturing method of the silicon wafer described in the above (6), wherein the growth of the silicon single crystal ingot is performed from melt added such that nitrogen falls in a range of 1×10^{16} atoms/cm³ to 1×10^{19} atoms/cm³.

(8) The manufacturing method of the silicon wafer described in any
10 one of the above (4) to (7), wherein a hydrogen concentration of the substrate just after being sliced from a crystal falls in a range of 1×10^{12} atoms/cm³ to 5×10^{16} atoms/cm³.

(9) The manufacturing method of the silicon wafer described in the above (8), wherein the growth of the silicon single crystal ingot
15 is performed under atmosphere where hydrogen gas is continuously introduced such that a concentrate of the hydrogen gas falls in a range of 0.01% to 3% at a volume ratio.

(10) The manufacturing method of the silicon wafer described in any one of the above (4) to (9), wherein a silicon single crystal layer
20 (epi-layer) is deposited by epitaxial method after the high-temperature anneal.

(Effect of the Invention

25 The silicon wafer of the present invention makes it possible to manufacture a silicon wafer with a large diameter (typically, 200mm or more) with high quality by performing such setting that a density of BMDs with sizes of 20nm to 40nm of BMDs present at a deep position which is spaced from a surface of a silicon wafer by a distance of
30 20μm or more is in a range of 5×10^{11} /cm³ to 5×10^{13} /cm³, and a density of BMDs with sizes of 300nm or more is equal to or less than 1×10^7 /cm³, thereby suppressing both slip dislocation and warpage extremely small.

The silicon wafer of the present invention is reduced in occurrence
35 of slip dislocation and warpage as compared with a mirror wafer that

has no BMD inside a wafer, and it is also excellent in gettering ability.

Best Embodiment for carrying out the Invention

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Silicon Wafer

A feature of the silicon wafer according to the present invention lies in that a density of BMDs with sizes of 20nm to 40nm of BMDs present at a deep position which is spaced from a surface of a silicon wafer by a distance of 20 μ m or more is in a range of $5 \times 10^{11}/\text{cm}^3$ to $5 \times 10^{13}/\text{cm}^3$, which is introduced from the present inventors' findings and facts described below.

From the result of the specific examinations of a state of BMDs generated inside a wafer after heat treatment which has been conducted by the present inventors, the present inventors have clarified such a fact that a wide size distribution is present in BMDs. Then, the present inventors have examined a relationship among the BMD size distribution, which is present at a deep position which is spaced from a surface of a silicon wafer by a distance of 20 μ m or more and influences the characteristics of slips and warpage, the slips and the warpage. As a result, they have obtained a finding, described below, clarifying an optimal BMD size for preventing slip. That is, by generating BMDs with sizes of 20nm to 40nm at a density of $5 \times 10^{11}/\text{cm}^3$ to $5 \times 10^{13}/\text{cm}^3$, lengths of slips can be suppressed to equal to or less than 10mm. When the lengths of slips are equal to or less than 10mm, the slips are not exposed to a surface of the silicon wafer. Even if a slip occurs at a wafer edge portion, when the length of the slip is equal to or less than 10mm, the slip does not reach a semiconductor device forming region, and it does not influence a device adversely.

When sizes of BMDs are less than 20nm or a BMD density is less than $5 \times 10^{11}/\text{cm}^3$, BMDs do not serve as a sufficient barrier with respect to slip propagation. There is no upper limit to the density and

sizes of BMDs which may serve as a barrier to slip propagation, but upper limits of ranges of the BMD density and the size realized in an actual silicon wafer are $5 \times 10^{13}/\text{cm}^3$ and 40nm, respectively because of the reason described later.

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The range of the density of BMDs is introduced from the fact described below. That is, when the BMDs are present at a high density, such a state that almost all solid solution oxygen has precipitated as BMDs occurs. Meanwhile, the number of oxygen atoms precipitating as BMDs does not exceed the number of oxygen atoms solved in CZ-Si in solid manner and the upper limit of a solid solution oxygen concentration is about $1 \times 10^{18} \text{ atoms}/\text{cm}^3$ at most. Therefore, it can be thought that a density of oxygen atoms precipitating as BMDs is about $1 \times 10^{18} \text{ atoms}/\text{cm}^3$ and it is constant in a state that BMDs are present at a high density. In this state, when the number of BMDs increases, individual sizes of BMDs become small, while the number decreases when the BMD size becomes large. That is, it is understood that there are upper limits in the size and the density of the BMDs present at a high density. Accordingly, it is impossible to realize BMDs present at a density of $5 \times 10^{11}/\text{cm}^3$ such that their sizes are more than 40nm, and it is impossible to realize BMDs with sizes of 20nm or more such that a density of the BMDs is more than $5 \times 10^{13}/\text{cm}^3$. Therefore, it is understood that ranges of the BMD density and the BMD size which can suppress slip propagation can be achieved by regulating the sizes of BMDs in a range of 20nm to 40nm and regulating the density thereof in a range of $5 \times 10^{11}/\text{cm}^3$ to $5 \times 10^{13}/\text{cm}^3$.

It is preferable that the BMD density is higher in such a range. In order to suppress the length of the slip to 5mm or less, it is more preferable that the BMD density is equal to or more than $1 \times 10^{12}/\text{cm}^3$.

Another feature of the silicon wafer according to the present invention lies in that the density of BMDs with sizes of 300nm or more is equal to or less than $1 \times 10^7/\text{cm}^3$. This is based upon the

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present inventors' finding described below.

That is, when thermal stress acts on a wafer, high-density dislocation is generated within the wafer from BMDs with large sizes acting as a starting point. As a result, the wafer is plastically deformed, which causes warpage. On the contrary, when BMDs serving as the starting point of dislocation decrease, even if thermal stress acts on a wafer, plastic deformation becomes hard to occur, and warpage is reduced. Especially, BMDs with sizes of 300nm or more tends to act as a source of generation dislocation easily, and the density of such BMDs exceeds $1 \times 10^7/\text{cm}^3$, dislocation inside a wafer becomes high density, which causes a warpage exceeding 20 μm . Accordingly, by suppressing the density of the BMDs with sizes of 300nm or more to $1 \times 10^7/\text{cm}^3$ or less, the warpage can be suppressed to 20 μm or less. Further, if the warpage of the wafer is equal to or less than 20 μm , a positional deviation occurring when a semiconductor device pattern is exposed on a silicon wafer does not exceed an allowable range.

Accordingly, the density of BMDs with sizes of 300nm or more exceeds $1 \times 10^7/\text{cm}^3$, the warpage becomes equal to or more than 20 μm undesirably.

As the heat treatment for evaluating resistance properties to the slip or the warpage, it is preferable to perform a heat treatment for performing temperature rising/falling at a rate of 30°C/sec or more in a temperature range from 700°C to 1100°C to maintain a silicon wafer at a temperature of 1100°C or more. Here, the reason why the heat treatment temperature is set to be equal to or more than 700°C is because, when the heat treatment temperature becomes equal to or more than 700°C, generation of slip dislocation or a warpage becomes easy. The reason why the heat treatment temperature is set to be equal to or less than 1100°C is because an upper limit of the heat treatment temperature in the device process is about 1100°C and a phenomenon which happens in a device process heat treatment

can be predicted approximately by examining characteristics up to 1100°C. Further, the reason why the temperature rising/falling rate is set to be equal to or more than 30°C/sec is because, when the temperature rising/falling rate becomes equal to or more than
5 30°C/sec, thermal stress acting on a silicon wafer becomes large so that occurrence of slips or a warpage becomes significant. Accordingly, if generation of dislocation is prevented in the temperature range and the temperature rising/falling rate range, it is said that such a silicon wafer is a silicon wafer where slip
10 dislocation and warpage are not generated in a general device process.

The feature of the silicon wafer according to the present invention lies in that the length of the slip generated in the abovementioned
15 heat treatment is equal to or less than 10mm and a warpage amount of the wafer after heat treatment is equal to or less than 20µm.

The silicon wafer according to the present invention includes the silicon wafer added with nitrogen and the silicon wafer added with
20 hydrogen. This is based upon the present inventors' finding described regarding a manufacturing method of a silicon wafer according to the present invention.

Incidentally, measurements of the BMD size distribution and the BMD
25 density can be made utilizing a conventional known measuring method. Specifically, such measurement includes measurement utilizing a transmission electron microscope and/or an Optical Precipitate Profiler or the like.

Slip dislocation in a wafer can be measured by a conventional known
30 measuring method. For example, such measurement includes measurement utilizing an X-ray topograph.

Further, warpage of a wafer can be measured by a conventional known
35 measuring method. Specifically, an amount of warpage after heat

treatment can be evaluated by performing observation using FT-90A manufactured by NIDEK Corporation, or the like.

Manufacturing Method of Silicon Wafer

5 A manufacturing method of a silicon wafer according to the present invention is a method for manufacturing a silicon wafer having the features described above.

10 Regarding a growing method of a silicon single crystal ingot used in the manufacturing method of a silicon wafer according to the present invention, the CZ method can be preferably used but the FZ method can be used by controlling an oxygen concentration contained in a substrate. The growing method can be selected properly according to a kind of a semiconductor silicon wafer, performance,
15 or the like which is required without including limitation about presence/absence of dope of various elements and a size (a diameter, a weight or the like) of an intended ingot.

A silicon single crystal manufacturing device used for the
20 manufacturing method of a silicon wafer according to the present invention is not limited especially and any one used for silicon single crystal manufacture according to the normal CZ method is preferably used.

25 A method for slicing a substrate from a silicon single crystal ingot, which is used in the manufacturing method of a silicon wafer according to the present invention is not limited and a conventional known method can be used. Specifically, a slicer with an inner peripheral blade, a wire saw, or the like can be used for the method.

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Devices used in the heat treatment and the high temperature anneal step according to the present invention are not limited, and conventional known devices can be preferably used. Specifically, the device used in the heat treatment includes a vertical furnace
35 of a batch type, and the device used in the high temperature anneal

step includes a vertical furnace of a batch type having an oxygen purge function. Both the heat treatment and the high temperature anneal step can be conducted continuously using the vertical furnace of a batch type having an oxygen purge function.

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The feature of the manufacturing method of a silicon wafer according to the present invention lies in growing a silicon single crystal ingot while maintaining a cooling rate in a range in which a center temperature of crystal during silicon single crystal growth changes from 1000°C to 900°C in 5°C/min or more. This is based upon the present inventors' finding that the temperature range where the abovementioned cooling rate is maintained influences the BMD size lowering considerably and when growth is performed while maintaining the cooling rate in such a range, the density of BMDs with sizes of 300nm or more can be suppressed to $1 \times 10^7/\text{cm}^3$ or less. Further, even if cooling is performed at the abovementioned cooling rate in a temperature range except for such a temperature range, it is not effective for the BMD size reduction so much.

It is preferable that the cooling rate is increased in such a temperature range, and it is more preferable that the cooling rate is set to 7°C/min or more in order to suppress the density of BMDs with sizes of 300nm or more to $1 \times 10^7/\text{cm}^3$ or less.

Another feature of the manufacturing method of a silicon wafer according to the present invention lies in, after applying heat treatment to a substrate sliced from the silicon single crystal ingot grown by the abovementioned growing method at a temperature of 400°C to 850°C for 30 minutes to 4 hours, applying heat treatment to the substrate at a temperature of 1100°C to 1250°C for 10 minutes to 2 hours in rare gas having an impurity concentration of 0.5% or less at a volume ratio or under non-oxidizing atmosphere where a thickness of an oxidized film after heat treatment is suppressed to 2nm or less as a high-temperature anneal step. This is based upon the present inventors' finding described below.

That is, the present inventors have found that performing heat treatment at a relatively low temperature where the heat treatment temperature is in a range of 400°C to 850°C is remarkably effective
5 for manufacturing a silicon wafer having the abovementioned high BMD density from a lower end of the DZ layer toward the center of a wafer thickness. The DZ layer is then formed by performing the following high-temperature anneal step. Incidentally, the high density BMDs formed by the low-temperature heat treatment did not
10 disappear even in the high-temperature anneal step.

When the heat treatment temperature is less than 400°C, since diffusion of oxygen does not occur sufficiently, the BMD form does not occur, therefore the BMD density becomes less than $5 \times 10^{11}/\text{cm}^3$,
15 which is undesirable. When the heat treatment temperature is more than 850°C, since disappearance of the BMD cores occurs, the BMD density becomes less than $5 \times 10^{11}/\text{cm}^3$, which is undesirable.

When the heat treatment time is less than 30 minutes, since diffusion
20 of oxygen does not occur sufficiently, the BMD form does not occur, therefore the BMD density becomes less than $5 \times 10^{11}/\text{cm}^3$, which is undesirable. When the heat treatment time exceeds 4 hours, a BMD total density exceeds $5 \times 10^{13}/\text{cm}^3$, the density of BMDs with sizes of 20nm or more of all the BMDs becomes less than $5 \times 10^{11}/\text{cm}^3$, and the
25 wafer manufacturing step is further prolonged, which results in undesirable productivity lowering.

It is necessary to suppress oxidized film growth on a surface of the wafer by performing the following high-temperature anneal step
30 under a rare gas atmosphere where an impurity concentration is 0.5% or less at a volume ratio. When the impurity concentration exceeds 0.5% at a volume ratio, the oxidized film on the surface exceeds 2nm, which is undesirable. The reason for suppressing the oxidized film on the surface 2nm or less is for promoting outward diffusion
35 of oxygen and facilitating void contraction and disappearance in

the vicinity of the surface. Meanwhile, when the oxidized film on the surface exceeds 2nm, outward diffusion of oxygen on the surface near the wafer surface is suppressed. As a result, inner wall oxidized films of voids in the vicinity of the wafer surface do not melt so that void contraction and disappearance do not occurs during anneal, which is undesirable.

When the abovementioned anneal temperature is less than 1100°C, a contraction rate of voids is low so that voids near the surface remains, which is undesirable. When the anneal temperature exceeds 1250°C, since degradation of members for the anneal furnace is significant, a replacement frequency of members becomes high, which results in undesirable increase in cost.

When the abovementioned anneal time is less than 10 minutes, time for the void contraction is short so that voids near the surface remains undesirably. When the anneal time exceeds 2 hours, a total anneal time becomes long, which results in deterioration of productivity, which is undesirable.

The manufacturing method of a silicon wafer according to the present invention includes the manufacturing method where an oxygen concentration of the substrate just after being sliced from a crystal is in a range of 7×10^{17} atoms/cm³ to 9×10^{17} atoms/cm³. This is based upon the present inventors' finding described below.

That is, by setting an oxygen concentration of the substrate just after being sliced from a single crystal ingot to 7×10^{17} atoms/cm³ or more, a high density of BMDs with a density of 5×10^{11} /cm³ or more can be realized when heat treatment is performed in a temperature range of 400°C to 850°C for a time period from 30 minutes to 4 hours. By setting the oxygen concentration of the substrate to 9×10^{17} atoms/cm³ or less, disappearance of grown-in defects present on the surface of the silicon wafer is facilitated by the high-temperature anneal. By setting the oxygen concentration to 9×10^{17} atoms/cm³

or less, it becomes possible to form a wide DZ layer with a width of 5 μ m or more.

Manufacturing a substrate having the abovementioned oxygen concentration can be adjusted by appropriately controlling an oxygen concentration in melt, the number of rotations of a crucible, or the like.

The manufacturing method of a silicon wafer according to the present invention includes the manufacturing method of the silicon wafer where a nitrogen concentration in the substrate just after being sliced from the single crystal ingot is set in a range of 1×10^{13} atoms/cm³ to 8×10^{15} atoms/cm³. This is based upon the present inventors' finding described below.

That is, when the nitrogen concentration in the substrate just after being sliced from the single crystal ingot is in a range of 1×10^{13} atoms/cm³ to 8×10^{15} atoms/cm³, a silicon wafer obtained by the abovementioned heat treatment where the BMD density has the abovementioned feature can be further reduced in warpages compared with a case of a substrate which is not added with nitrogen.

When the nitrogen concentration in the substrate is equal to or more than 1×10^{13} atoms/cm³, propagation of dislocation generated by BMDs is suppressed so that warpage can be further reduced compared with the case of a substrate which is not added with nitrogen, but when the nitrogen concentration is equal to or more than 8×10^{15} atoms/cm³, multi-crystallization takes place, which may result in lowering of yield, which is undesirable.

The substrate can be realized by conducting growth of a silicon single crystal ingot in the CZ method from melt added with nitrogen in an amount of 1×10^{16} atoms/cm³ to 1×10^{19} atoms/cm³.

As methods for adding nitrogen to melt, the conventional known method

can be used preferably. Specifically, the adding methods include a method for dipping a wafer with a nitride film in melt.

5 The manufacturing method of a silicon wafer according to the present invention includes the manufacturing method of the silicon wafer where a hydrogen concentration in the substrate just after being sliced from a single crystal ingot is set in a range of 1×10^{12} atoms/cm³ to 5×10^{16} atoms/cm³. This is based upon the present inventors' finding described below.

10 That is, even if the oxygen concentration is relatively low, a more preferable BMD density of 1×10^{12} /cm³ or more can be realized by addition of hydrogen. The low oxygen concentration is effective for forming a DZ layer with further reduced crystal defects. Even
15 if annealing is performed in a low-temperature heat treatment for a relatively short time, the abovementioned BMD density can be realized by the hydrogen addition. Such a merit is advantageous regarding a point that an annealed wafer with further reduced surface defects can be manufactured at a low cost.

20 The hydrogen concentration must be 1×10^{12} atoms/cm³ or more in order to achieve the abovementioned effect, but when the hydrogen concentration exceeds 5×10^{16} atoms/cm³, bubble defects due to hydrogen occur, which is undesirable.

25 The substrate can be realized by continuously introducing hydrogen gas into the atmosphere during crystal growth such that a concentration of the hydrogen gas is in a range of 0.01% to 3% at a volume ratio to perform growth.

30 When the concentration of the hydrogen gas is less than 0.01%, the hydrogen concentration in the substrate does not reach 1×10^{12} atoms/cm³ or more, which is undesirable. When the concentration of the hydrogen gas exceeds 3%, the hydrogen concentration in the
35 substrate exceeds 5×10^{16} atoms/cm³, which results in occurrence of

bubble defects, which is undesirable.

The manufacturing method of a silicon wafer according to the present invention includes the manufacturing method of a silicon wafer where
5 a silicon single crystal layer (epi-layer) is deposited by the epitaxial method after the high-temperature anneal.

The present invention will be further explained below in detail referring to Examples, but the present invention is not limited to
10 the Examples.

Examples

Manufacturing method of annealed wafer and epitaxial wafer
15 Annealed wafers and epitaxial wafers were manufactured in the following manner.

(1) Preparation of Melt:

Silicon and doping agent were filled in a crucible in pulling furnace
20 so as to obtain a desired resistivity.

(2) Growth of single crystal ingot:

After melt was prepared by heating the crucible using a heater, seed
crystal was dipped in the melt and pulled up, and a neck portion
25 and an expanded diameter portion were formed while controlling the number of rotations of the crucible and the number of rotations of the seed crystal. After the expanded diameter portion was formed, a diameter thereof was controlled by utilizing a heater output and a pulling speed, and a straight barrel portion was grown such that
30 its length reached a predetermined length (wafer with diameter of 200mm: 1000mm, wafer with diameter of 300mm: 500mm). Thereafter, a reduced diameter portion was formed and each single crystal ingot was produced by separation from the melt. Conduction types of single crystal ingots obtained were p-type (boron-doped) and n-type
35 (phosphorus-doped).

A cooling rate in a range where a center temperature of crystal changed from 1000°C to 900°C was obtained by the following method. That is, a temperature distribution of a crystal center portion during crystal growth was calculated by heat conduction analysis and an crystal growth axial direction average temperature gradient G [°C/mm] in a range of 1000°C to 900°C was obtained. A crystal growth rate average value V [mm/min] was obtained from the experimental result, and $V \times G$ [°C/min] was determined as a cooling rate.

The heat conduction was performed using FEMAG that was a commercially-available heat conduction analysis software. Rising and falling of the cooling rate in a range where the crystal center temperature changed from 1000°C to 900°C that was calculated according to the abovementioned method were performed by placing a heat shielding plate made from metal with excellent heat conduction (for example, silver) or the like at a position where the crystal center temperature changed from 1000°C to 900°C to properly water-cool the heat shielding plate, or properly changing a structure of the heat shielding plate to change a pulling-up speed.

(3) Adjustment of oxygen concentration, nitrogen concentration, and hydrogen concentration in substrate

Adjustments of an oxygen concentration, a nitrogen concentration, and a hydrogen concentration in a substrate were conducted in the following manner.

1) Oxygen concentration:

Adjustment of the oxygen concentration was conducted by controlling the number of rotations of a crucible or the like to control an oxygen concentration in the crystal. Incidentally, the oxygen concentration in the substrate was measured by the infrared absorption spectrophotometry and a value of JEITA (Japan Electronics and Information Technology Industries Association) was used as a conversion factor.

2) Nitrogen concentration:

A relationship between nitrogen mixed in liquid and a concentration of nitrogen added in crystal was preliminarily obtained, and adjustment of the nitrogen concentration was performed by determining a nitrogen concentration in melt from a nitrogen concentration introduced in an intended substrate and dipping a substrate with a nitrogen film in the melt to control mixed nitrogen in the melt. Incidentally, the nitrogen concentration in the substrate was measured using the secondary ion mass spectrometer (SIMS). The nitrogen concentration equal to or less than 5×10^{14} atoms/cm³ was obtained from calculation using a segregation factor of 0.0007 based upon the concentration of nitrogen added in the melt and the solidification ratio of crystal.

3) Hydrogen concentration:

Crystals were preliminarily manufactured in crystal added with high concentration boron while mixing hydrogen in atmosphere during crystal growth at various volume ratios, a silicon wafer sliced from the obtained crystals was measured by the infrared absorption spectrophotometry, and the hydrogen concentration was obtained from the concentration of a hydrogen-boron pair. A relationship between the volume ratio of the mixed hydrogen and the concentration of hydrogen added in the crystal was preliminarily obtained by this method, and the concentration of hydrogen introduced into the substrate was determined by controlling the volume ratio of the mixed hydrogen. Incidentally, mixing of hydrogen was performed by introducing hydrogen from an argon gas introducing port of a silicon single crystal manufacturing apparatus such that hydrogen had a predetermined volume ratio thereof to argon gas.

(4) Slicing method of substrate:

Substrates obtained by slicing same portions of straight barrel portions of respective single crystal ingots grown by the abovementioned method using a wire saw as a plurality of sheets to apply a mirror processing to them were used as substrates.

(5) Heat treatment (Low-temperature heat treatment and

high-temperature heat treatment):

The obtained substrates were put in a vertical type heat treatment furnace of a batch type having a purge function where a temperature within a reaction chamber was held at a predetermined temperature, and subjected to heat treatment (low-temperature heat treatment) under argon gas atmosphere for a predetermined time. Then, they were subjected to high-temperature heat treatment (1200°C) under argon atmosphere for a predetermined time (200mm: one hour, 300mm: two hours) in the same furnace (hereinafter, the wafer after the heat treatments is called "annealed wafer").

(6) Epitaxial layer deposition:

An epitaxial layer with a thickness of 5 μ m was deposited on a surface of a portion of the annealed wafer using a vapor growth apparatus (hereinafter, the annealed wafer deposited with the epitaxial layer is called "epitaxial wafer").

Measurement and evaluation of annealed wafer and epitaxial wafer

The following measurement and evaluation about the annealed wafer and the epitaxial wafer obtained by the abovementioned method, namely, (1) BMD size distribution measurement, (3) measurement of slip length and evaluation of warpage (RTA heat treatment), and (4) measurement of width of DZ layer, were conducted. Regarding the wafer added with nitrogen, (2) nitrogen concentration was measured.

(1) BMD size distribution:

The BMD size distribution was measured by the infrared interferometry and a transmission electron microscope. As a defect evaluating apparatus based upon an infrared interferometry, an OPP (Optical Precipitate Profiler) manufactured by AXENT Technologies Inc. was used. Three portions positioned at depths of 20 μ m, 100 μ m, and 300 μ m from a surface of each of the annealed wafer and the epitaxial wafer were measured. BMD sizes were obtained from signal intensities obtained by applying electrical signal processing to

phase differences of transmission lasers and an average value of values obtained regarding the three portions was adopted as a representative value. Detection sensitivity was set to a sensitivity which allowed measurement of octahedral BMDs with diagonal lengths of 80nm or more. The BMD size was determined as a diagonal length of an octahedral precipitate. As samples for the transmission electron microscope, samples were sampled from the positions at depths of 20 μ m, 100 μ m, and 300 μ m from the surfaces of the annealed wafer and the epitaxial wafer and BMD sizes were obtained from microscope images obtained by the measurements. The BMD size was determined as a diagonal length of an octahedral precipitate. The BMD density was obtained from the number of BMDs observed in a view field and a volume of the sample corresponding to a region observed. Regarding the BMD density and the BMD size, their average value of values obtained regarding the three portions were determined as representative values. The density of BMDs with sizes of 20nm to 40nm and the density of BMDs with sizes of 300nm or more were obtained from the BMD size distributions obtained by the OPP and TEM.

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(2) Nitrogen concentrations in annealed wafer and epitaxial wafer: Samples were sampled from the annealed wafer and the epitaxial wafer and, after polishing up to 20 μ m was performed in order to remove the outward diffusion layers of nitrogen on surfaces of the wafers, the nitrogen concentrations in the wafers were measured using SIMS.

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(3) Slip lengths in annealed wafer and epitaxial wafer and warpages thereof:

The annealed wafer and the epitaxial wafer were annealed using an RTA (Rapid Thermal Annealer) under the following conditions ten times.

30

Insertion: room temperature

Temperature rising: 50°C/min

Holding: 1100°C for 1 minute

35 Atmosphere: argon

Temperature falling: 30°C/min

Pulling: room temperature

Warpages of the annealed wafer and the epitaxial wafer before the RTA heat treatment and after the RTA heat treatment were measured using FT-90A manufactured by NIDEK Corporation. The annealed wafer after the RTA heat treatment was observed using an X-ray topograph, and the maximum length of lengths of the observed slips was determined as a representative value.

(10 (4) Width of DZ layer of annealed wafer:

A surface of an annealed wafer was re-polished at a polishing depth $X\mu\text{m}$, and defects present on a whole face of the re-polished annealed wafer were measured using LSTD scanner (MO-6) manufactured by MITSUI MINING & SMELTING CO., LTD. Since the detection depth obtained by the MO-6 was a depth from the surface of the wafer up to $1\mu\text{m}$, defects detected after re-polishing up to $X\mu\text{m}$ were present from the original annealed wafer surface in a depth range of X to $(X+1)\mu\text{m}$. The detection sensitivity was set to a sensitivity which allowed measurement of grown-in defects with a diagonal length of 100nm. The volume density of the defects was calculated by dividing the total number of the defects detected by the MO-6 by an area of the measured region and a measurement depth of $1\mu\text{m}$. Re-polishing was conducted while changing the polishing depth X variously, and a polishing depth when the volume density of the measured defects became $0.1 \text{ piece}/\text{cm}^3$ or less was determined as a width of the DZ layer.

[Table 1] to [Table 5] show measurement and evaluation results under various conditions referred to below.

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Brief description of the drawings

Fig. 1 shows a diagram for explaining slips and warpage introduced by RTA heat treatment;

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Fig. 2 shows illustrative diagrams showing a relationship between a BMD size distribution and slip/warpage, illustrating results given in Tables 1-5. **Fig. 2 (A)** illustrates the BMD size distribution claimed in Claim 1 which leads to suppression of both slip and warpage amount to certain minima whereas in all other combinations of BMD size distributions shown in (B) to (D) at least one of slip or warpage amount is undesirably high as illustrated in each of the slip/warpage tables (x means slip/warpage "not OK", O means slip/warpage "good enough").

Fig. 3 shows illustrative diagrams showing a relationship between a prior art BMD size distribution and slip/warpage.

Respective measurement results and evaluation results of annealed wafer and epitaxial wafer

Regarding wafers obtained by the above methods under various conditions (oxygen concentration, nitrogen concentration, hydrogen concentration, cooling time, and heat treatment time), the results of the above-mentioned measurement (1) and evaluation (3) of the wafer obtained the above-mentioned method are shown in Table 1 to Table 5.

BMD size distributions measured regarding annealed wafers that had a wafer diameter of 200mm, each conduction type (p or n), various nitrogen concentrations, hydrogen concentrations, and oxygen concentrations, and that were subjected to various low-temperature heat treatment (temperature, time) and a high-temperature annealing treatment, slips and warpage amounts obtained by evaluation tests were collectively shown in Table 1 as Examples.

BMD size distributions measured regarding annealed wafers that had a wafer diameter of 300mm, each conduction type (p or n), various nitrogen concentrations, hydrogen concentrations, and oxygen concentrations, and that were subjected to various low-temperature

heat treatment (temperature, time) and a high-temperature annealing treatment, slips and warpage amounts obtained by evaluation tests were collectively shown in Table 2 as Examples.

5 BMD size distributions measured regarding epitaxial wafers that had wafer diameters of 200mm and 300mm, each conduction type (p or n), various nitrogen concentrations, hydrogen concentrations, and oxygen concentrations, and that were subjected to a low-temperature heat treatment and a high-temperature annealing treatment and the
10 epitaxial layer is disposed, and the slips and warpage amounts obtained by evaluation tests were collectively shown in Table 3 as Examples.

BMD size distributions measured regarding annealed wafers that had
15 a wafer diameter of 200mm, each conduction type (p or n), various nitrogen concentrations, hydrogen concentrations, and oxygen concentrations, and that were subjected to various low-temperature heat treatments (temperature, time) and a high-temperature annealing treatment, and the slips and warpage amounts obtained by
20 evaluation tests were collectively shown in Table 4 as Examples and Comparative Examples.

(BMD size distributions measured regarding annealed wafers that had a wafer diameter of 300mm, each conduction type (p or n), various
25 nitrogen concentrations, hydrogen concentrations, and oxygen concentrations, and that were subjected to various low-temperature heat treatments (temperature, time) and a high-temperature annealing treatment, slips and warpage amounts obtained by evaluation tests were collectively shown in Table 5 as Examples and
30 Comparative Examples.

Incidentally, all the warpage amounts of wafers before the RTA heat treatment were equal to or less than 10 μ m. The nitrogen concentrations in the annealed wafer and the epitaxial wafer that
35 were added with nitrogen remained unchanged from those measured as

grown.

The BMD density (1) in Tables means the density of BMDs with sizes of 20nm to 40nm, while the BMD density (2) means the density of BMDs with sizes of 300nm or more.

It is understood from Table 1 to Table 3 that, when the annealed wafers and the epitaxial wafers with any diameters, regardless of conduction type of the silicon wafers, satisfy the conditions that the oxygen concentration in each substrate is in a range of 7×10^{17} atoms/cm³ to 9×10^{17} atoms/cm³, the temperature for the low-temperature heat treatment is in a range of 400°C to 850°C, the time for the low-temperature heat treatment is set to 30 minutes to 4 hours, and the cooling rate in a range in which a center temperature of crystal changes from 1000°C to 900°C is set to 5°C/min or more, the BMD density (1) falls in a range of 5×10^{11} /cm³ to 5×10^{13} /cm³, and the BMD density (2) becomes equal to or less than 1×10^7 /cm³. As a result, it is understood that the length of a slip becomes 10mm or less, and a warpage amount is suppressed to 20μm or less.

It is understood that, even if the BMD density (2) is constant, when the nitrogen concentration of the substrate becomes equal to or more than 1×10^{13} atoms/cm³, the warpage is reduced. Especially, it is understood that, when the nitrogen concentration is 1×10^{13} atoms/cm³ or more and the BMD density (2) is 1×10^6 /cm³ or less, all the warpages become equal to or less than 10μm.

It is understood that, even if the oxygen concentration and the heat treatment condition are constant, when the hydrogen concentration becomes equal to or more than 1×10^{12} atoms/cm³ or more, the BMD density (1) becomes high and slips are further shortened. Especially, it is understood that, when the low-temperature heat treatment temperature is equal to or less than 700°C and the heat treatment time is equal to or more than 30 minutes, the BMD density (1) becomes

equal to or more than 1×10^{12} atoms/cm³, and the lengths of slips can be suppressed to 5mm or less.

Incidentally, widths of the DZ layers were equal to or more than 5 μ m in all levels. Especially, when the nitrogen concentration was equal to or more than 1×10^{13} atoms/cm³, or when the oxygen concentration was 7×10^{17} atoms/cm³, the widths of the DZ layers were equal to or more than 7 μ m, which resulted in wider widths.

It is understood from Table 4 and Table 5 that, when the oxygen concentration in the substrate is less than 7×10^{17} atoms/cm³, the BMD density (1) becomes less than 5×10^{11} /cm³. As a result, lengths of slips exceed 10mm.

Incidentally, when the hydrogen gas volume ratio during silicon single crystal growth exceeds 3%, bubble defects occurred, which resulted in incapable evaluation. When the nitrogen concentration in the silicon melt exceeds 1×10^{19} atoms/cm³, multi-crystallization occurs, which results in incapable evaluation.

It is understood that, when the cooling rate in a period in which a center temperature of crystal changes from 1000°C to 900°C is less than 5°C/min, the BMD density (2) exceeds 1×10^7 /cm³, so that the warpage amount exceeds 20 μ m.

When the low-temperature heat treatment is not performed before the high-temperature annealing, when the temperature in the low-temperature heat treatment is less than 400°C or it is more than 850°C, and when the time is less than 30 minutes, the BMD density (1) becomes less than 5×10^{11} /cm³, so that the lengths of slips exceed 10mm.

Incidentally, though not described in Table 5, when the oxygen concentration in the substrate exceeded 9×10^{17} atoms/cm³, the width of the DZ layer was less than 5 μ m. When the oxidized film thickness

of the substrate after annealed exceeded 2nm, or when the temperature in the high-temperature annealing was less than 1100°C and the time was less than 10 minutes, the width of the DZ layer was less than 5µm.

Table 1

Wafer Diameter mm	Conduction Type	Nitrogen Concentration atoms/cm ³	Nitrogen Concentration in Melt atoms/cm ³	Hydrogen Concentration atoms/cm ³	Hydrogen Flow Rate %	Oxygen Concentration atoms/cm ³	Cooling Rate °C/min	Heat Treatment		BMD (atoms/cm ³)		Slip mm	Warpage Amount um
								Low-Temperature Heat Treatment	High-Temperature Annealing	(1)	(2)		
200	P	---	---	---	---	7E+17	5	700°C30min	1200°C1hour	5.9E+11	2.0E+06	6.1	16.9
200	P	---	---	---	---	9E+17	5	700°C4hours	1200°C1hour	3.3E+12	4.6E+06	4.6	16.9
200	P	---	---	---	---	9E+17	7	700°C4hours	1200°C1hour	3.7E+12	5.6E+05	4.6	12.3
200	P	---	---	---	---	9E+17	9	700°C4hours	1200°C1hour	4.3E+12	3.8E+04	4.0	7.0
200	P	1E+13	1E+16	---	---	7E+17	5	700°C4hours	1200°C1hour	7.4E+11	2.7E+06	8.2	11.8
200	P	1E+13	1E+16	---	---	7E+17	7	700°C4hours	1200°C1hour	6.3E+11	4.3E+05	7.3	6.9
200	P	1E+13	1E+16	---	---	9E+17	5	700°C30min	1200°C1hour	6.2E+11	3.6E+06	8.7	11.2
200	P	1E+13	1E+16	---	---	9E+17	5	700°C4hours	1200°C1hour	4.1E+12	7.2E+06	4.0	12.6
200	P	1E+13	1E+16	---	---	9E+17	7	700°C4hours	1200°C1hour	4.9E+12	5.3E+05	4.0	6.5
200	P	1E+15	1E+18	---	---	9E+17	5	700°C4hours	1200°C1hour	4.4E+12	1.1E+04	4.2	6.7
200	P	1E+15	1E+18	---	---	9E+17	7	700°C4hours	1200°C1hour	3.7E+12	5.1E+06	4.8	9.6
200	P	1E+15	1E+18	---	---	9E+17	7	700°C4hours	1200°C1hour	3.2E+12	1.2E+05	4.9	6.5
200	P	---	---	---	---	9E+17	9	700°C4hours	1200°C1hour	4.8E+12	1.1E+04	5.0	6.2
200	P	---	---	1E+16	2.5	7E+17	5	700°C30min	1200°C1hour	2.5E+12	1.0E+06	4.5	16.9
200	P	---	---	1E+16	2.5	7E+17	5	700°C2hours	1200°C1hour	1.3E+13	5.1E+06	2.2	15.2
200	P	---	---	1E+16	2.5	7E+17	5	700°C4hours	1200°C1hour	4.6E+13	4.0E+06	2.4	16.9
200	P	---	---	1E+16	2.5	7E+17	7	700°C4hours	1200°C1hour	4.5E+13	5.1E+05	2.3	13.0
200	P	---	---	1E+16	2.5	9E+17	5	700°C30min	1200°C1hour	2.2E+12	7.5E+06	4.7	15.9
200	P	---	---	1E+16	2.5	9E+17	5	700°C2hours	1200°C1hour	1.0E+13	2.7E+06	3.0	15.7
200	P	---	---	1E+16	2.5	9E+17	5	700°C4hours	1200°C1hour	4.5E+13	7.7E+05	2.9	15.0
200	P	---	---	1E+16	2.5	9E+17	7	700°C4hours	1200°C1hour	4.7E+13	1.7E+05	2.5	12.1
200	P	1E+13	1E+16	---	---	9E+17	9	700°C4hours	1200°C1hour	4.8E+13	1.9E+04	2.7	8.4
200	P	1E+13	1E+16	---	---	7E+17	5	700°C30min	1200°C1hour	2.0E+12	4.9E+06	4.7	12.4
200	P	1E+13	1E+16	---	---	7E+17	5	700°C2hours	1200°C1hour	1.4E+13	3.8E+06	2.4	12.6
200	P	1E+13	1E+16	---	---	7E+17	5	700°C4hours	1200°C1hour	4.8E+13	6.3E+06	2.2	11.6
200	P	1E+13	1E+16	---	---	7E+17	9	700°C4hours	1200°C1hour	4.8E+13	8.8E+03	2.0	6.4
200	P	1E+13	1E+16	---	---	9E+17	5	700°C30min	1200°C1hour	2.1E+12	5.4E+06	4.3	12.3
200	P	1E+13	1E+16	---	---	9E+17	5	700°C2hours	1200°C1hour	1.1E+13	3.5E+06	2.5	12.7
200	P	1E+13	1E+16	---	---	9E+17	5	700°C4hours	1200°C1hour	4.8E+13	3.0E+06	3.0	12.4
200	P	1E+13	1E+16	---	---	9E+17	7	700°C4hours	1200°C1hour	4.7E+13	2.8E+05	2.0	6.4
200	P	4E+15	4E+18	---	---	9E+17	9	700°C4hours	1200°C1hour	4.6E+13	3.9E+04	2.9	6.2
200	P	4E+15	4E+18	---	---	9E+17	5	700°C30min	1200°C1hour	2.5E+12	5.1E+06	4.5	9.8
200	P	4E+15	4E+18	---	---	9E+17	5	700°C2hours	1200°C1hour	1.3E+13	6.3E+06	2.1	9.3
200	P	4E+15	4E+18	---	---	9E+17	5	700°C4hours	1200°C1hour	4.8E+13	6.5E+06	2.7	8.2
200	P	4E+15	4E+18	---	---	9E+17	7	700°C4hours	1200°C1hour	4.8E+13	1.5E+05	3.0	6.3
200	P	4E+15	4E+18	---	---	9E+17	9	700°C4hours	1200°C1hour	4.8E+13	2.2E+04	2.4	6.9
200	P	4E+15	4E+18	---	---	9E+17	5	850°C30min	1200°C1hour	5.4E+11	5.5E+06	8.7	8.1
200	P	4E+15	4E+18	---	---	9E+17	5	850°C4hours	1200°C1hour	1.5E+12	7.8E+06	4.7	9.1
200	P	4E+15	4E+18	---	---	9E+17	5	400°C30min	1200°C1hour	1.3E+12	5.9E+06	4.2	8.5
200	P	4E+15	4E+18	---	---	9E+17	5	400°C4hours	1200°C1hour	2.3E+13	6.6E+06	2.4	8.4
200	n	---	---	---	---	9E+17	5	700°C4hours	1200°C1hour	4.0E+12	8.0E+06	4.7	16.6
200	n	1E+15	1E+18	---	---	9E+17	5	700°C4hours	1200°C1hour	3.5E+12	2.9E+06	4.9	9.7
200	n	---	---	---	---	9E+17	5	700°C4hours	1200°C1hour	4.8E+13	1.3E+08	2.8	16.2
200	n	4E+15	4E+18	---	---	9E+17	5	700°C4hours	1200°C1hour	4.7E+13	3.5E+06	3.0	8.2

Table 2

Wafer Diameter mm	Conduction Type	Nitrogen Concentration atoms/cm ³	Nitrogen Concentration in Melt atoms/cm ³	Hydrogen Concentration atoms/cm ³	Hydrogen Flow Rate %	Oxygen Concentration atoms/cm ³	Cooling Rate °C/min	Heat Treatment		BMD (atoms/cm ³)		Slip mm	Warpage Amount um
								Low-Temperature Heat Treatment	High-Temperature Annealing	(1)	(2)		
300	p	---	---	---	---	7E+17	5	700°C30min	1200°C2hours	5.9E+11	3.0E+06	8.6	16.0
300	p	---	---	---	---	9E+17	5	700°C4hours	1200°C2hours	4.5E+12	3.0E+06	4.4	15.4
300	p	---	---	---	---	9E+17	7	700°C4hours	1200°C2hours	3.8E+12	3.1E+05	4.1	13.4
300	p	1E+13	1E+16	---	---	7E+17	5	700°C4hours	1200°C2hours	8.4E+11	2.6E+06	7.5	12.5
300	p	1E+13	1E+16	---	---	7E+17	7	700°C4hours	1200°C2hours	8.6E+11	2.4E+05	8.3	6.5
300	p	1E+13	1E+16	---	---	9E+17	5	700°C30min	1200°C2hours	6.0E+11	7.3E+06	6.1	11.8
300	p	1E+13	1E+16	---	---	9E+17	5	700°C4hours	1200°C2hours	4.8E+12	6.1E+06	4.7	12.6
300	p	1E+13	1E+16	---	---	9E+17	7	700°C4hours	1200°C2hours	4.8E+12	2.1E+05	4.0	6.9
300	p	1E+15	1E+18	---	---	9E+17	5	700°C4hours	1200°C2hours	4.0E+12	4.4E+06	4.3	9.9
300	p	1E+15	1E+18	---	---	9E+17	7	700°C4hours	1200°C2hours	3.5E+12	5.4E+05	4.2	6.6
300	p	---	---	1E+16	2.5	7E+17	5	700°C30min	1200°C2hours	2.5E+12	4.8E+06	4.4	15.5
300	p	---	---	1E+16	2.5	7E+17	5	700°C2hours	1200°C2hours	1.5E+13	6.0E+06	2.7	16.2
300	p	---	---	1E+16	2.5	7E+17	5	700°C4hours	1200°C2hours	5.0E+13	1.7E+06	2.7	16.7
300	p	---	---	1E+16	2.5	7E+17	7	700°C4hours	1200°C2hours	4.8E+13	1.0E+05	2.4	12.4
300	p	---	---	1E+16	2.5	9E+17	5	700°C30min	1200°C2hours	2.3E+12	3.9E+06	4.3	15.7
300	p	---	---	1E+16	2.5	9E+17	5	700°C2hours	1200°C2hours	1.1E+13	7.0E+06	2.4	15.7
300	p	---	---	1E+16	2.5	9E+17	5	700°C4hours	1200°C2hours	5.0E+13	1.2E+06	2.1	16.8
300	p	---	---	1E+16	2.5	9E+17	7	700°C4hours	1200°C2hours	4.9E+13	5.5E+05	2.2	12.8
300	p	1E+13	1E+16	1E+16	2.5	7E+17	5	700°C30min	1200°C2hours	2.2E+12	1.9E+06	4.4	12.3
300	p	1E+13	1E+16	1E+16	2.5	7E+17	5	700°C2hours	1200°C2hours	1.4E+13	3.3E+06	2.1	11.9
300	p	1E+13	1E+16	1E+16	2.5	7E+17	5	700°C4hours	1200°C2hours	4.5E+13	9.5E+05	2.8	12.5
300	p	1E+13	1E+16	1E+16	2.5	9E+17	5	700°C30min	1200°C2hours	2.3E+12	7.2E+06	4.7	12.9
300	p	1E+13	1E+16	1E+16	2.5	9E+17	5	700°C2hours	1200°C2hours	1.2E+13	4.4E+06	2.3	12.2
300	p	1E+13	1E+16	1E+16	2.5	9E+17	5	700°C4hours	1200°C2hours	4.6E+13	3.2E+06	2.2	12.7
300	p	1E+13	1E+16	1E+16	2.5	9E+17	7	700°C4hours	1200°C2hours	4.8E+13	4.7E+05	2.0	6.6
300	p	4E+15	4E+18	1E+16	2.5	9E+17	5	700°C30min	1200°C2hours	2.3E+12	7.1E+06	4.6	8.4
300	p	4E+15	4E+18	1E+16	2.5	9E+17	5	700°C2hours	1200°C2hours	1.2E+13	7.1E+06	2.7	9.0
300	p	4E+15	4E+18	1E+16	2.5	9E+17	5	700°C4hours	1200°C2hours	4.6E+13	3.8E+06	2.9	9.2
300	p	4E+15	4E+18	1E+16	2.5	9E+17	7	700°C4hours	1200°C2hours	4.6E+13	4.5E+05	2.2	6.3
300	n	---	---	---	---	9E+17	5	700°C4hours	1200°C2hours	3.1E+12	6.5E+06	4.7	15.1
300	n	1E+15	1E+18	---	---	9E+17	5	700°C4hours	1200°C2hours	3.3E+12	2.2E+06	5.0	9.9
300	n	---	---	1E+16	2.5	9E+17	5	700°C4hours	1200°C2hours	4.5E+13	5.4E+06	2.1	15.5
300	n	4E+15	4E+18	1E+16	2.5	9E+17	5	700°C4hours	1200°C2hours	4.8E+13	1.8E+06	2.8	9.4

Table 3

Wafer Diameter	mm	Conduction Type	Nitrogen Concentration atoms/cm ³	Nitrogen Concentration in Melt atoms/cm ³	Hydrogen Concentration atoms/cm ³	Hydrogen Flow Rate %	Oxygen Concentration atoms/cm ³	Cooling Rate °C/min	Heat Treatment		BMD (atoms/cm ³)		Slip mm	Warpage Amount um
									Low-Temperature Heat Treatment	High-Temperature Annealing	(1)	(2)		
200	p	---	---	---	---	---	9E+17	5	700°C4hours	1200°C1hour	3.2E+12	5.7E+06	4.3	16.4
200	p	1E+15	1E+18	---	---	---	9E+17	5	700°C4hours	1200°C1hour	3.5E+12	4.0E+06	4.2	9.2
200	p	---	---	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C1hour	4.9E+13	7.5E+06	2.8	16.4
200	p	4E+15	4E+18	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C1hour	4.6E+13	3.5E+06	2.2	8.8
200	n	---	---	---	---	---	9E+17	5	700°C4hours	1200°C1hour	4.9E+12	5.3E+06	4.2	16.2
200	n	1E+15	1E+18	---	---	---	9E+17	5	700°C4hours	1200°C1hour	5.0E+12	3.3E+06	4.9	8.2
200	n	---	---	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C1hour	4.9E+13	2.7E+06	2.6	15.8
200	n	4E+15	4E+18	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C1hour	4.8E+13	3.5E+06	2.5	9.2
300	p	---	---	---	---	---	9E+17	5	700°C4hours	1200°C2hours	3.6E+12	2.8E+06	4.7	15.3
300	p	1E+15	1E+18	---	---	---	9E+17	5	700°C4hours	1200°C2hours	4.1E+12	5.1E+06	4.7	8.8
300	p	---	---	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C2hours	4.7E+13	9.9E+05	2.1	16.0
300	p	4E+15	4E+18	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C2hours	4.8E+13	9.9E+05	2.4	9.8
300	n	---	---	---	---	---	9E+17	5	700°C4hours	1200°C2hours	3.1E+12	1.4E+06	4.0	15.4
300	n	1E+15	1E+18	1E+16	---	---	9E+17	5	700°C4hours	1200°C2hours	3.0E+12	1.9E+06	4.6	9.3
300	n	---	---	---	---	2.5	9E+17	5	700°C4hours	1200°C2hours	4.9E+13	4.2E+06	2.5	16.6
300	n	4E+15	4E+18	1E+16	---	2.5	9E+17	5	700°C4hours	1200°C2hours	4.7E+13	6.5E+06	3.0	10.0

Table 4

Wafer Diameter	Conduction Type	Nitrogen Concentration atoms/cm ³	Nitrogen Concentration in Melt atoms/cm ³	Hydrogen Concentration atoms/cm ³	Hydrogen Flow Rate %	Oxygen Concentration atoms/cm ³	Cooling Rate °C/min	Heat Treatment		BMD (atoms/cm ³)		Slip mm	Warpage Amount um
								Low-Temperature Heat Treatment	High-Temperature Annealing	(1)	(2)		
200	p	---	---	---	---	6E+17	4	700°C4hours	1200°C1hour	7.1E+07	2.0E+07	14.8	27.0
200	p	---	---	---	---	6E+17	5	700°C4hours	1200°C1hour	3.0E+07	1.9E+06	16.6	14.4
200	p	---	---	---	---	9E+17	4	700°C4hours	1200°C1hour	3.7E+12	2.4E+07	4.2	29.5
200	p	---	---	---	---	9E+17	7	700°C10min	1200°C1hour	5.7E+10	2.9E+05	16.5	13.5
200	p	1E+15	1E+18	---	---	6E+17	4	700°C4hours	1200°C1hour	3.0E+07	2.3E+07	15.2	21.2
200	p	1E+15	1E+18	---	---	6E+17	5	700°C4hours	1200°C1hour	9.2E+07	2.4E+06	15.8	7.1
200	p	1E+15	1E+18	---	---	9E+17	4	700°C4hours	1200°C1hour	3.3E+12	1.5E+07	4.4	22.5
200	p	1E+15	1E+18	---	---	9E+17	7	700°C10min	1200°C1hour	3.7E+10	2.2E+05	15.2	6.7
200	p	---	---	1E+16	2.5	9E+17	4	---	1200°C1hour	5.4E+08	1.2E+07	15.1	28.7
200	p	---	---	1E+16	2.5	9E+17	4	700°C10min	1200°C1hour	2.8E+10	1.8E+07	15.4	27.1
200	p	---	---	1E+16	2.5	9E+17	4	700°C4hours	1200°C1hour	4.5E+13	1.7E+07	2.8	25.6
200	p	---	---	1E+16	2.5	9E+17	7	---	1200°C1hour	4.4E+09	6.0E+05	14.3	12.4
200	p	---	---	1E+16	2.5	9E+17	7	700°C10min	1200°C1hour	2.3E+09	6.5E+05	15.4	12.7
200	p	---	---	1E+16	2.5	9E+17	7	350°C4hours	1200°C1hour	4.6E+08	4.4E+05	16.4	13.3
200	p	---	---	1E+16	2.5	9E+17	7	900°C4hours	1200°C1hour	4.8E+08	6.6E+05	17.0	12.6
200	p	1E+15	1E+18	---	---	9E+17	4	700°C4hours	1200°C1hour	4.9E+13	2.5E+07	2.1	21.1
200	p	1E+15	1E+18	---	---	9E+17	7	---	1200°C1hour	4.4E+09	1.6E+05	15.2	6.6
200	p	1E+15	1E+18	---	---	9E+17	7	700°C10min	1200°C1hour	5.4E+10	5.9E+05	15.7	6.6
200	p	1E+15	1E+18	---	---	9E+17	7	350°C4hours	1200°C1hour	4.5E+09	9.4E+04	14.4	6.6
200	p	1E+15	1E+18	---	---	9E+17	7	900°C4hours	1200°C1hour	8.6E+09	5.8E+05	15.8	6.9
200	p	---	---	Incapable Measurement	3.5	Incapable Measurement	5	Incapable Evaluation					
200	p	Incapable Measurement	5E+18	---	---	Incapable Measurement	5	Incapable Evaluation					

Table 5

Wafer Diameter	Conduction Type	Nitrogen Concentration atoms/cm3	Nitrogen Concentration in Melt atoms/cm3	Hydrogen Concentration atoms/cm3	Hydrogen Flow Rate %	Oxygen Concentration atoms/cm3	Cooling Rate °C/min	Heat Treatment		BMD (atoms/cm3)		Slip mm	Warpage Amount um
								Low-Temperature Heat Treatment	High-Temperature Annealing	(1)	(2)		
mm													
300	p	---	---	---	---	6E+17	4	700°C4hours	1200°C2hours	2.8E+07	1.5E+07	14.6	26.2
300	p	---	---	---	---	6E+17	5	700°C4hours	1200°C2hours	2.0E+07	2.2E+06	15.3	15.4
300	p	---	---	---	---	9E+17	4	700°C4hours	1200°C2hours	4.6E+12	1.1E+07	4.5	27.7
300	p	---	---	---	---	9E+17	7	700°C10min	1200°C2hours	4.2E+10	7.9E+05	14.4	13.6
300	p	1E+15	1E+18	---	---	6E+17	4	700°C4hours	1200°C2hours	3.7E+07	2.3E+07	14.7	21.3
300	p	1E+15	1E+18	---	---	6E+17	5	700°C4hours	1200°C2hours	4.7E+07	3.5E+06	16.5	7.3
300	p	1E+15	1E+18	---	---	9E+17	4	700°C4hours	1200°C2hours	3.3E+12	2.5E+07	4.6	24.0
300	p	1E+15	1E+18	---	---	9E+17	7	700°C10min	1200°C2hours	7.2E+10	2.7E+05	16.3	6.7
300	p	---	---	1E+16	2.5	9E+17	4	---	1200°C2hours	5.2E+08	2.1E+07	16.2	29.4
300	p	---	---	1E+16	2.5	9E+17	4	700°C10min	1200°C2hours	2.3E+10	2.0E+07	15.5	26.7
300	p	---	---	1E+16	2.5	9E+17	4	700°C4hours	1200°C2hours	6.5E+12	2.6E+07	4.7	28.7
300	p	---	---	1E+16	2.5	9E+17	7	---	1200°C2hours	8.3E+09	3.6E+05	15.2	12.6
300	p	---	---	1E+16	2.5	9E+17	7	700°C10min	1200°C2hours	1.8E+09	5.4E+05	14.5	12.9
300	p	---	---	1E+16	2.5	9E+17	7	350°C4hours	1200°C2hours	6.1E+08	1.3E+05	14.8	13.0
300	p	---	---	1E+16	2.5	9E+17	7	900°C4hours	1200°C2hours	3.3E+08	6.7E+05	14.4	13.6
300	p	1E+15	1E+18	1E+16	2.5	9E+17	4	700°C4hours	1200°C2hours	5.0E+13	2.3E+07	2.3	22.8
300	p	1E+15	1E+18	1E+16	2.5	9E+17	7	---	1200°C2hours	7.2E+09	3.4E+05	14.5	6.3
300	p	1E+15	1E+18	1E+16	2.5	9E+17	7	700°C10min	1200°C2hours	7.4E+10	2.0E+05	14.7	6.5
300	p	1E+15	1E+18	1E+16	2.5	9E+17	7	350°C4hours	1200°C2hours	1.2E+09	4.8E+05	16.2	6.8
300	p	1E+15	1E+18	1E+16	2.5	9E+17	7	900°C4hours	1200°C2hours	4.7E+09	2.6E+05	14.5	6.1
300	p	---	---	Incapable Measurement	3.5	Incapable Measurement	5	Incapable Evaluation					
300	p	Incapable Measurement	5E+18	---	---	Incapable Measurement	5	Incapable Evaluation					

Claims

1. A silicon wafer having, at a position 20 μm or more from a wafer surface, a density of bulk micro defects with sizes of 20nm to 40nm in the range of $5 \times 10^{11}/\text{cm}^3$ to $5 \times 10^{13}/\text{cm}^3$, and having a density of BMDs with sizes of 300nm or more equal to or less than $1 \times 10^7/\text{cm}^3$.

2. The silicon wafer according to claim 1, which is doped with nitrogen.

3. The silicon wafer according to claim 1 or 2, which is doped with hydrogen.

4. A method for manufacturing a silicon wafer according to any of claims 1 to 3, comprising growing a silicon single crystal ingot while maintaining a cooling rate in a range in which a center temperature of the crystal during crystal growth changes from 1000°C to 900°C at a rate of $5^\circ\text{C}/\text{min}$ or more; heat treating a wafer sliced from the ingot at a temperature of 400°C to 850°C for 30 minutes to 4 hours; high temperature annealing by heat treating the wafer at a temperature of 1100°C to 1250°C for 10 minutes to 2 hours under an atmosphere of rare gas having an impurity concentration of 0.5% or less by volume or under a non-oxidizing atmosphere, wherein the thickness of any oxidized film after heat treating is 2nm or less.

5. The method according to claim 4, wherein the oxygen concentration of the wafer immediately after being sliced from the crystal is in the range of 7×10^{17} atoms/ cm^3 to 9×10^{17} atoms/ cm^3 .

6. The method according to claim 4 or 5, wherein the nitrogen concentration of the wafer immediately after being sliced from a crystal is in a range of 1×10^{13} atoms/ cm^3 to 8×10^{15} atoms/ cm^3 .

7. The method according to claim 6, wherein the growth of the silicon single crystal ingot is performed from a melt to which nitrogen is added such that the nitrogen concentration falls in a range of 1×10^{16} atoms/cm³ to 1×10^{19} atoms/cm³.

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8. The method according to any of claims 4 to 7, wherein the hydrogen concentration of the wafer immediately after being sliced from a crystal is in a range of 1×10^{12} atoms/cm³ to 5×10^{16} atoms/cm³.

10 9. The method according to claim 8, wherein the growth of the silicon single crystal ingot is performed under an atmosphere where hydrogen gas is continuously introduced such that the concentration of hydrogen is within the range of 0.01% to 3% at a volume ratio.

15 10. The method according to any of claims 4 to 9, wherein in a further step, a silicon single crystal epi-layer is epitaxially deposited after the high-temperature anneal.