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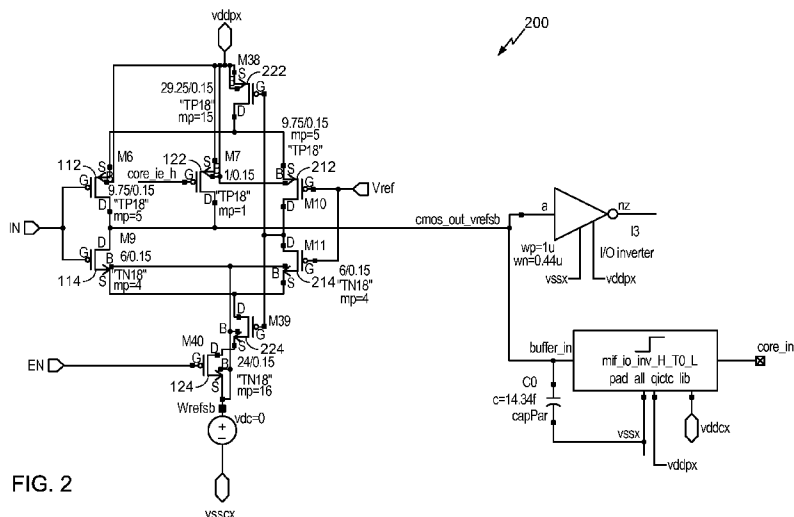
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(54) Title: ADJUSTABLE INPUT RECEIVER FOR LOW POWER HIGH SPEED INTERFACE



(S7) Abstract: A pseudo-differential input receiver is disclosed which is configured to support a wide-range of reference voltage V_{ref} and a wide-range frequency interface with no parallel termination are described herein. The pseudo-differential receiver implementations described herein are very efficient in terms of area, power, and performance. A wide-frequency-range V_{ref} -adjustable input receiver is described herein. The receiver can be configured with a V_{ref} -monitoring PMOS helper FET or an enabled stacked PMOS helper FET to enable the receiver to work at $V_{ref}=0V$ like a conventional CMOS receiver. The receiver can also be configured with a V_{ref} -monitoring NMOS helper FET to enable a V_{ref} -based input receiver to work with programmability on bias currents & trip-point at $V_{ref}=(0.5\sim 0.7)V_{dd}$, depending on the ratio of output driver's impedance and parallel on/off-die termination impedance.