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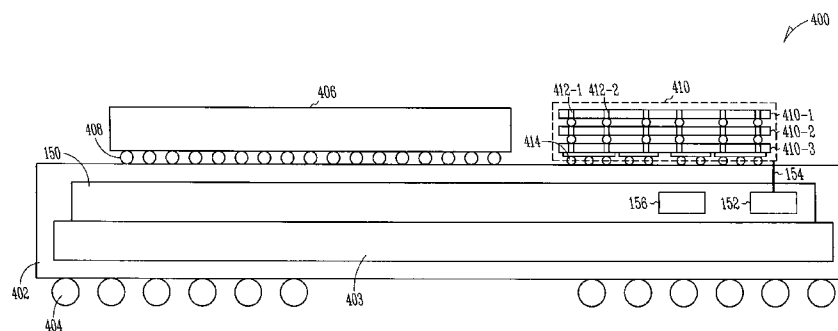


FIG. 4

(57) Abstract: Apparatus and systems may include a substrate, an interface chip disposed on the substrate, a first memory die having a plurality of memory arrays disposed on the interface chip, the first memory die coupled to a plurality of through wafer interconnects (TWI), and a second memory die having a plurality of memory arrays disposed on the first memory die, the second memory die including a plurality of vias, wherein the plurality of vias are configured to allow the plurality of TWI to pass through the second memory die. The second memory die may be coupled to a second plurality of TWI. In this way, the interface chip may be used to communicatively couple the first memory die and the second memory die using the first and second plurality of TWI. Other apparatus, systems, and methods are disclosed.