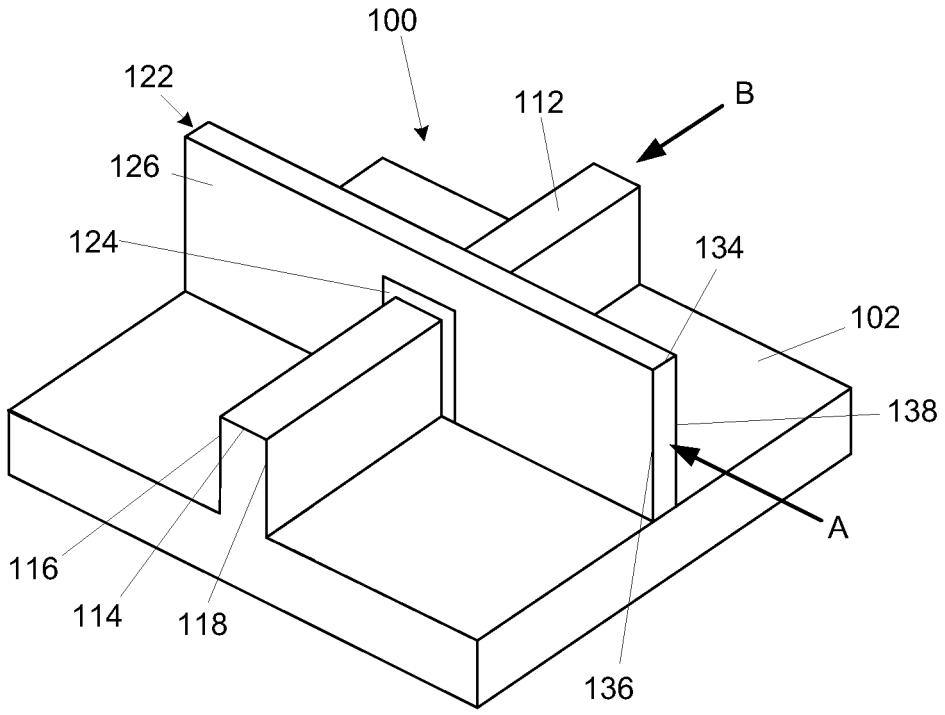

100
122
112
B
126
124
134
102
138
A
116
114
118
136

FIG. 1

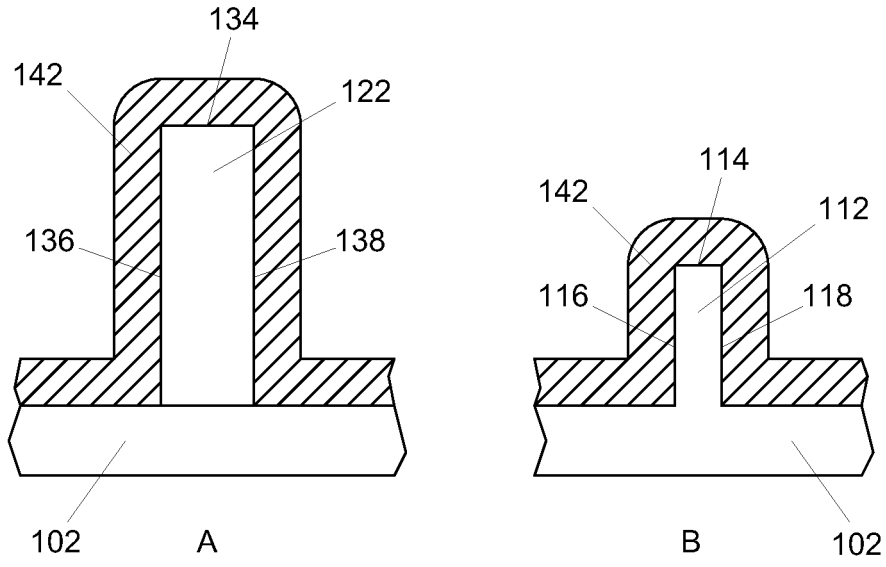

134
142
122
136
138
102
A
114
142
112
116
118
B
102

FIG. 2

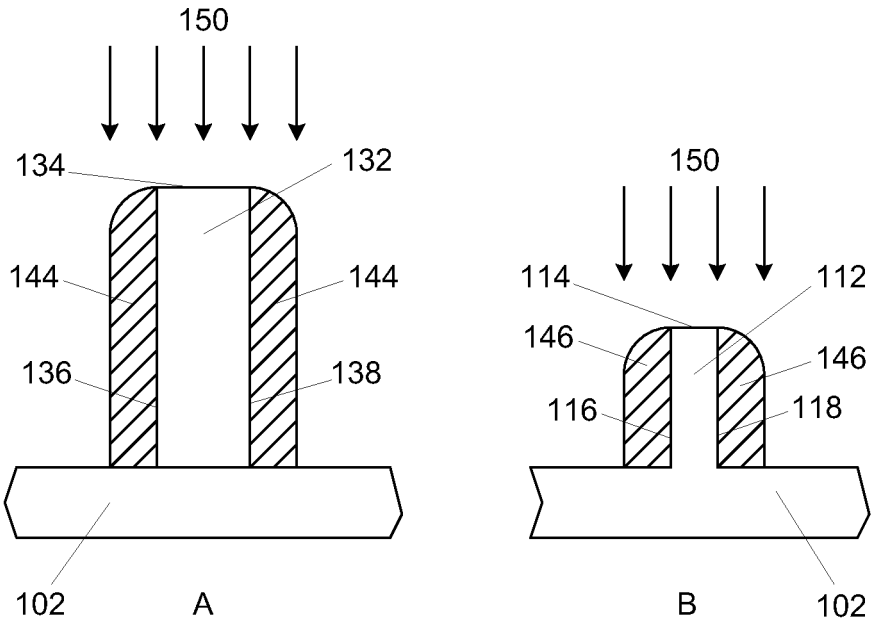

150
134
132
144
144
136
138
102
A
150
114
112
146
146
116
118
B
102

FIG. 3

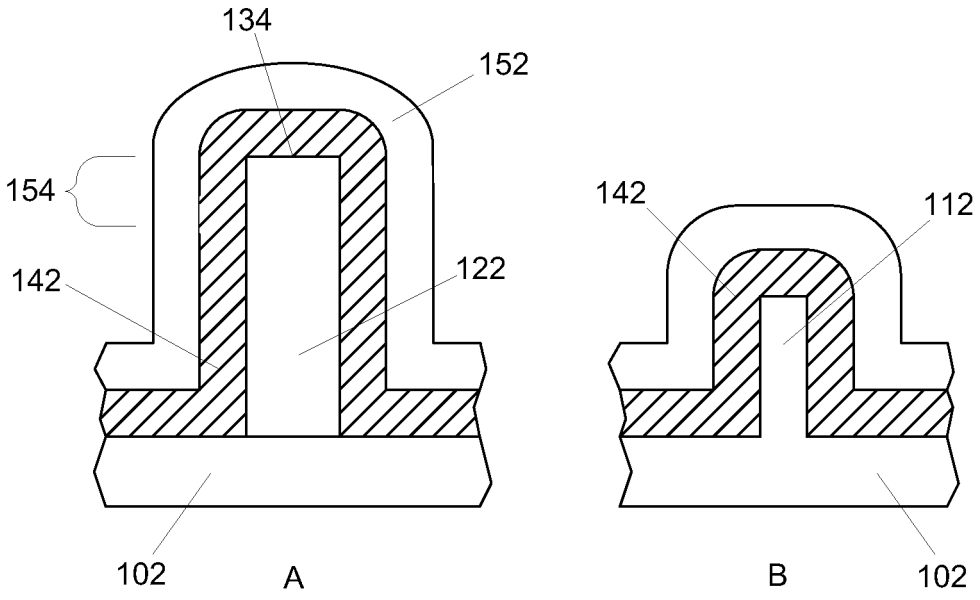

134
152
154
142
122
102
A
142
112
B
102

FIG. 4

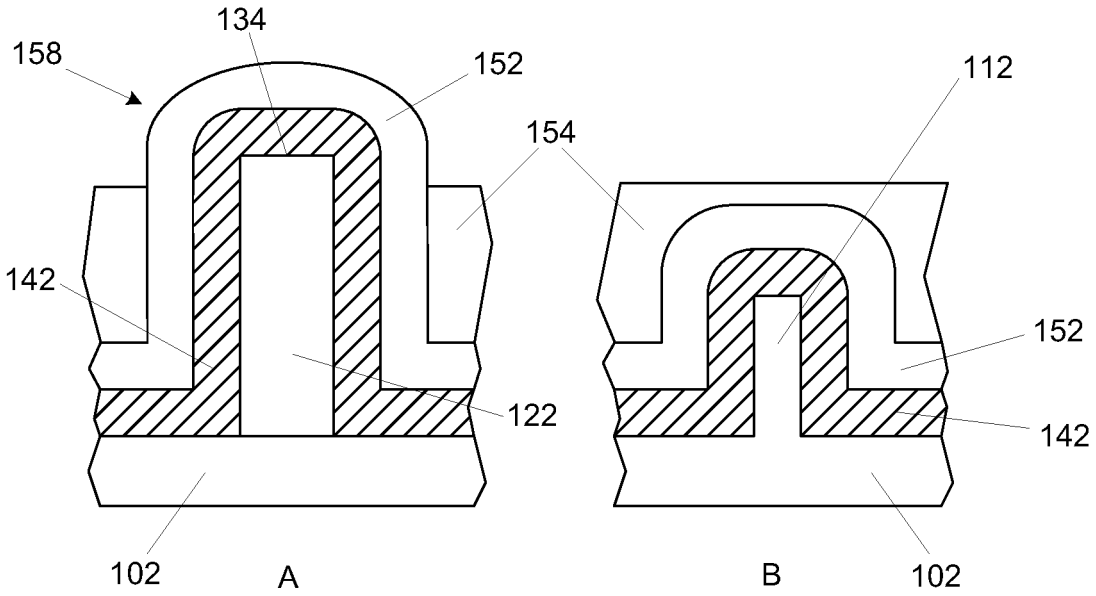

158
134
152
154
112
142
152
122
142
102
A
B
102

FIG. 5

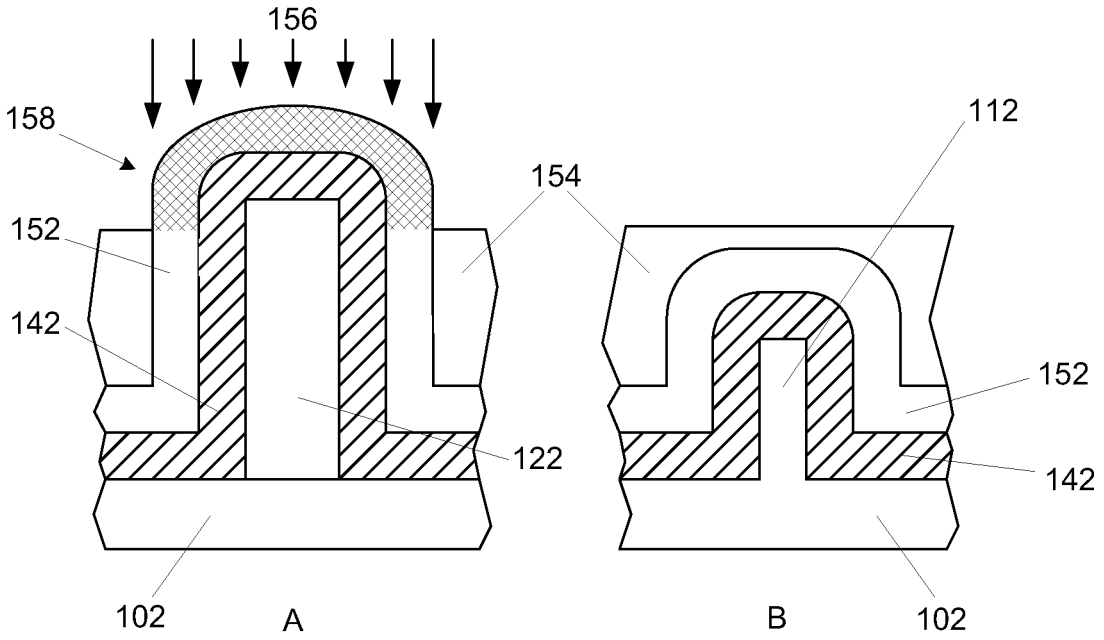

156
158
112
154
152
142
152
122
142
102
A
B
102

FIG. 6

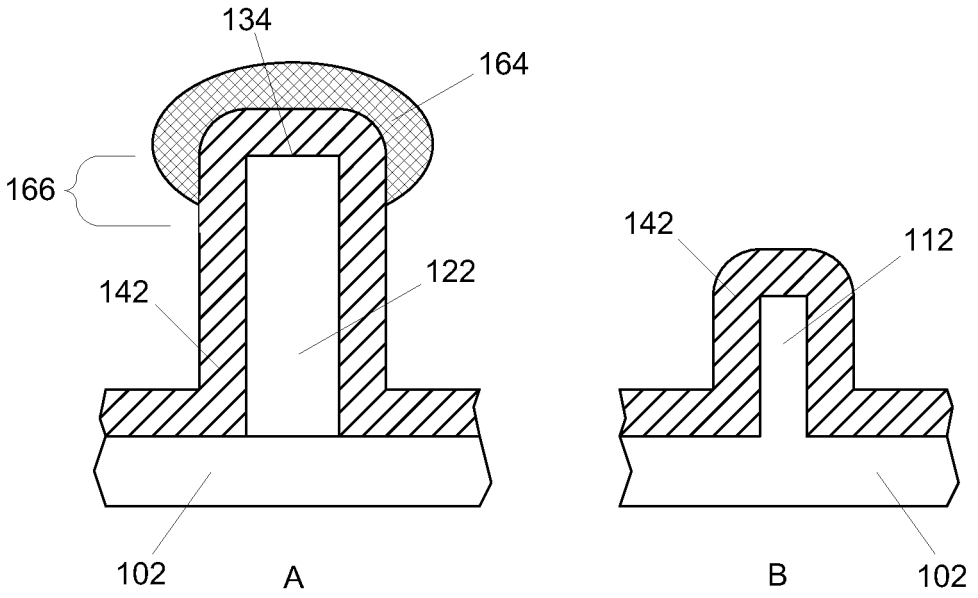

134
164
166
142
122
102
A
142
112
B
102

FIG. 7

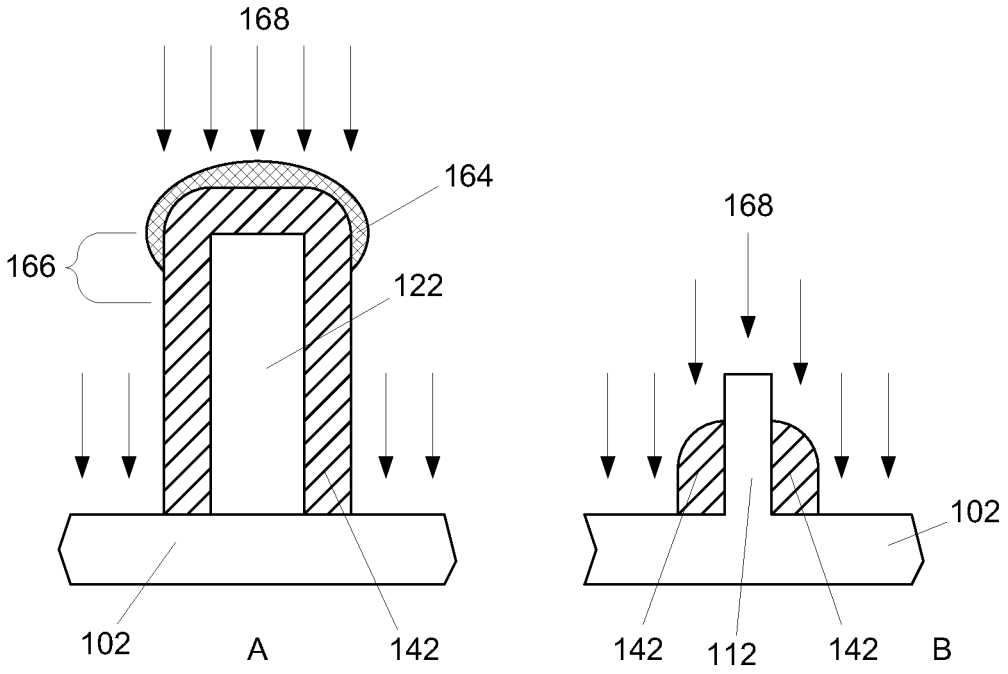

168
164
166
122
102
A
142
168
102
142
112
142
B

FIG. 8

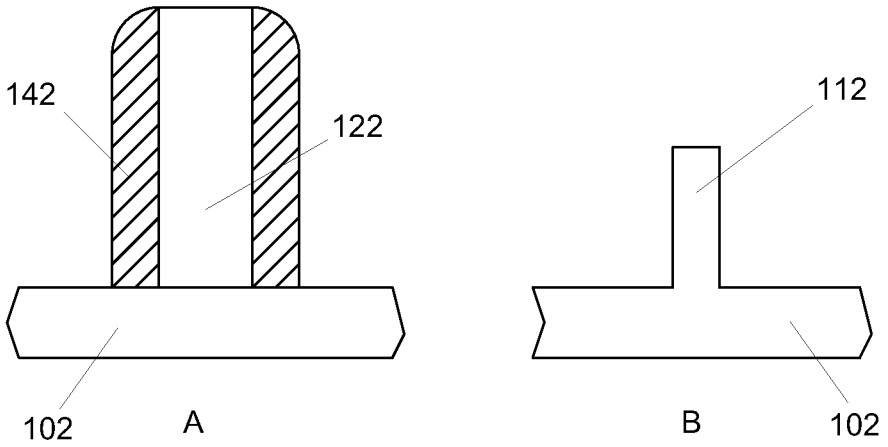


FIG. 9

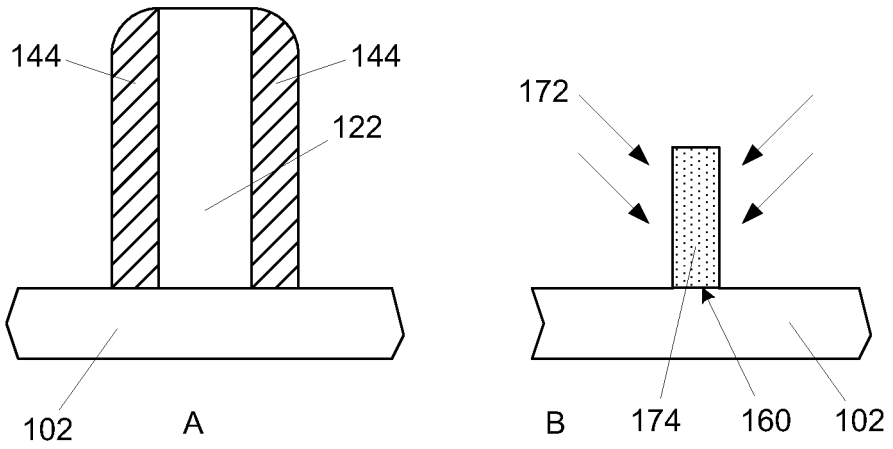


FIG. 10

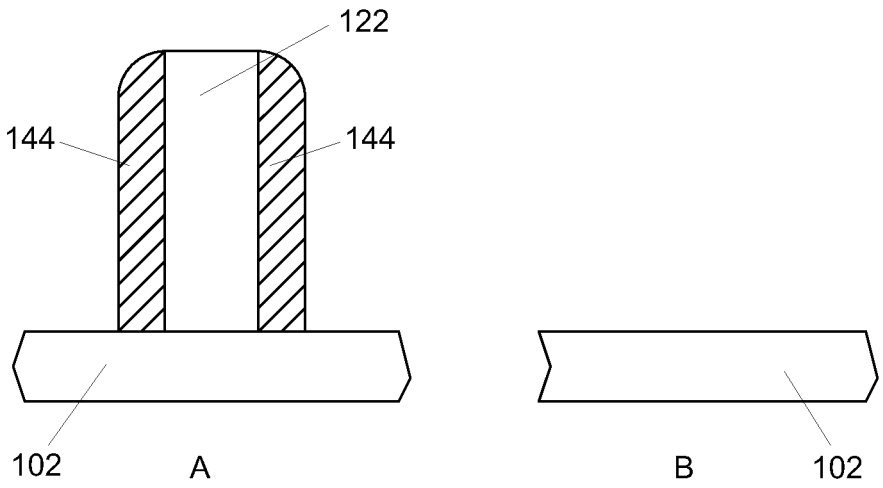


FIG. 11

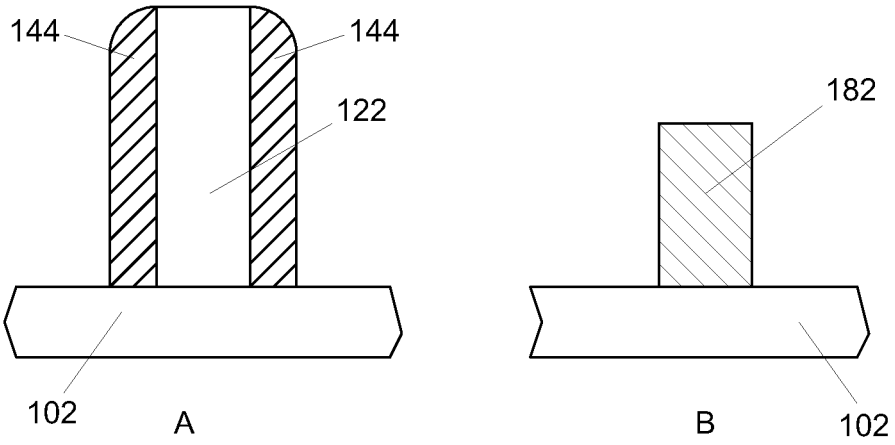


FIG. 12

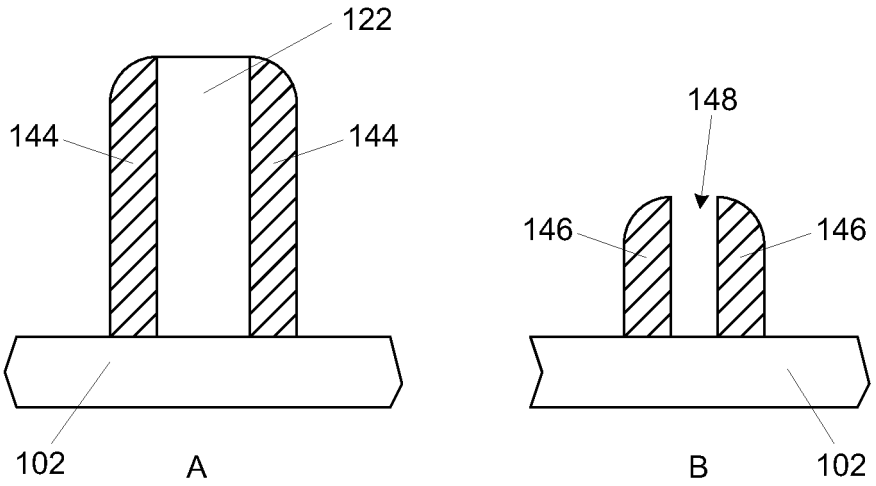

122
144
144
102
A
148
146
146
B
102

FIG. 13

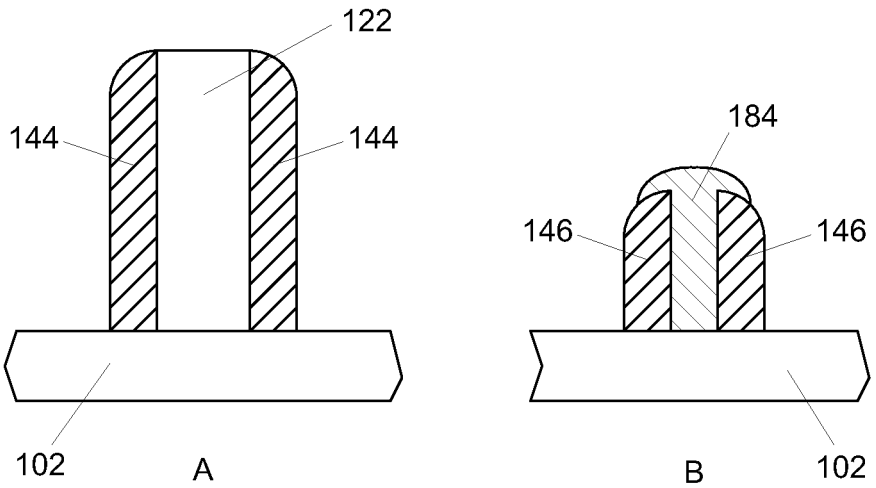

122
144
144
102
A
184
146
146
B
102

FIG. 14

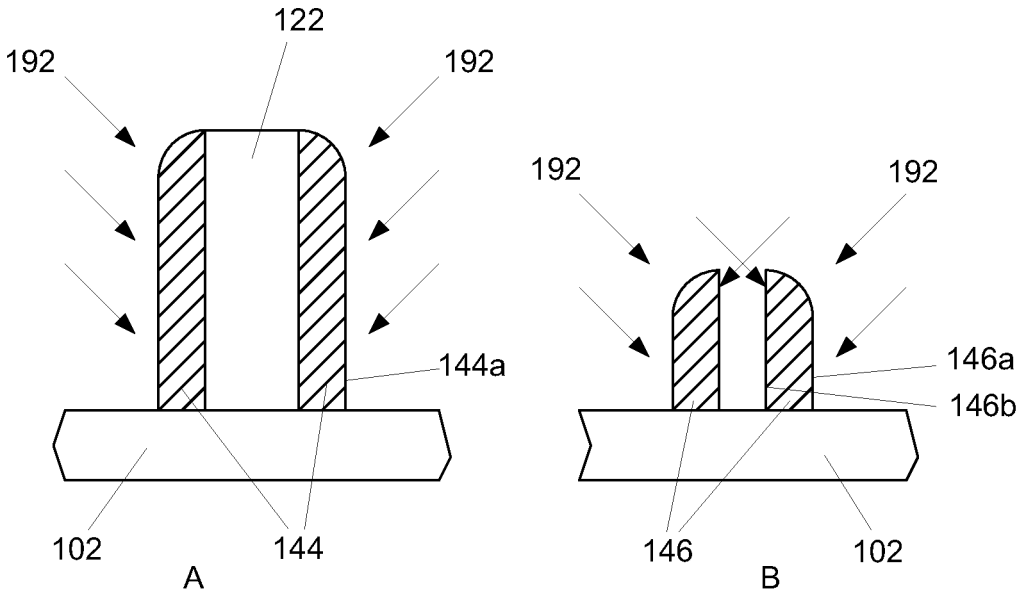

122
192
192
144a
102
144
A
192
192
146a
146b
146
102
B

FIG. 15

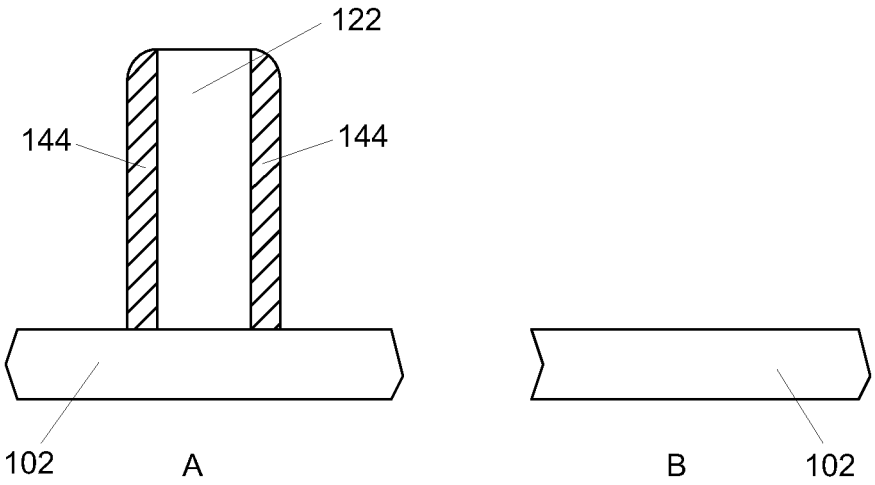

122
144
144
102
A
B
102

FIG. 16

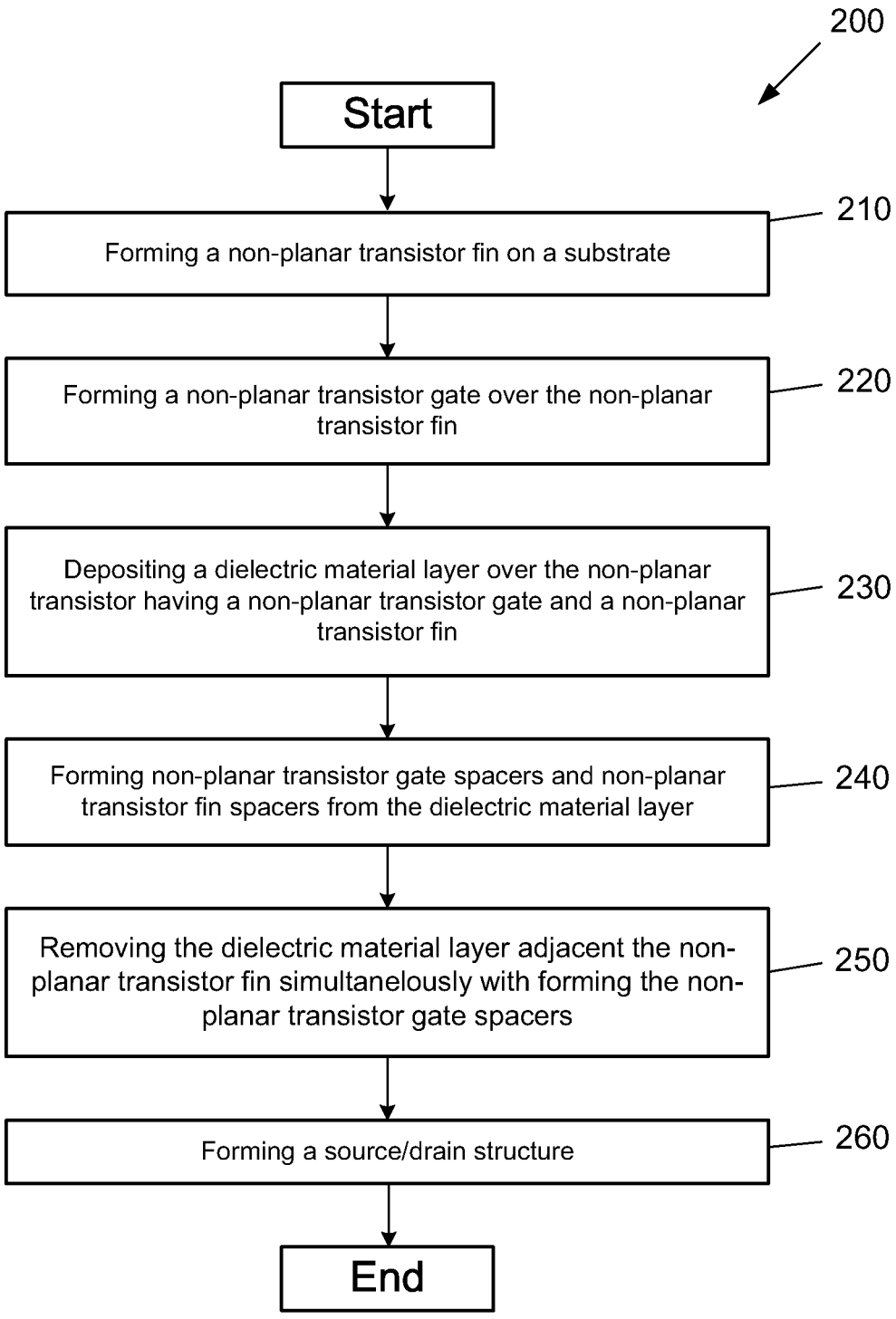

200
Start
Forming a non-planar transistor fin on a substrate
210
Forming a non-planar transistor gate over the non-planar transistor fin
220
Depositing a dielectric material layer over the non-planar transistor having a non-planar transistor gate and a non-planar transistor fin
230
Forming non-planar transistor gate spacers and non-planar transistor fin spacers from the dielectric material layer
240
Removing the dielectric material layer adjacent the non-planar transistor fin simultanelously with forming the non-planar transistor gate spacers
250
Forming a source/drain structure
260
End

FIG. 17

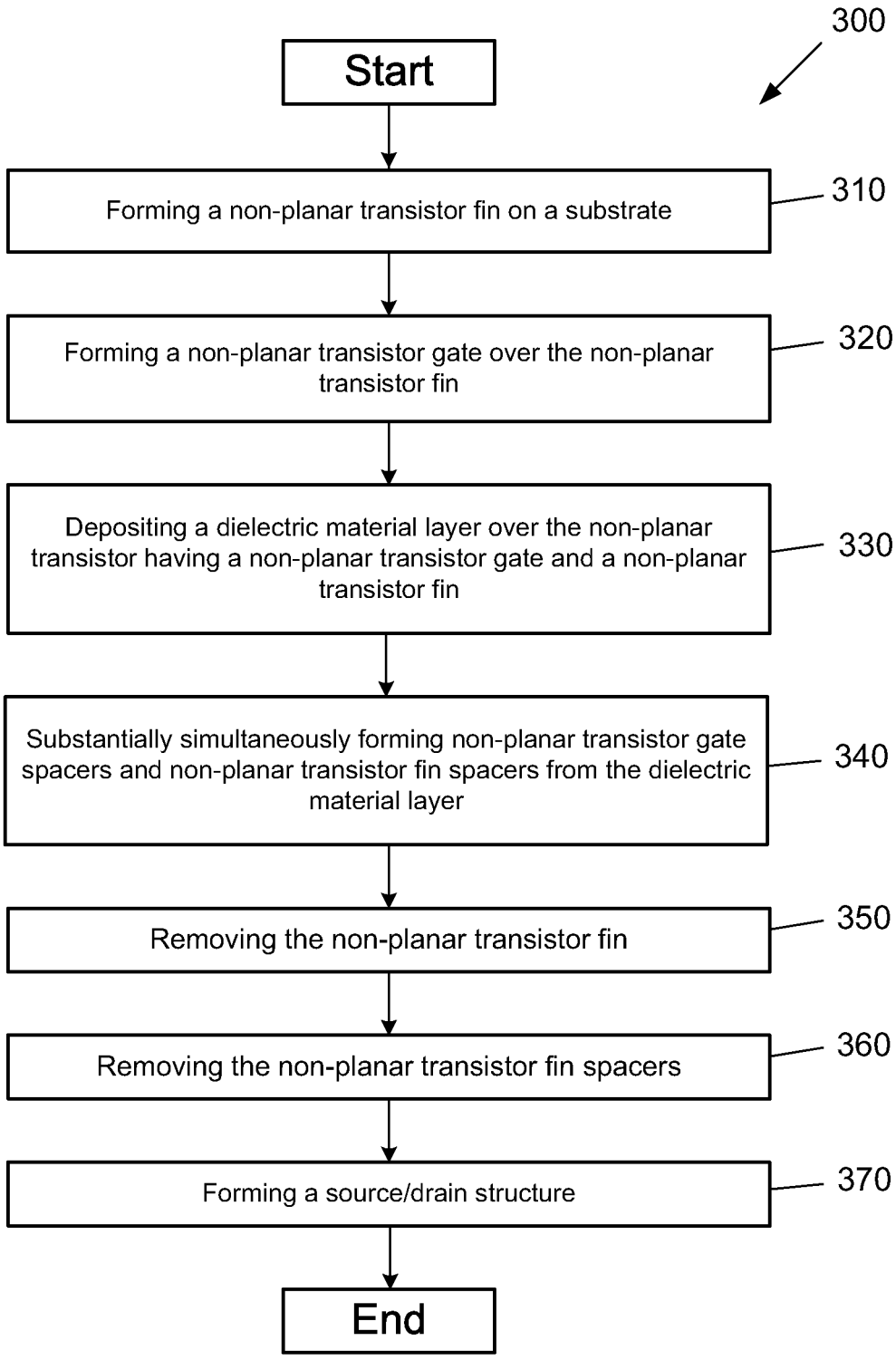

300
Start
Forming a non-planar transistor fin on a substrate
310
Forming a non-planar transistor gate over the non-planar transistor fin
320
Depositing a dielectric material layer over the non-planar transistor having a non-planar transistor gate and a non-planar transistor fin
330
Substantially simultaneously forming non-planar transistor gate spacers and non-planar transistor fin spacers from the dielectric material layer
340
Removing the non-planar transistor fin
350
Removing the non-planar transistor fin spacers
360
Forming a source/drain structure
370
End

FIG. 18