FIG. 1

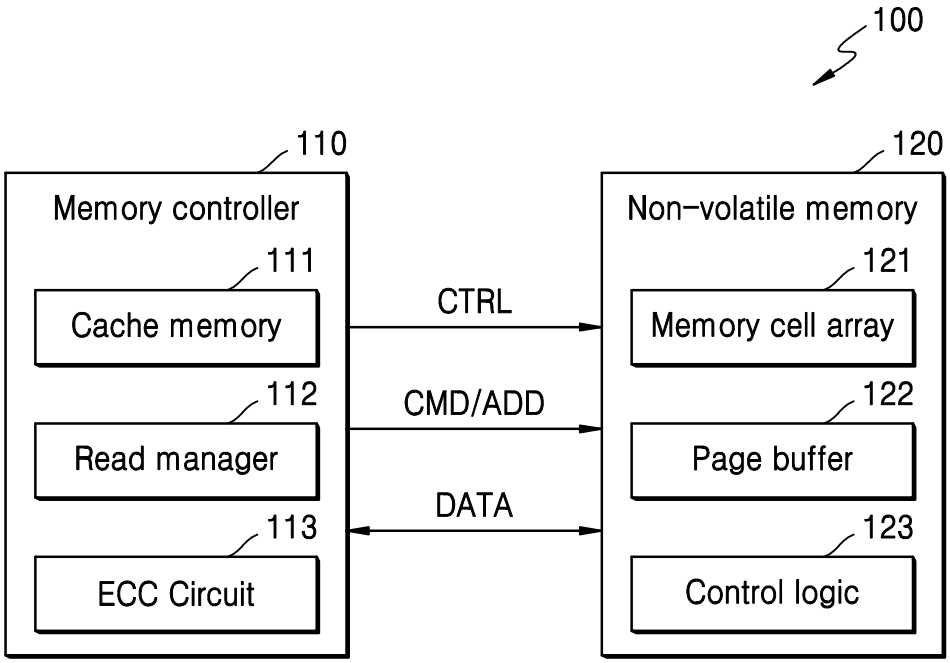

100
110
Memory controller
111
Cache memory
112
Read manager
113
ECC Circuit
CTRL
CMD/ADD
DATA
120
Non-volatile memory
121
Memory cell array
122
Page buffer
123
Control logic

FIG. 2

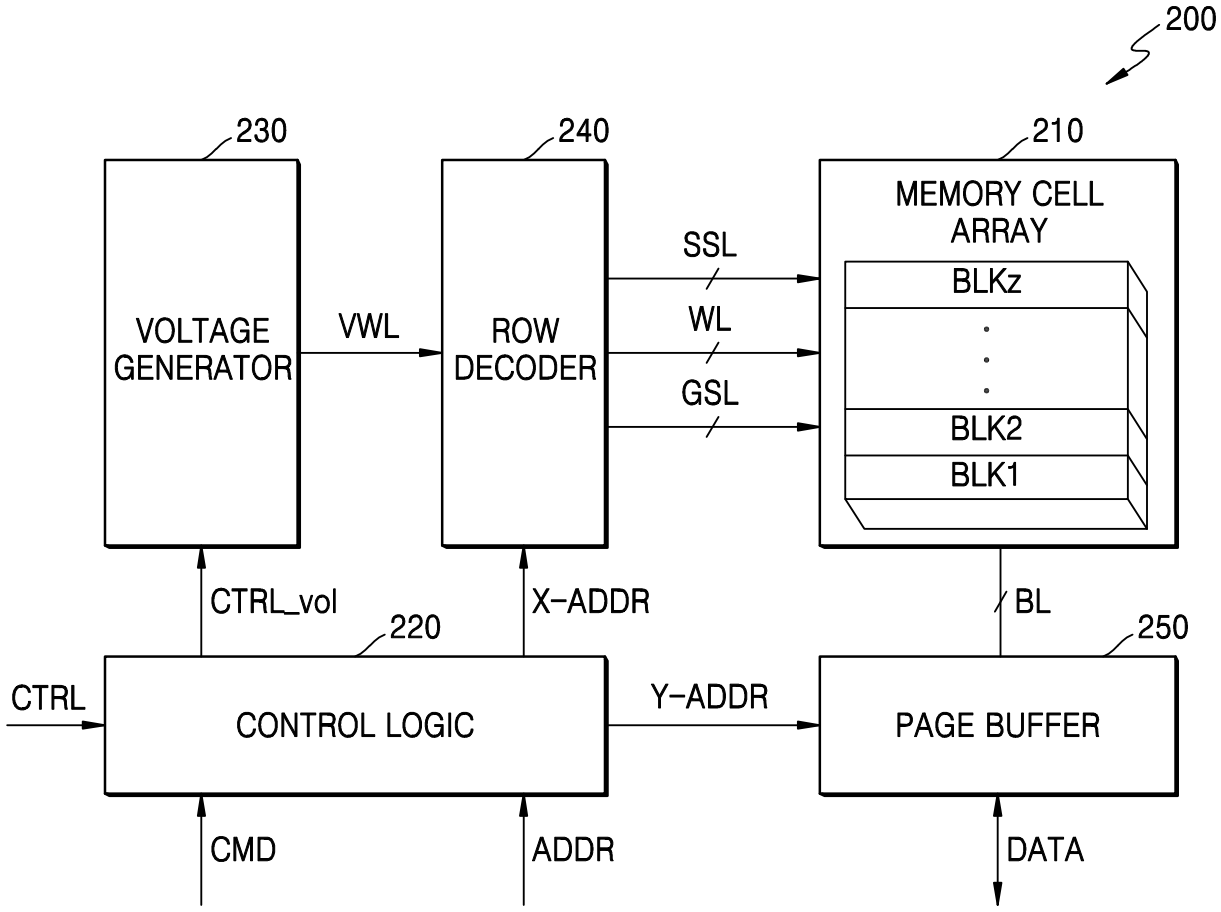

200
230
240
210
VOLTAGE GENERATOR
VWL
ROW DECODER
SSL
WL
GSL
MEMORY CELL ARRAY
BLKz
BLK2
BLK1
CTRL_vol
X-ADDR
BL
220
250
CTRL
CONTROL LOGIC
Y-ADDR
PAGE BUFFER
CMD
ADDR
DATA

FIG. 3

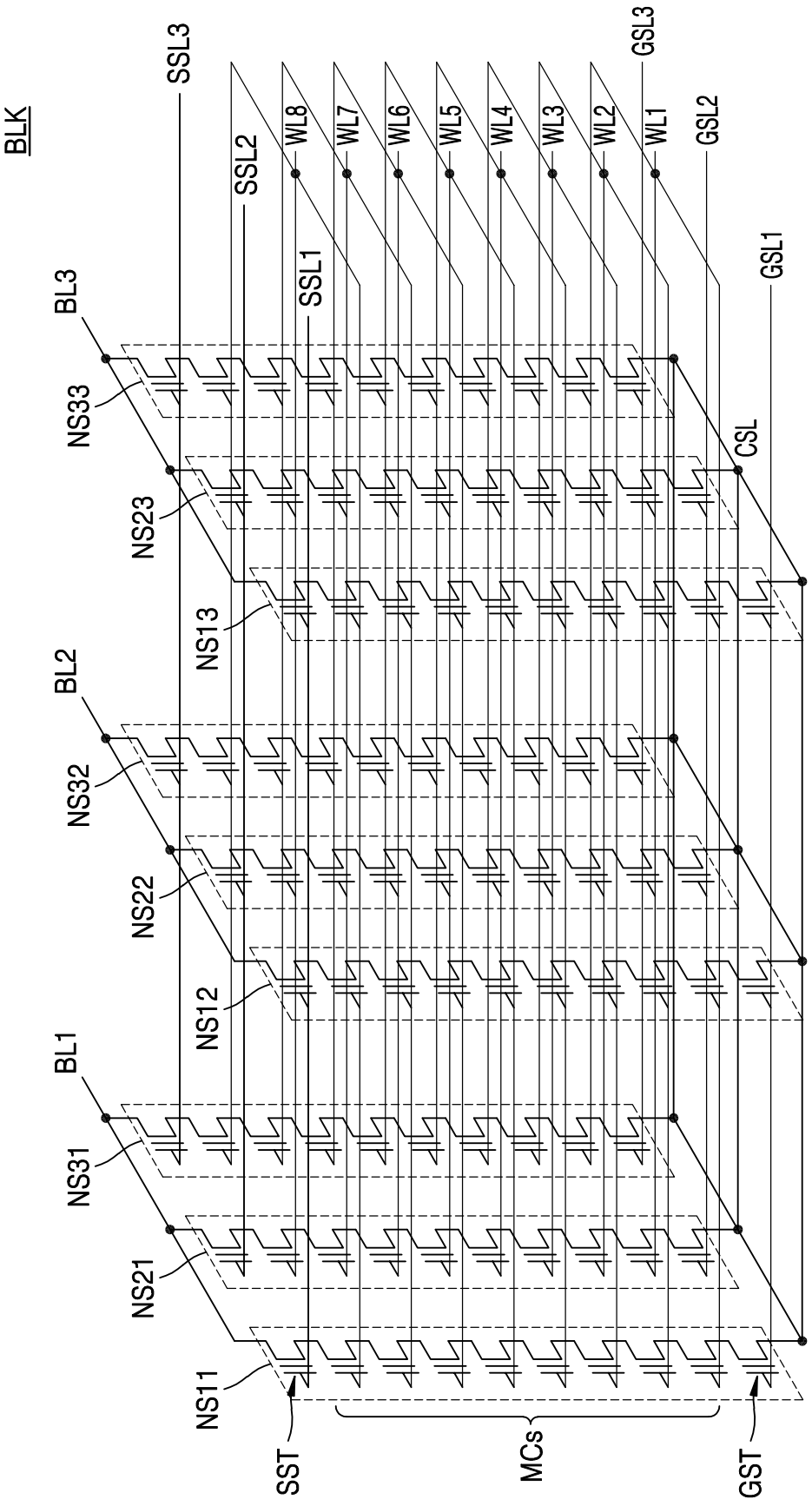

BLK
SSL3
SSL2
SSL1
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL3
GSL2
GSL1
CSL
BL3
BL2
BL1
NS33
NS23
NS13
NS32
NS22
NS12
NS31
NS21
NS11
SST
MCs
GST

FIG. 4

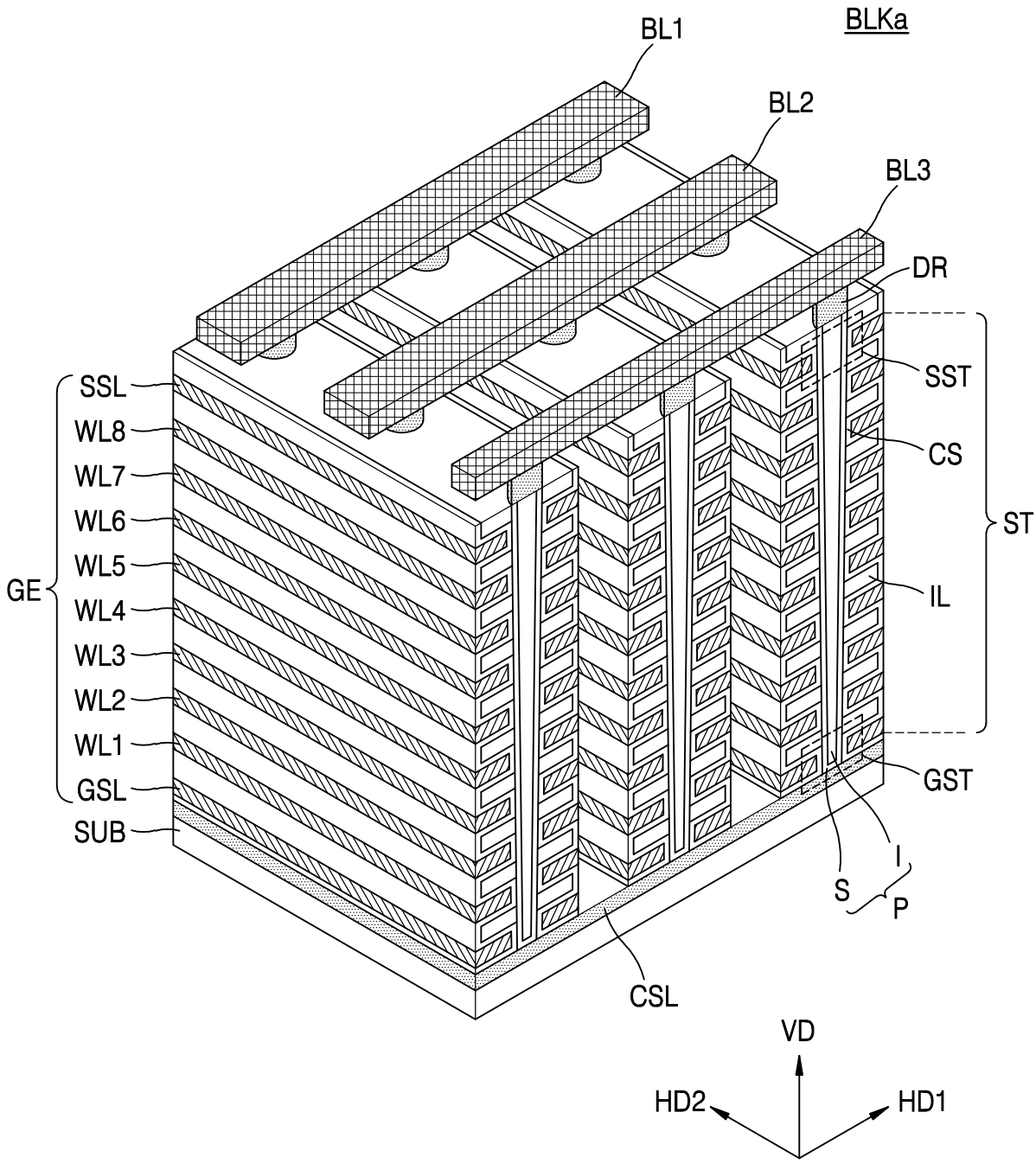

BLKa
BL1
BL2
BL3
DR
SST
CS
ST
IL
GST
I
S
P
CSL
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
VD
HD2
HD1

FIG. 5

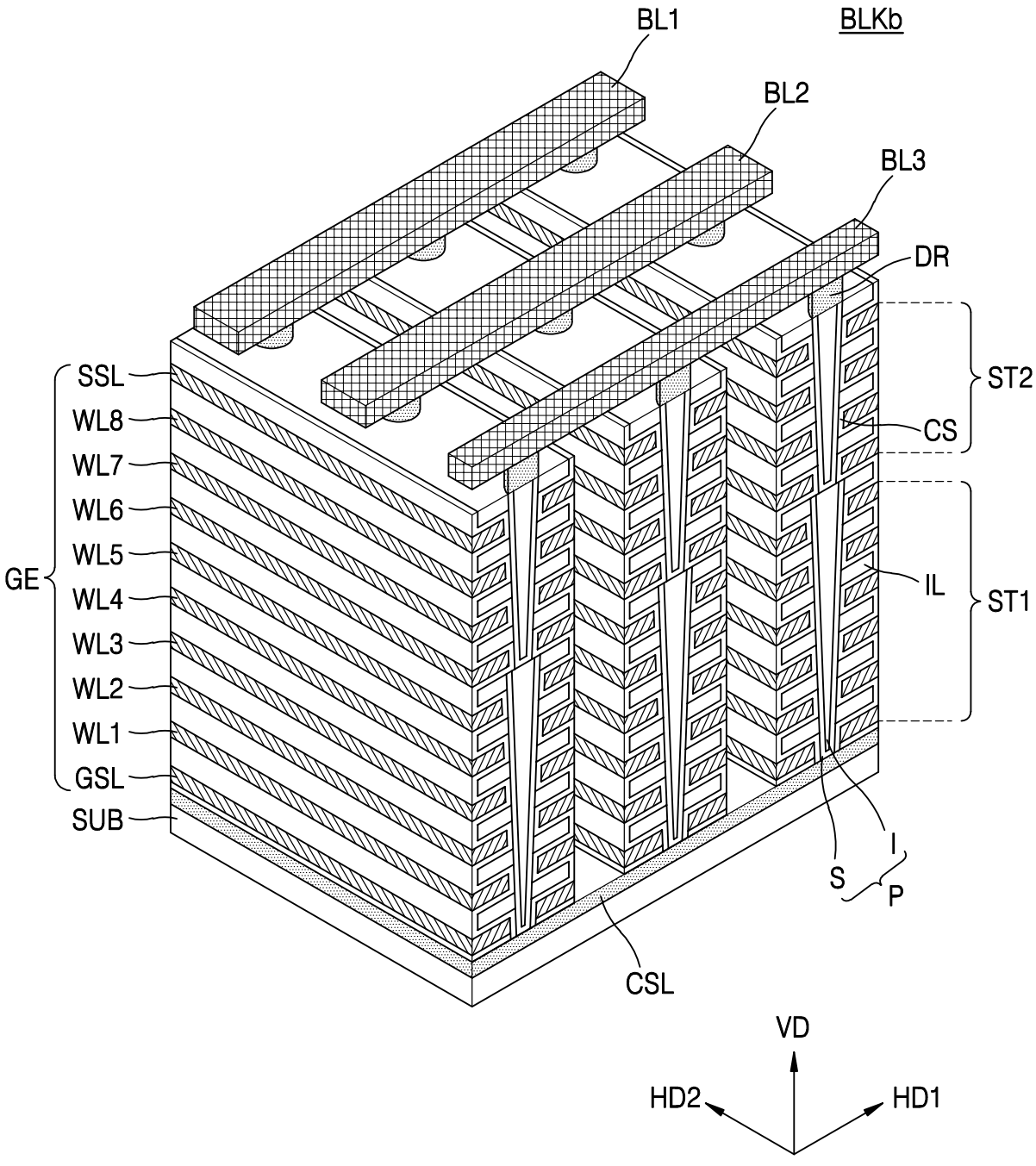

BL1
BLKb
BL2
BL3
DR
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
ST2
CS
IL
ST1
I
S
P
CSL
VD
HD2
HD1

FIG. 6

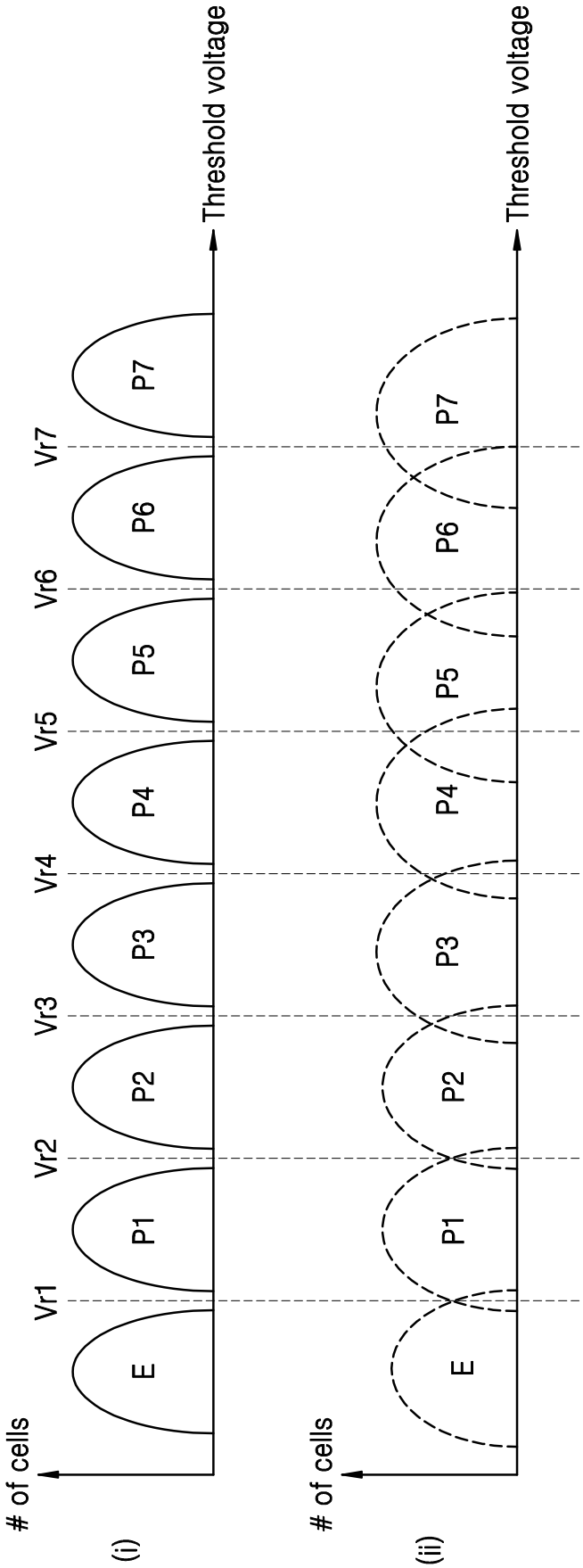

(i)
# of cells
Threshold voltage
E
P1
P2
P3
P4
P5
P6
P7
Vr1
Vr2
Vr3
Vr4
Vr5
Vr6
Vr7
(ii)
# of cells
Threshold voltage
E
P1
P2
P3
P4
P5
P6
P7

FIG. 7

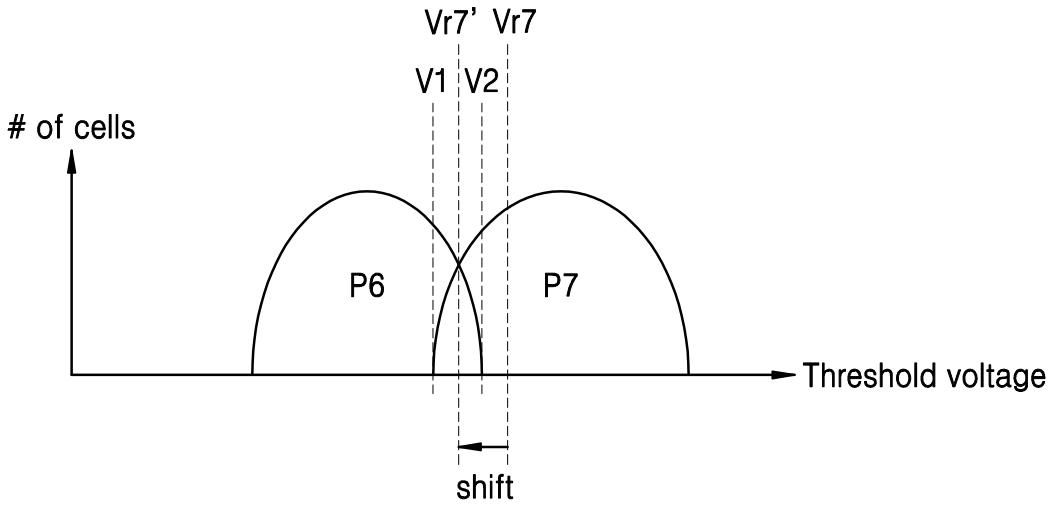


FIG. 8

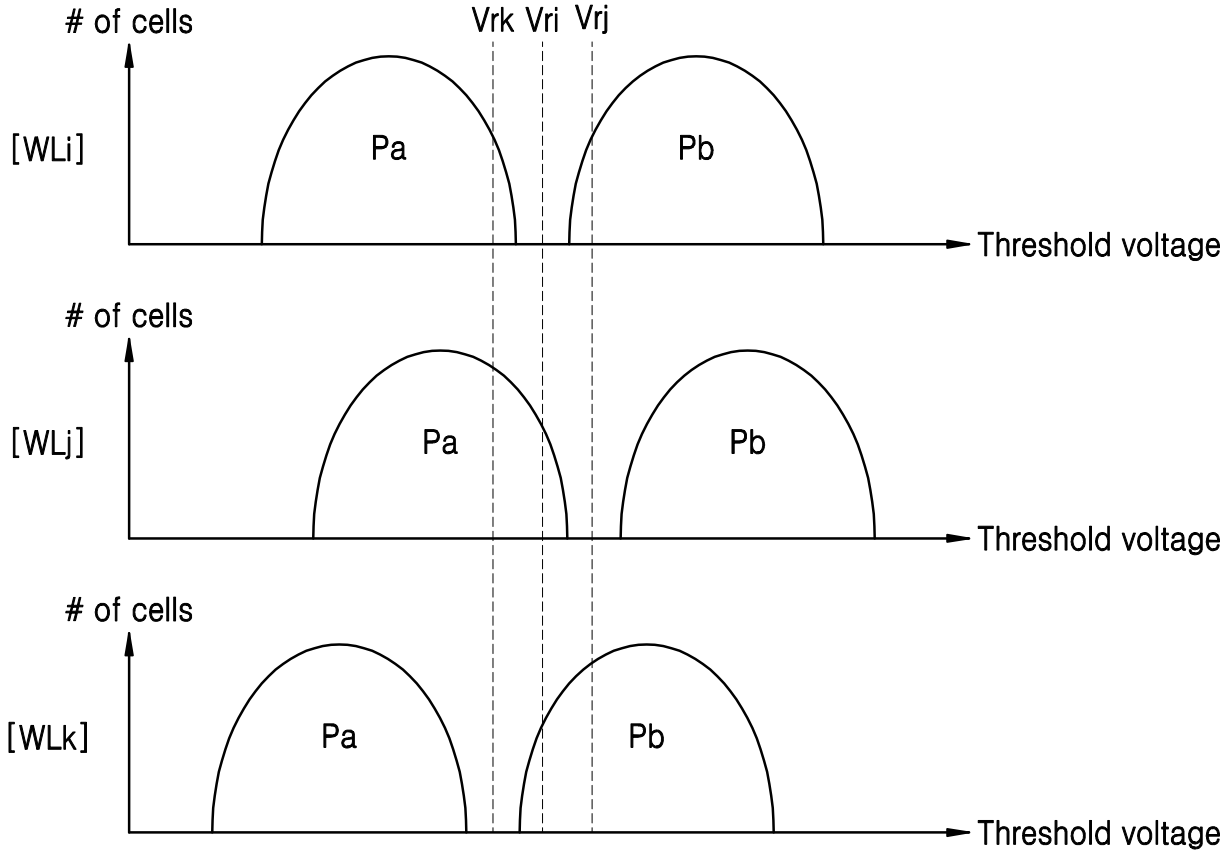

# of cells
Vrk Vri Vrj
[WLi]
Pa
Pb
Threshold voltage
# of cells
[WLj]
Pa
Pb
Threshold voltage
# of cells
[WLk]
Pa
Pb
Threshold voltage

FIG. 9

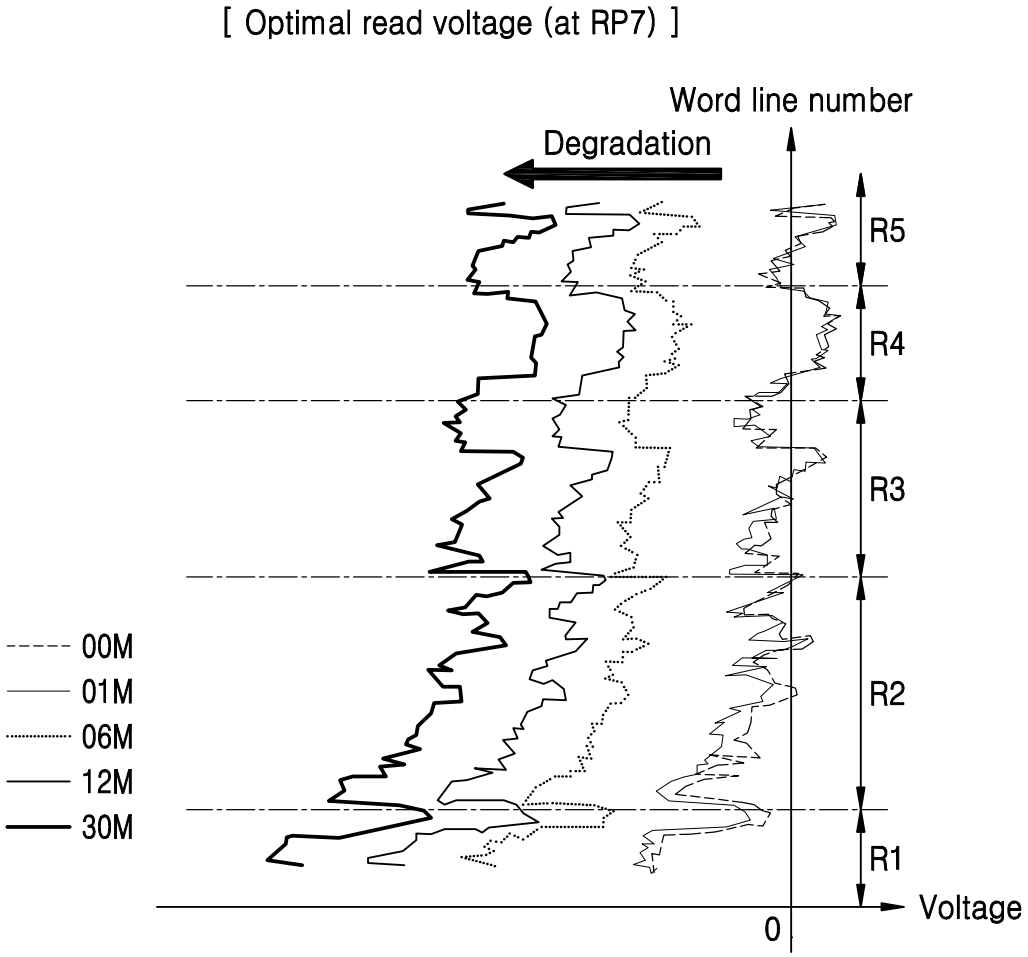

[Optimal read voltage (at RP7)]
Word line number
Degradation
R5
R4
R3
R2
R1
00M
01M
06M
12M
30M
0
Voltage

FIG. 10

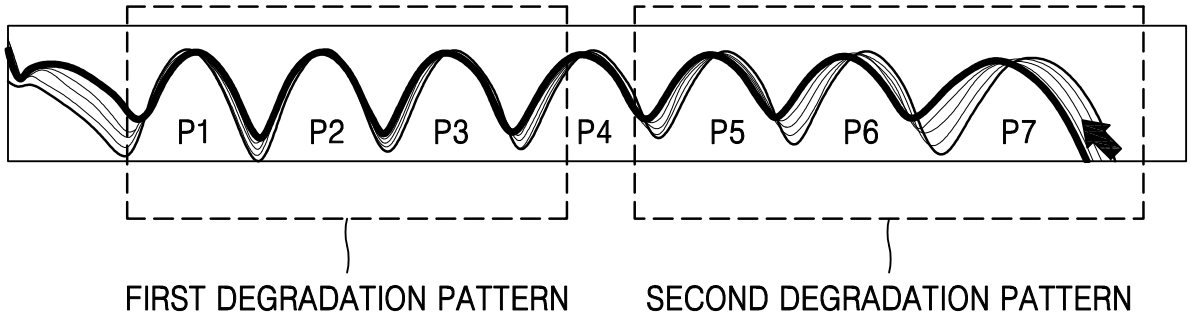

P1
P2
P3
P4
P5
P6
P7
FIRST DEGRADATION PATTERN
SECOND DEGRADATION PATTERN

FIG. 11

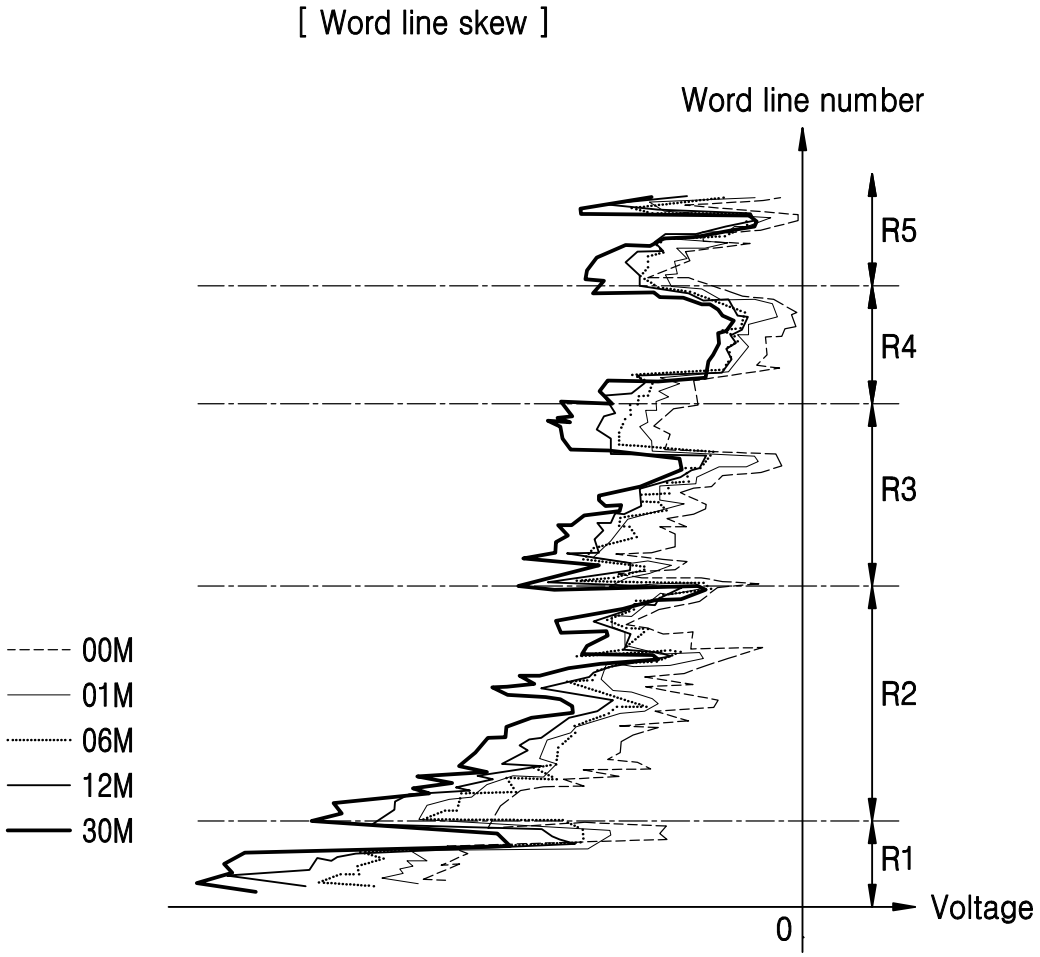

[Word line skew]
Word line number
R5
R4
R3
R2
R1
00M
01M
06M
12M
30M
0
Voltage

FIG. 12

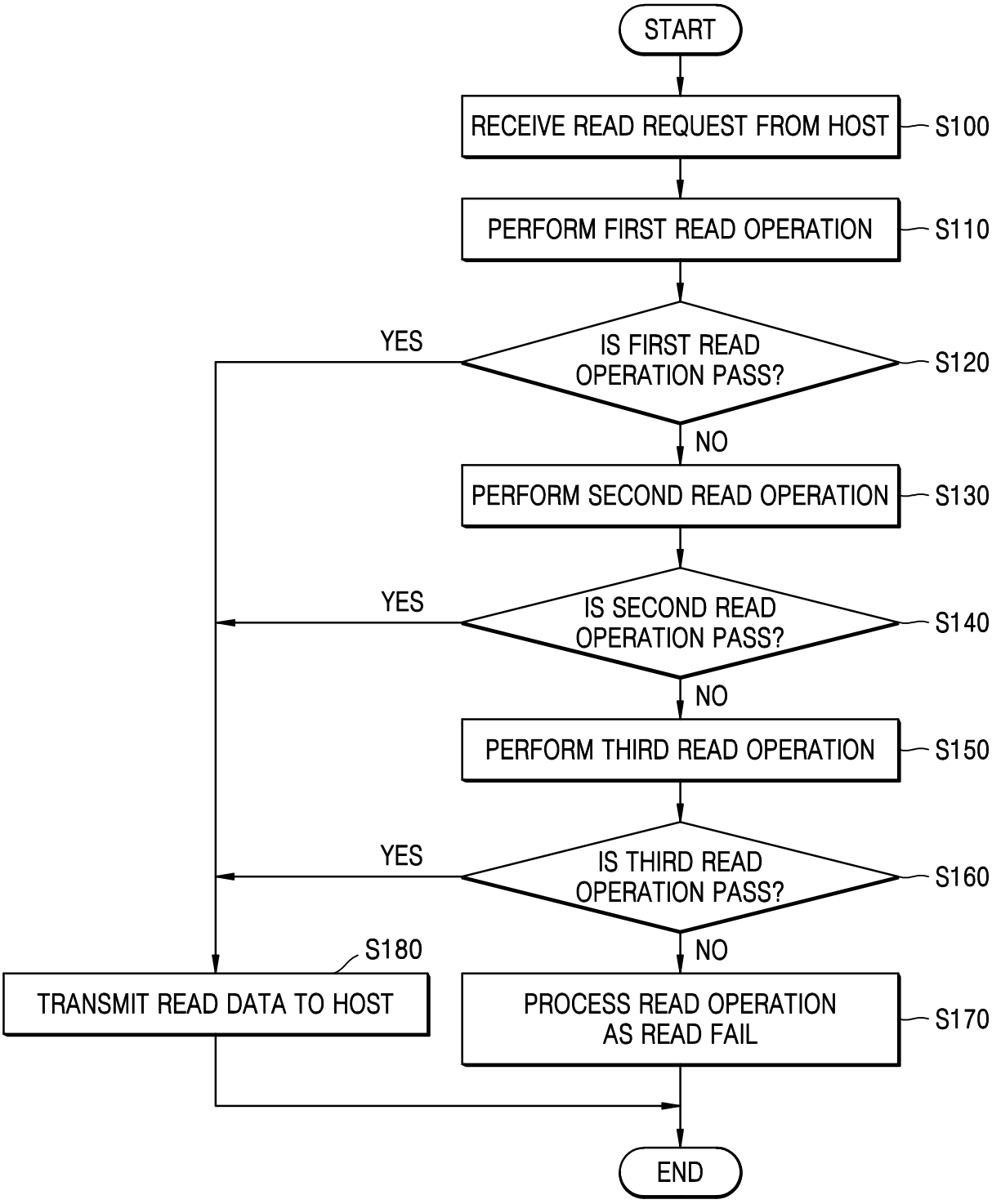

START
RECEIVE READ REQUEST FROM HOST
S100
PERFORM FIRST READ OPERATION
S110
IS FIRST READ OPERATION PASS?
S120
YES
NO
PERFORM SECOND READ OPERATION
S130
IS SECOND READ OPERATION PASS?
S140
YES
NO
PERFORM THIRD READ OPERATION
S150
IS THIRD READ OPERATION PASS?
S160
YES
NO
S180
TRANSMIT READ DATA TO HOST
PROCESS READ OPERATION AS READ FAIL
S170
END

FIG. 13

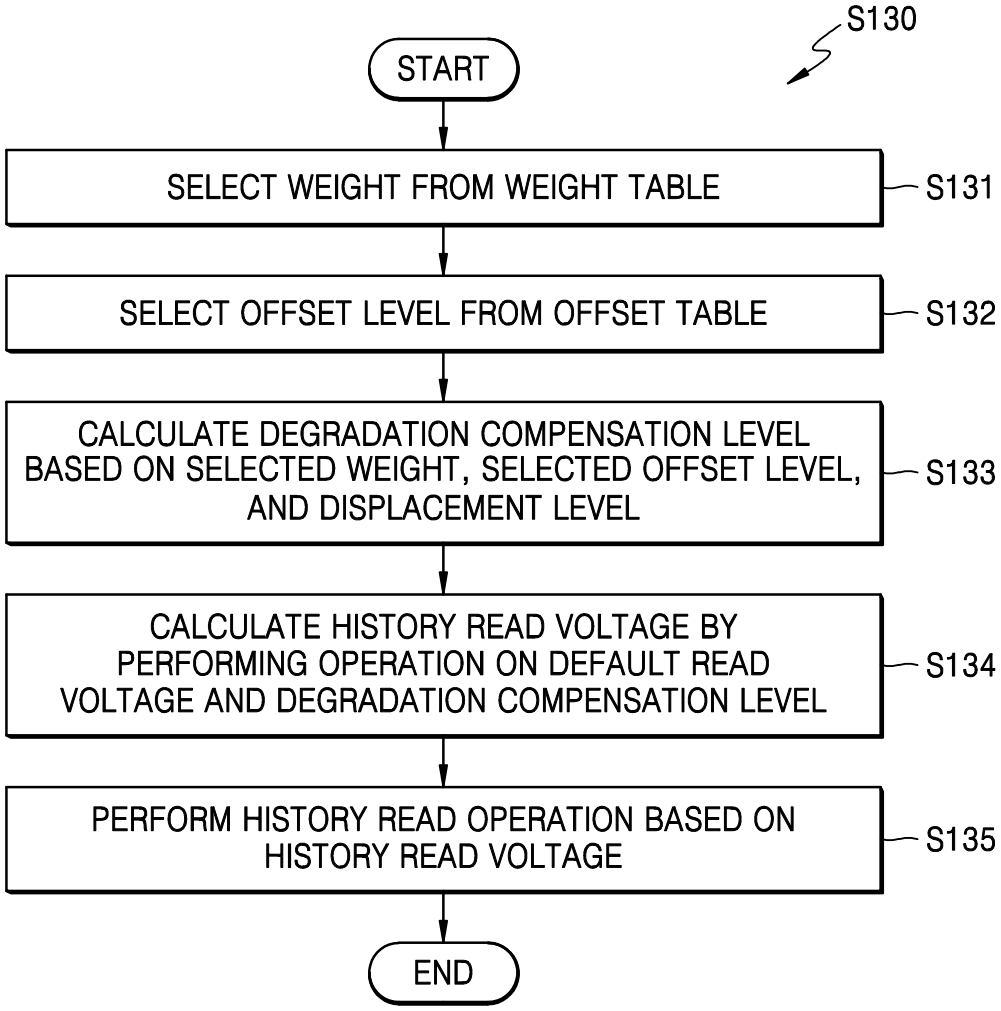

S130
START
SELECT WEIGHT FROM WEIGHT TABLE
S131
SELECT OFFSET LEVEL FROM OFFSET TABLE
S132
CALCULATE DEGRADATION COMPENSATION LEVEL BASED ON SELECTED WEIGHT, SELECTED OFFSET LEVEL, AND DISPLACEMENT LEVEL
S133
CALCULATE HISTORY READ VOLTAGE BY PERFORMING OPERATION ON DEFAULT READ VOLTAGE AND DEGRADATION COMPENSATION LEVEL
S134
PERFORM HISTORY READ OPERATION BASED ON HISTORY READ VOLTAGE
S135
END

FIG. 14A

α	RP1	RP2	RP3	RP4	RP5	RP6	RP7
R1 (WL0~WL11)	1.2	1.3	3.1	3.9	2	1.6	1.4
R2 (WL12~WL27)	1.2	1.3	3	4	2	1.6	1.4
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
RN (WL189~WL200)	1.2	1.3	2.2	1.1	1.5	1.3	1

FIG. 14B

β	RP1	RP2	RP3	RP4	RP5	RP6	RP7
R1 (WL0~WL11)	-30	-30	-30	-30	-30	-30	-30
R2 (WL12~WL27)	-35	-20	-45	-45	-45	-45	-40
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
RN (WL189~WL200)	-20	-20	-10	0	0	0	-20

FIG. 15

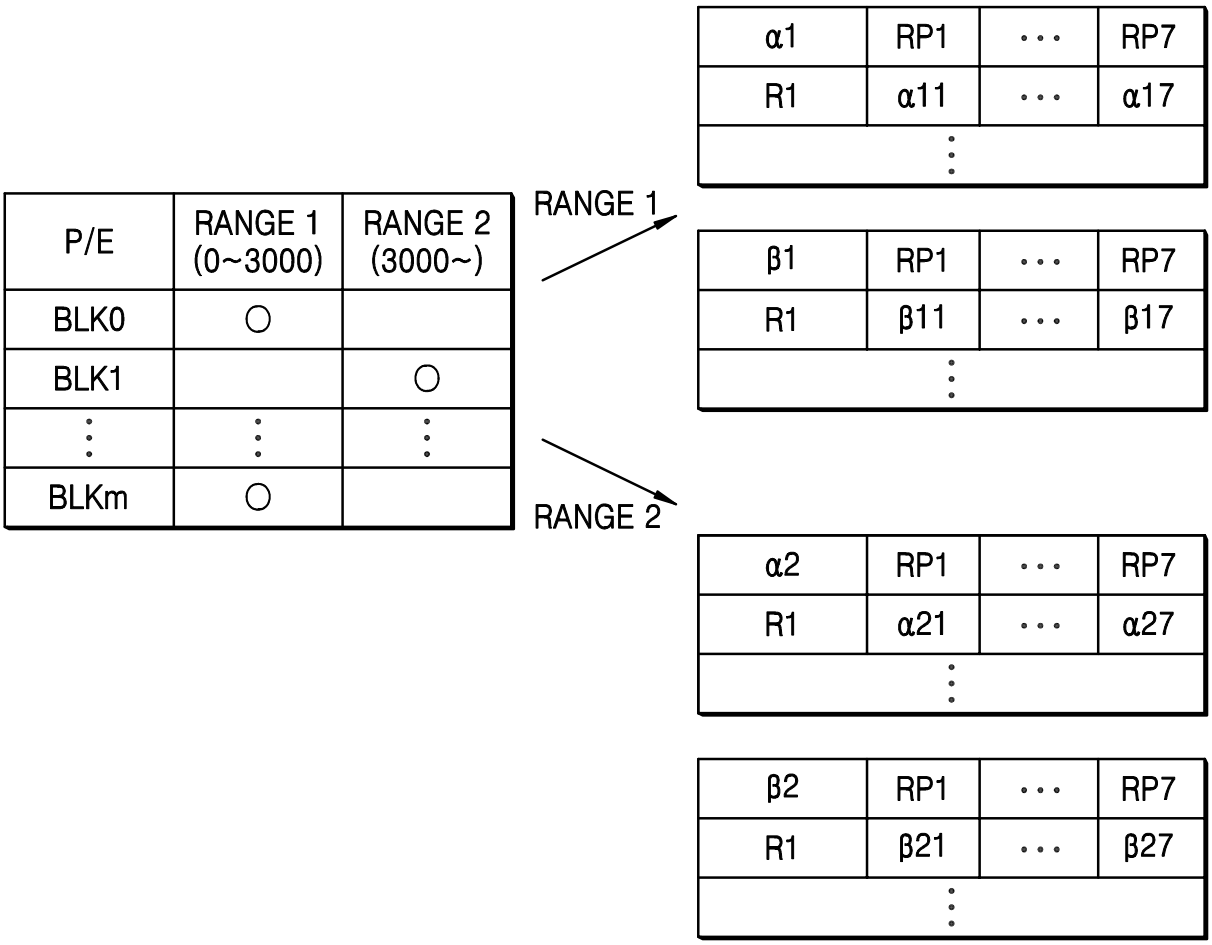

P/E
RANGE 1 (0~3000)
RANGE 2 (3000~)
BLK0
BLK1
BLKm
RANGE 1
RANGE 2
α1
RP1
RP7
R1
α11
α17
β1
β11
β17
α2
α21
α27
β2
β21
β27

FIG. 16

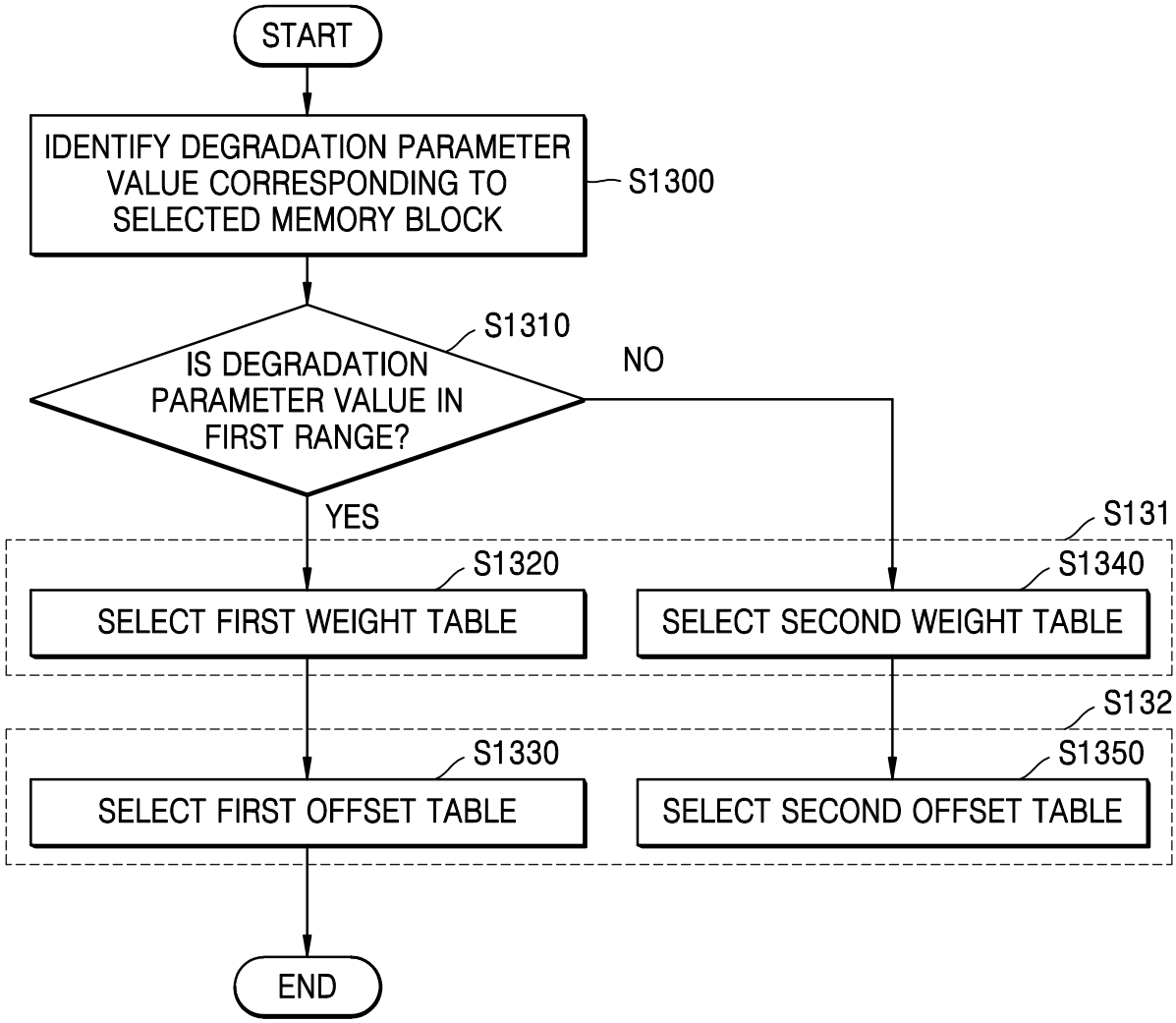

START
IDENTIFY DEGRADATION PARAMETER VALUE CORRESPONDING TO SELECTED MEMORY BLOCK
S1300
S1310
IS DEGRADATION PARAMETER VALUE IN FIRST RANGE?
NO
YES
S131
S1320
SELECT FIRST WEIGHT TABLE
S1340
SELECT SECOND WEIGHT TABLE
S132
S1330
SELECT FIRST OFFSET TABLE
S1350
SELECT SECOND OFFSET TABLE
END

FIG. 17

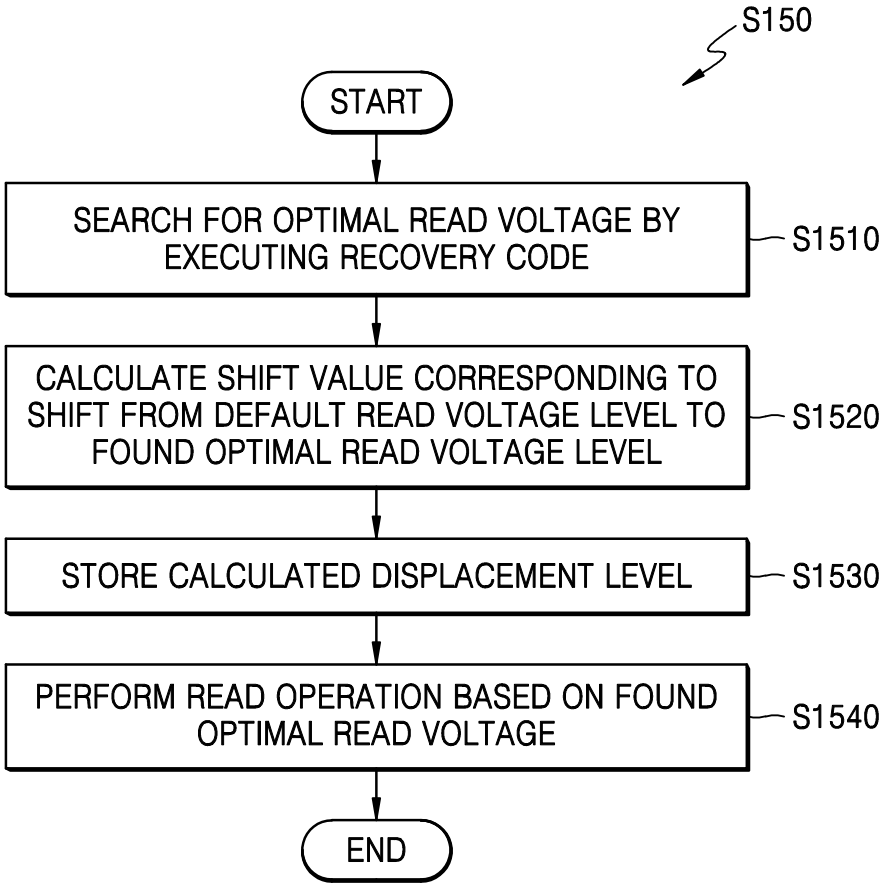

S150
START
SEARCH FOR OPTIMAL READ VOLTAGE BY EXECUTING RECOVERY CODE
S1510
CALCULATE SHIFT VALUE CORRESPONDING TO SHIFT FROM DEFAULT READ VOLTAGE LEVEL TO FOUND OPTIMAL READ VOLTAGE LEVEL
S1520
STORE CALCULATED DISPLACEMENT LEVEL
S1530
PERFORM READ OPERATION BASED ON FOUND OPTIMAL READ VOLTAGE
S1540
END

FIG. 18

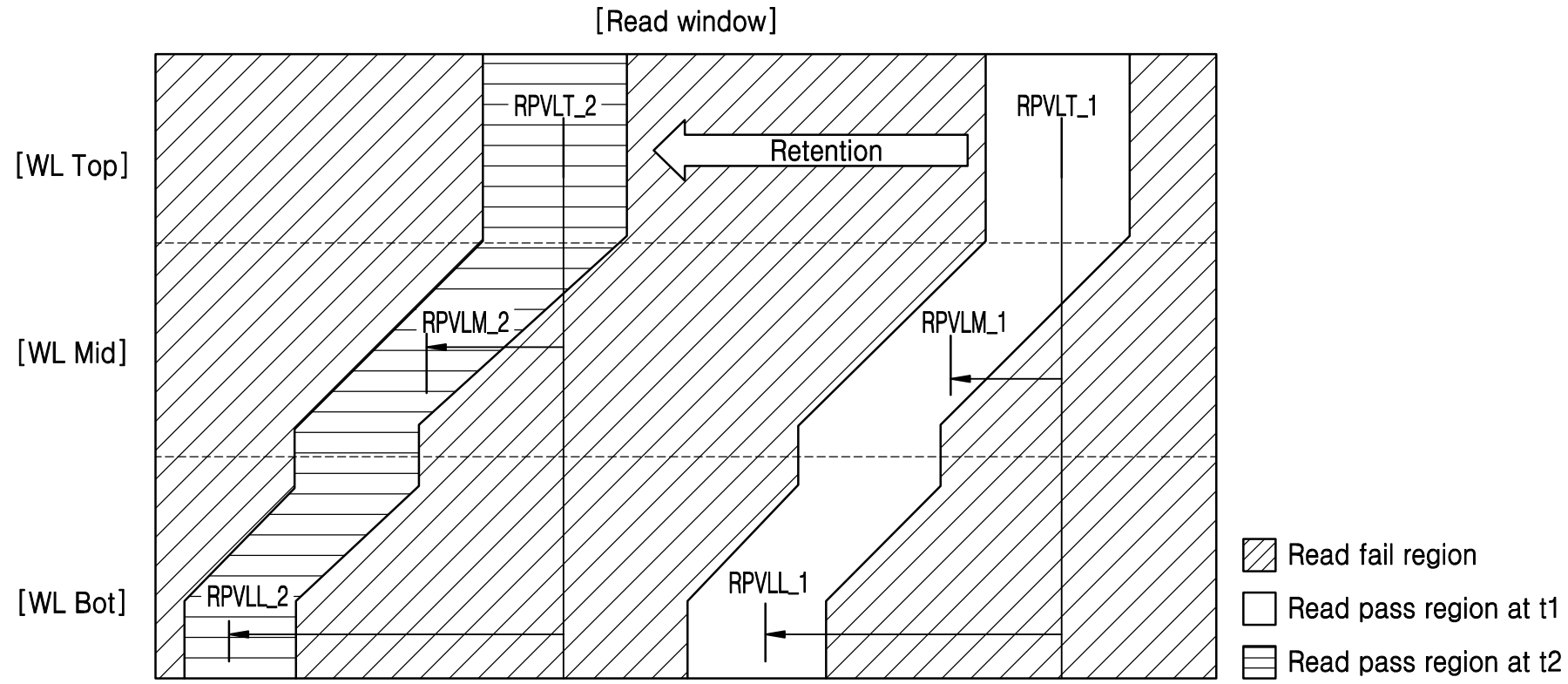

[Read window]
[WL Top]
[WL Mid]
[WL Bot]
RPVLT_2
RPVLT_1
Retention
RPVLM_2
RPVLM_1
RPVLL_2
RPVLL_1
Read fail region
Read pass region at t1
Read pass region at t2

FIG. 19A

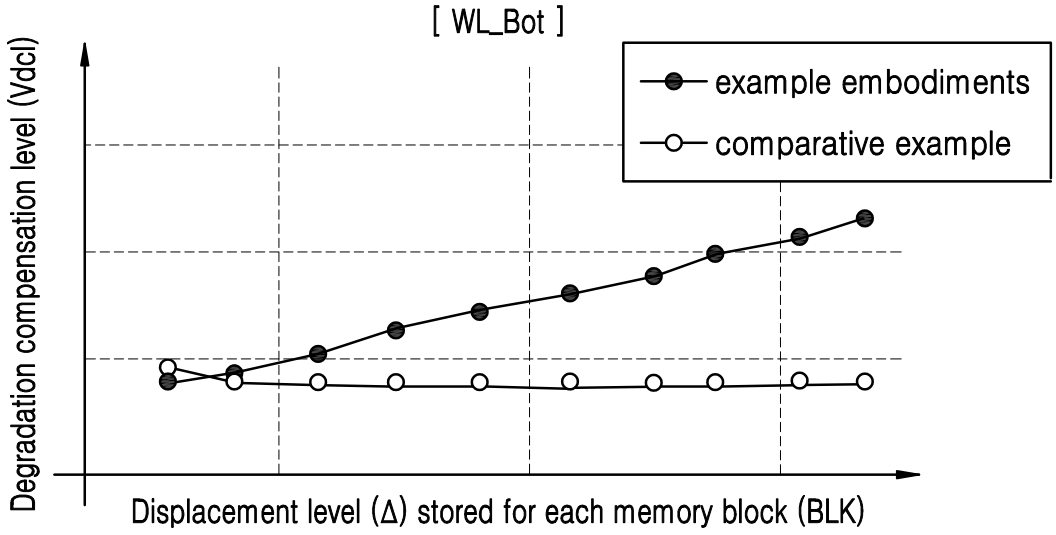

[WL_Bot]
example embodiments
comparative example
Degradation compensation level (Vdcl)
Displacement level (Δ) stored for each memory block (BLK)

FIG. 19B

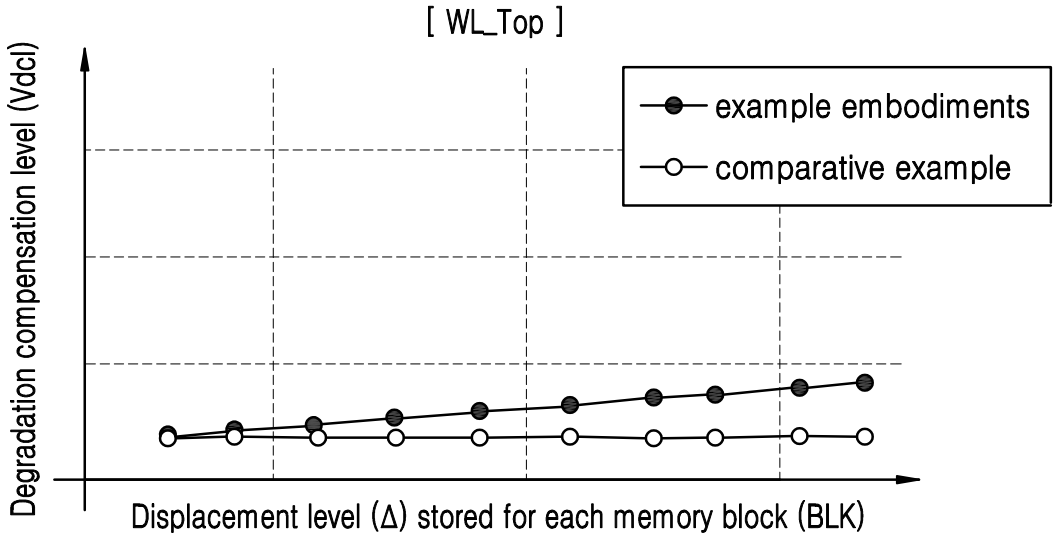

[WL_Top]
example embodiments
comparative example
Degradation compensation level (Vdcl)
Displacement level (Δ) stored for each memory block (BLK)

FIG. 20

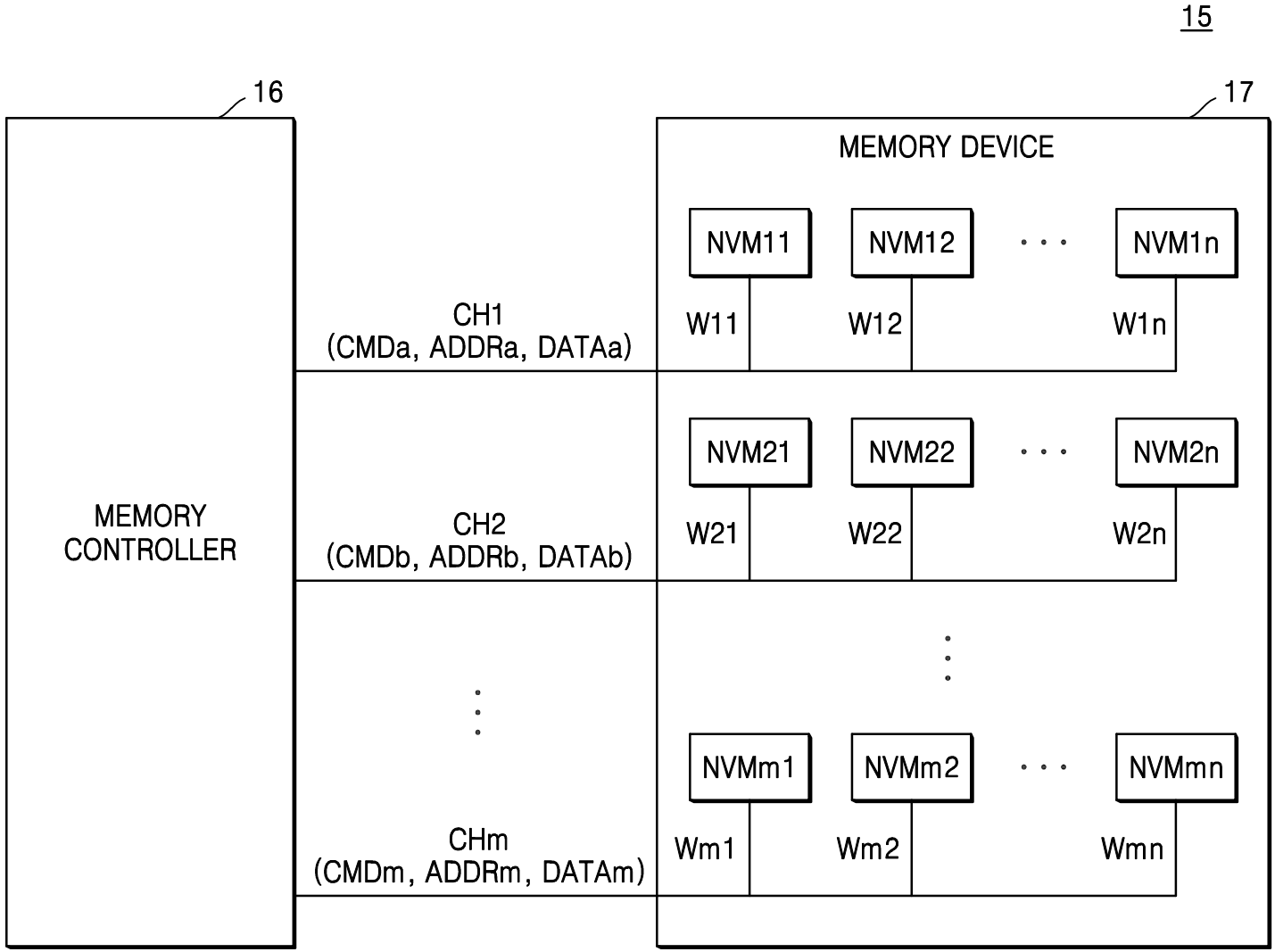

15
16
17
MEMORY DEVICE
MEMORY CONTROLLER
CH1
(CMDa, ADDRa, DATAa)
CH2
(CMDb, ADDRb, DATAb)
CHm
(CMDm, ADDRm, DATAm)
NVM11
NVM12
NVM1n
W11
W12
W1n
NVM21
NVM22
NVM2n
W21
W22
W2n
NVMm1
NVMm2
NVMmn
Wm1
Wm2
Wmn

FIG. 21

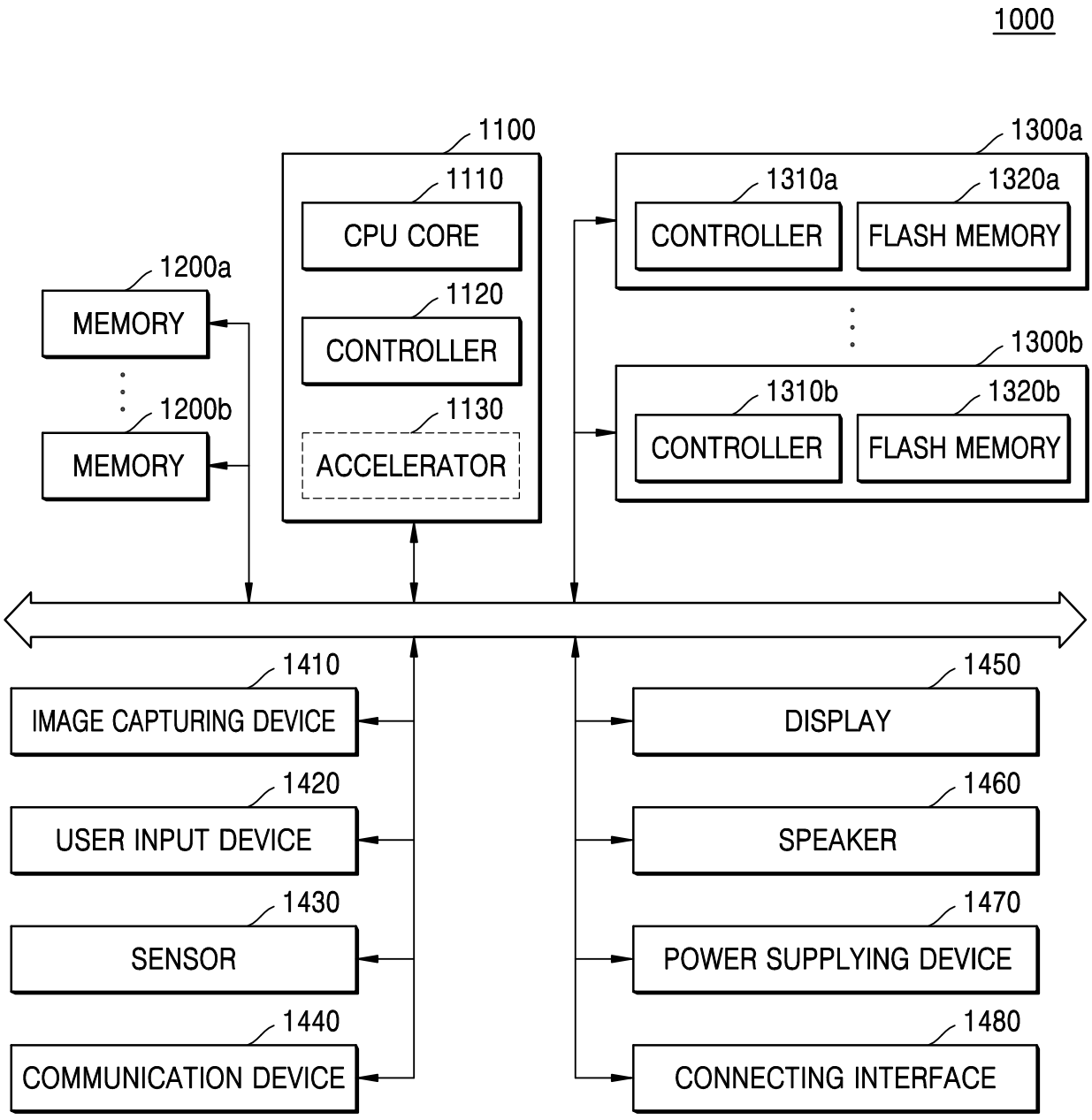

1000
1100
1110
CPU CORE
1120
CONTROLLER
1130
ACCELERATOR
1200a
MEMORY
1200b
MEMORY
1300a
1310a
CONTROLLER
1320a
FLASH MEMORY
1300b
1310b
CONTROLLER
1320b
FLASH MEMORY
1410
IMAGE CAPTURING DEVICE
1420
USER INPUT DEVICE
1430
SENSOR
1440
COMMUNICATION DEVICE
1450
DISPLAY
1460
SPEAKER
1470
POWER SUPPLYING DEVICE
1480
CONNECTING INTERFACE

FIG. 22

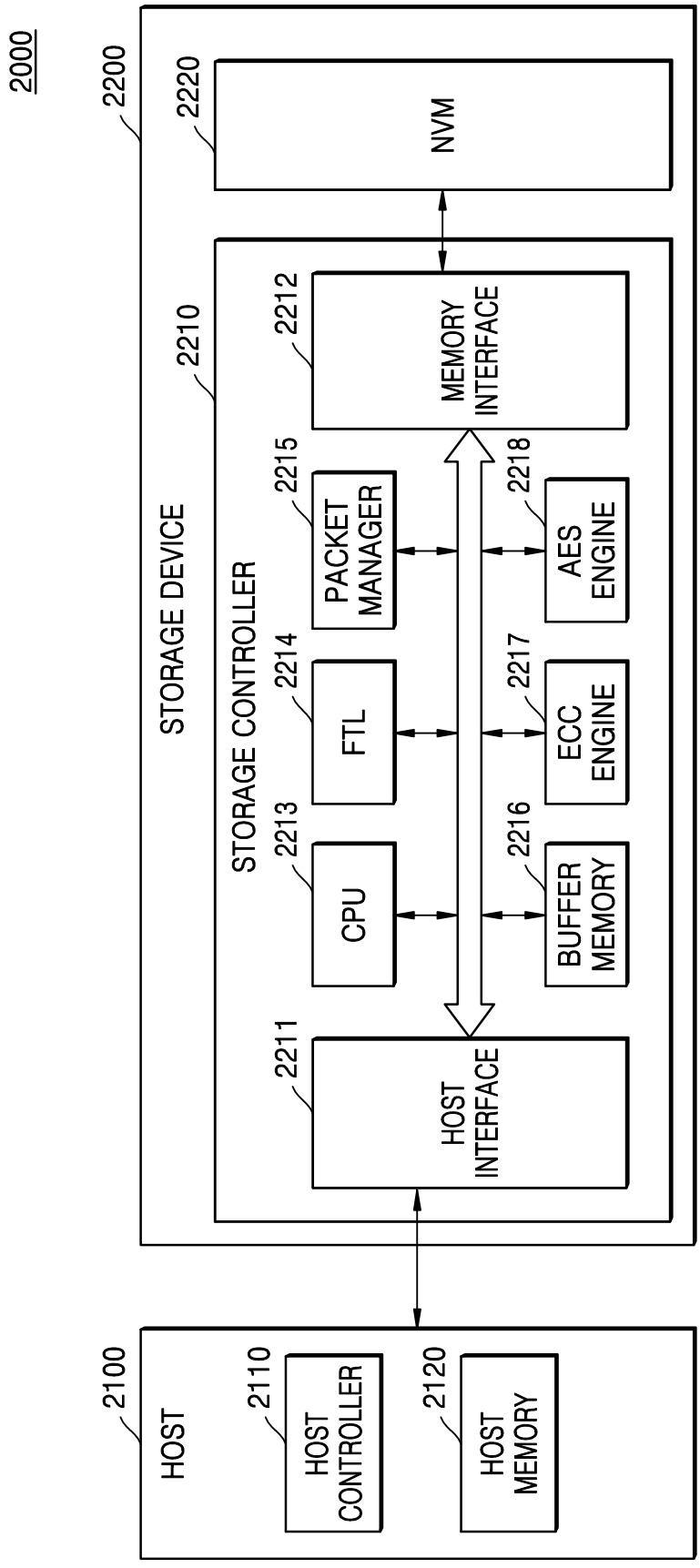
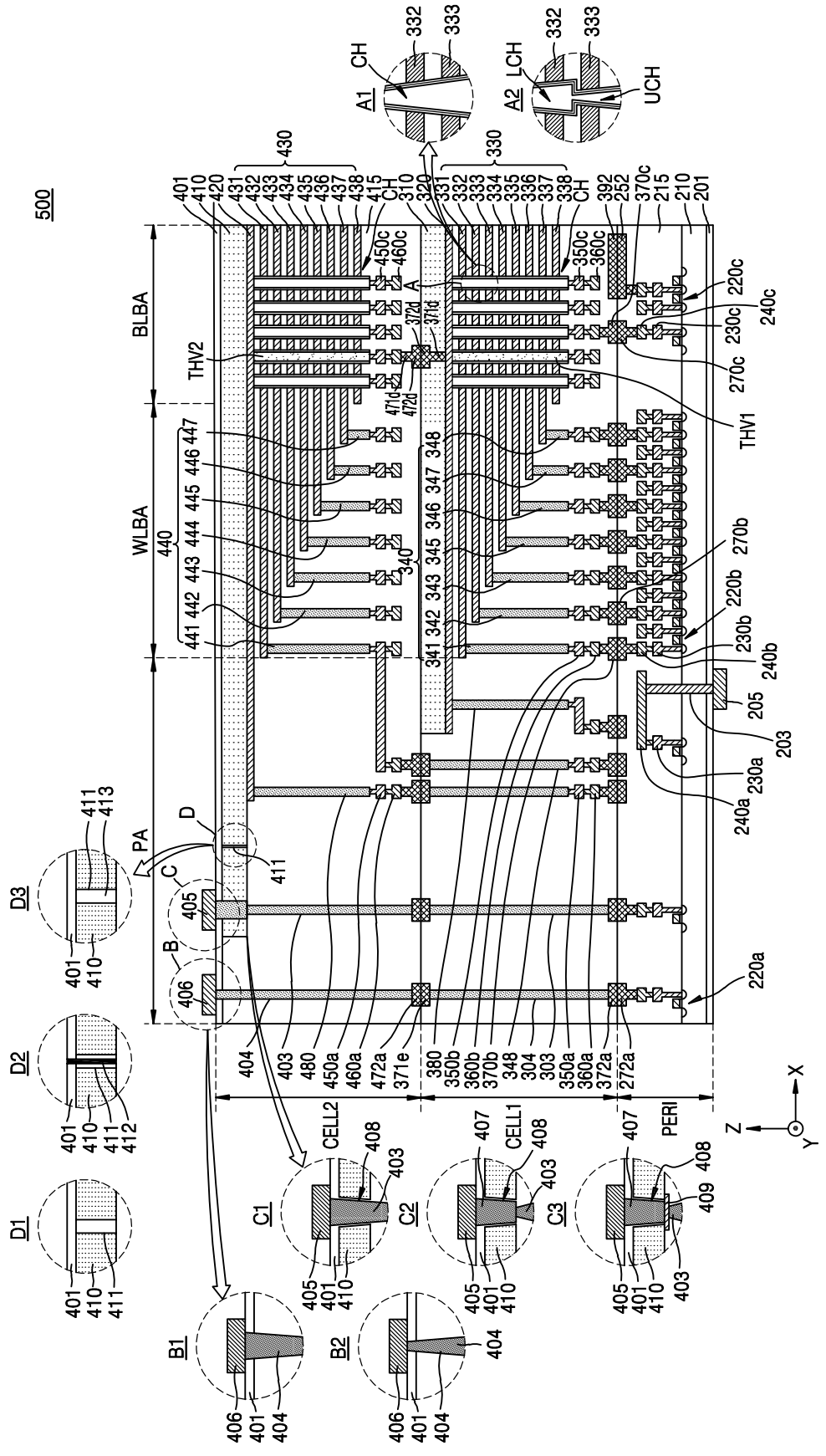

2000
2200
2220
NVM
STORAGE DEVICE
2210
STORAGE CONTROLLER
2212
MEMORY INTERFACE
2215
PACKET MANAGER
2218
AES ENGINE
2214
FTL
2217
ECC ENGINE
2213
CPU
2216
BUFFER MEMORY
2211
HOST INTERFACE
2100
HOST
2110
HOST CONTROLLER
2120
HOST MEMORY

FIG. 23


500
BLBA
WLBA
PA
THV1
THV2
CELL1
CELL2
PERI
A1
A2
B1
B2
C1
C2
C3
D1
D2
D3
CH
LCH
UCH
X
Y
Z