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METHOD OF CONTROLLING THE SWITCHING DI/DT
AND DV/DT OF A MOS-GATED POWER TRANSISTOR

BACKGROUND OF THE INVENTION

The present invention is directed to clamped inductive load circuits and, more particularly, to clamped inductive load circuits in which a MOS gate controlled ("MOS-gated") power transistor is switched on and off.

Power transistor devices, while turning on or off, divert the flow of current and reconfigure the voltage distribution of a power conversion circuit. MOS-gated transistors, such as MOSFETs or IGBTs, perform this operation within a fraction of a microsecond at very rapid voltage and current slew rates. The fast switching wavefronts of their waveforms are desirable for reducing switching losses and for increasing operating frequency but also have the adverse effect of generating unwanted electromagnetic interference (EMI) in the surrounding environment. In environments where the EMI susceptibility is critical or where EMI interference regulated by legislation, it is desirable to independently adjust the voltage and current waveforms to meet these requirements without unnecessarily increasing the switching losses.

A clamped inductive load circuit is a power circuit whose load inductance prevents its current from being brought to zero within a cycle of the operating frequency. Most power conversion circuits are clamped inductive load circuit. Fig. 1A shows a simplified representation of a clamped inductive load circuit in which a MOSFET 103 goes in and out of conduction. The switching transient can be divided into a number of intervals, shown in Fig. 1B and 1C, wherein the current rise interval and the voltage fall interval follow each other and can be controlled independently.

While the gate drive circuit feeds current to the gate, the gate voltage rises in the manner of a capacitor being charged, shown as interval 1 in Fig. 1B. When the gate voltage V_g reaches the threshold voltage of the MOSFET 103, the drain current I_d increases and diverts current away from the freewheeling diode 102, as shown in interval 2. As long as the diode 102 carries current, the drain voltage is clamped to the supply voltage. When all the current (plus reverse recovery current, if any) is transferred from the diode to the MOSFET, the drain voltage falls to its final, fully enhanced, value. Hence, the drain voltage only begins to fall after the drain current rise is completed which allows separate control of both waveforms. This process is described in detail in International Rectifier Application note AN-944: "A New Gate Charge Factor Leads to Easy Drive Design for Power MOSFET Circuits".

During the drain current rise, shown in interval 2, the drain current is proportional to the gate voltage, and the rate of rise of the gate voltage determines the switching di/dt . Since the gate capacitance of MOSFET 103 behaves as capacitor 103B, the

current rise time can be controlled by controlling the quantity of current supplied to the gate. The reverse recovery of the diode prolongs interval 2.

During the drain voltage fall, shown as interval 3, the output capacitance 103A and the reverse transfer capacitance 103C of MOSFET 103 discharge. The rate at which these two capacitances are discharged determine the rate at which the drain voltage falls. While the output capacitance discharges rapidly through the channel resistance, the reverse transfer capacitance only discharges through the gate drive circuit. The flat portion of the gate voltage curve shown in interval 3 indicates that the current supplied to the gate terminal is almost completely delivered to the reverse transfer capacitance whereas the voltage across the input capacitance does not change. Thus, the value of the dv/dt here can be controlled by supplying an appropriate amount of current to the gate.

At the end of interval 3, the switching transient is completed and any additional current supplied to the gate does not change the drain voltage or drain current, as shown in interval 4.

The turn-off process is generally a mirror image of the turn-on process. First, the gate voltage V_g is reduced to a value that barely maintains the drain current, as depicted in interval 1 of Fig. 1C. Then, the voltage across the device rises, while the drain current is constant, as shown in interval 2. When the voltage across the MOSFET 103 exceeds the supply voltage by a value equal to the diode voltage drop, the diode starts conducting and load current is transferred from the MOSFET through the diode, as shown in interval 3. As when the device turns on, the rise in drain voltage and

the fall in drain current occur sequentially. The drain voltage rise time is thus substantially determined by the charging of the reverse transfer capacitance through the gate circuit impedance 104, and the subsequent drain current fall time is determined by the discharging of the input capacitance. A voltage overshoot is often present at the drain when interval 2 ends which prolongs this interval.

MOS-gated devices with a significant minority carrier component of current, such as IGBTs, MCTs and other derivatives, behave somewhat differently at turn-off because their current fall time is influenced by the recombination of the minority carriers. Similarly, the current rise time during their turn-on is influenced by the carrier injection efficiency.

Typically, resistors are incorporated into the gate drive circuit to slow down the switching. An additional resistor 201 and diode 202, as shown in Fig. 2B, may be added to the circuit of Fig. 1A to change the wave form at turn-on and at turn-off and, particularly, to limit the reverse recovery current from the diode. Because different respective current values are needed to obtain the desired di/dt and dv/dt , the selection of the added resistor requires a compromise between obtaining the desired di/dt and obtaining the desired dv/dt . The added resistors in the gate drive circuit also make the circuit more prone to dv/dt induced turn-on, namely an unwanted conduction caused by a transient current in the drain that is coupled to the gate through the reverse transfer capacitance.

By contrast, the diode 202 shunts the resistor 201 shown in Fig. 2A and bypasses the resistor, thus providing a low impedance path for fast transients

injected from the drain, but eliminates the possibility of providing turn-off waveshaping.

Control of dv/dt was attempted by Siliconix using a gate driver IC, such as an Si9910. As shown in Fig. 3, the voltage slew rate is sensed using a small capacitance 308 connected to the drain of power device 310. The sensed dv/dt is controlled by a feedback loop. The circuit however, uses a linear loop which is prone to oscillations. The chip also provides control of the peak current, but di/dt in the power device is controlled only when appropriate feedback is provided.

Additionally, the short-circuit protection scheme used in this circuit typically turns off the power transistor in two steps to avoid voltage overshoots frequently associated with fast turn-off of a large current. The gate voltage is initially reduced to approximately half its initial value and then is totally shut off. This approach allows a power device to be turned off slowly, rather than in two steps, from a short circuit condition. The circuit, however, does not control di/dt during switching because they are intended to protect the device from the overvoltage transient associated with the turn-off of a fault, such as short circuit, are triggered by the fault and are otherwise inoperative during normal operation. Such methods are described in "IGBT Fault Current Limiting Circuit" by R. Chokhawala and G. Castino, IR IGBT Data Book IGBT-3, page E-127.

It therefore is desirable to provide a circuit which both drives a MOS-gated power transistor device and controls both the switching di/dt and the switching dv/dt .

SUMMARY OF THE INVENTION

The present invention controls the switching di/dt and dv/dt of a MOS gate controlled power transistor by respectively controlling the voltage and current wavefronts of the waveform. Both open loop and closed loop control are available. The di/dt is sensed in a lossless and inexpensive manner.

According to an aspect of the invention, open loop control of the switching di/dt and switching dv/dt at turn-on the MOS-gated device is provided by coupling a common terminal of a current generator circuit, which provides a current to the gate of the MOS device, to a first resistor for controlling the di/dt . When a negative dv/dt is detected, the common terminal of the current generator circuit is decoupled from the first resistor and is then coupled to a second resistor for controlling the switching dv/dt . The first and second resistors are, in turn, coupled to the source terminal of the MOS-gated device. An analogous operation using this circuit provides turn-off control of the switching dv/dt and the switching di/dt of the MOS-gated power device.

According to another aspect of the invention, closed loop control is provided by further measuring the switching dv/dt and the switching di/dt which are then fed back to the circuit to control the current supplied to the gate of the MOS-gated device.

According to a further novel aspect of the invention, the value of the switching di/dt is determined by measuring the voltage difference across the length of a calibrated wire bond having a predetermined length and diameter.

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Other features and advantages of the present invention will be apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in greater detail in the following detailed description with reference to the drawings in which:

Fig. 1A is a schematic diagram showing a known clamped inductive load circuit; Fig. 1B illustrates the turn-on waveforms of the power transistor of the circuit of Fig. 1A; and Fig. 1C illustrates the turn-off waveforms of the power transistor of the circuit of Fig. 1A.

Figs. 2A and 2B show known circuits for slowing down the turn-on and turn-off of the power transistor of the circuit of Fig. 1A.

Fig. 3 is a functional block diagram showing a known circuit having closed loop dv/dt sensing and overcurrent protection.

Fig. 4A illustrates a circuit arrangement for controlling the switching di/dt and dv/dt according to an aspect of the present invention; Fig. 4B shows the turn-on waveforms of the power transistor of the circuit of Fig. 4A; and Fig. 4C shows the turn-off waveforms of the circuit of Fig. 4A.

Fig. 5A shows an example of an implementation of the clamp of the circuit of Fig. 4A; and Fig. 5B shows an example of an implementation of the detection and switching circuit of the circuit of Fig. 4A.

Fig. 6 illustrates a circuit arrangement for sensing switching di/dt according to another aspect of

the invention in which a known value of a wire bond inductance is used.

DETAILED DESCRIPTION OF THE INVENTION

Referring first to Fig. 4A, there is shown a circuit according to an aspect of the invention in which open loop control of the current and voltage wavefronts is provided. Here, a gate driver circuit 400, which may be an IC, controls the gate of power transistor 418 which, in turn, drives a load circuit (not shown). Though a power MOSFET is shown, the invention is also applicable to other MOS gate controlled devices such as IGBTs.

The gate driver circuit 400 includes a current generator circuit 411 which receives a gate drive signal V_{GATE} and supplies a gate drive current to the gate of MOSFET 418. The current generator circuit 411 charges or discharges the gate of the MOSFET 418 using one of two possible values of gate drive current which are determined by, in this example, di/dt control resistor 413 and dv/dt control resistor 414 which control the current and voltage waveforms, respectively. Specifically, the common terminal of the current generating circuit 411 is connected to a switch circuit which connects the common terminal of the current generating circuit 411 to one of the resistors 413 and 414 which are, in turn, connected to the source terminal of the MOSFET 418. A known switching circuit may be used here.

Initially, after the power transistor 418 has been turned off in a previous switching cycle and after the turn-off transient has passed, a low impedance short between the gate and the source of MOSFET 418 is provided

by turning on a hard clamp transistor 416 which rapidly discharges the gate-to-source capacitance. The subsequent switching transitions from one operating mode to the other are described below.

The turn-on sequence of the circuit is as follows:

First, the hard clamp is released by turning off MOSFET 416. Preferably, the MOSFET 418 is controlled by a D-type flip-flop 420, shown in Fig. 5A, which controls the clamp MOSFET as a function of the gate drive signal V_{GATE} .

The current generating circuit is then connected to the external di/dt control resistor 413. A first gate drive current, whose value is determined by the value of the di/dt control resistor 413, is supplied to the gate of MOSFET 418 from the current generator circuit 411. The desired current value is maintained over the operating temperature range as is compliance of the gate drive supply, as shown as intervals 1 and 2 in Fig. 4B. During this interval, the gate-to-source voltage and drain current ramp up to their maximum values in a manner similar to that shown in Fig. 1B but with the di/dt being controlled by resistor 413.

Once the gate-to-source voltage and drain current reach their maximum values, the supply voltage begins to fall. The resulting negative dv/dt is detected and triggers the output of a second value of the gate drive current by the current generator circuit 411 for providing dv/dt control, shown as intervals 3 and 4. The new value of the gate drive current is set by switching the terminal of circuit 411 from di/dt control resistor 413 to external dv/dt control resistor 414.

Preferably, the negative dv/dt is detected using a negative dv/dt detecting capacitor 417 and resistor 415, which may be coupled to a diode 420, which supply a negative dv/dt signal to an arrangement of D-type flip-flops 430 and 432, shown in Fig. 5B. The flip-flops 430 and 432 supply control signals which control the switching between resistors 413 and 414.

Then, the second current is turned off when the voltage supplied by the current generator 411 reaches the value of the gate supply voltage, namely at the limit of compliance of current generator, or at some other suitable predefined limit.

Advantageously, the circuit shown in Fig. 4A includes no feedback loops and operates without instability. The circuit also operates in a predetermined gate drive current mode in each of the intervals. Though the values of the preset resistances 413 and 414 are dependent upon the specific MOSFET device used and the load circuit being driven, the method is generally applicable to other load circuits. The transition from one mode to the next mode is triggered by the respective di/dt and dv/dt events of the circuit.

The turn-off sequence is now described as follows:

First, the gate of MOSFET 418 is discharged at a rate determined by the dv/dt control resistor 414, shown as intervals 1 and 2 in Fig. 4C. Here, the drain-to-source voltage and the drain current behave in a manner similar to that of intervals 1 and 2 of Fig. 1C, but the dv/dt is controlled by resistor 414.

Then, when the source-to-drain voltage across the power MOSFET 418 reaches the value of the supply voltage, the current output of the current generator 411

is changed to a second value by switching from external resistor 413 to external di/dt control resistor 413, as shown in intervals 3 and 4. During this interval, the di/dt of the drain current is controlled by the value of resistor 413.

Thereafter, when the gate voltage falls below the threshold voltage, the hard clamp transistor 416 is turned on.

In the above example, it is assumed that the values of di/dt and the dv/dt are the same at turn-on and at turn-off. However, different values may alternatively be assumed for the turn-on and turn-off di/dt , if necessary, to limit the reverse recovery of the diode.

It should also be noted that the current generator circuit 411 "sinks" the gate drive current during turn-off and sources the gate drive current during turn-on.

The invention is also applicable to providing closed loop control of the current and voltage waveforms, as described below

Closed loop control of current or voltage wavefronts requires the measurement of the di/dt or dv/dt . Measuring dv/dt is relatively simple and can be carried out using a small capacitance 417 that is connected to the drain of MOSFET 418 as described above and shown in Fig. 4A. Measuring the di/dt , however, typically required a more complex and expensive arrangement. When the value of the device current is used to operate the circuit, the same current feedback signal can also be used to control the current rise and fall times, namely the di/dt . When this signal is not available and the addition of a current feedback is not

justified, open loop methods are used in the manner described above.

According to another aspect of the invention, a simple lossless and inexpensive approach for sensing di/dt is provided by a hybrid circuit using a calibrated wire bond 540, 542, shown in Fig. 6. A bonding wire of predetermined length and diameter has a known value of inductance and will develop a voltage difference across it that is proportional to the value of di/dt .

Typically, a wire bond in a power hybrid device is 10 mm long and has an inductance of 5 to 10 nH, and when conducting a current having a di/dt of 0.1 to 0.5 A/ns, typically develops a 0.5V to 5V voltage difference across its length. This voltage difference can be supplied to di/dt feedback circuit 500 to control the current supplied to the gate of devices 508 and 526, which may be MOS-gated devices, to attain the desired di/dt using known feedback methods.

This same technique can be applied to a discrete device that is provided with a kelvin source or emitter connection. The voltage developed across the inductance of the source or emitter wire bond is sensed across the kelvin source wires, as shown in Fig. 6. Because the length of the bonding wire is controllable with very good accuracy by the manufacturing process, the di/dt can be measured with high accuracy.

The measured value of di/dt according to the invention can be used in conjunction with the previously described measured value of dv/dt to provide closed loop control using a circuit similar to that shown in Fig. 4A. However, the resistors 413 and 414 are replaced with an arrangement of operational amplifiers to control the

switching di/dt and dv/dt as a function of the measured values.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.



WHAT IS CLAIMED IS:

1. A control circuit for controlling the switching di/dt and switching dv/dt of a MOS gate controlled power device, said MOS gate controlled device providing a supply voltage to a load circuit; said control circuit comprising:

a current generator circuit having an output coupled to a gate terminal of said MOS gate controlled device for supplying a current to said gate terminal;

a first resistor having a first resistance and being coupled to a source terminal of said MOS gate controlled device;

a second resistor having a second resistance and coupled to said source terminal; and

a switching circuit for coupling a common terminal of said current generator circuit to a respective one of said first and second resistors for controlling the switching dv/dt and for coupling said common terminal to another of said first and second resistors for controlling the switching di/dt .

2. The circuit of claim 1, further comprising negative dv/dt detection circuit.

3. The circuit of claim 1, further comprising a clamp circuit coupled between said gate terminal and a source terminal of said MOS gate controlled device.

4. The circuit of claim 3, further comprising a clamp control circuit for controlling said clamp circuit as a function of an applied gate signal.

5. The circuit of claim 1, further comprising a switching circuit for controlling the coupling of said



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common terminal of said current generator circuit to said one of said resistors as a function of a detected negative dv/dt .

6. A method of controlling the switching di/dt and switching dv/dt of a MOS gate controlled device; said MOS gate controlled device controlling a supply voltage to a circuit; said method comprising the steps of:

- providing a current generator circuit for supplying a current to a gate of said MOS gate controlled power device;

- coupling a common terminal of said current generator circuit to a first resistor which is coupled to a source terminal of said MOS device for supplying a first current to said gate of said MOS gate controlled device and thereby controlling the switching dv/dt of said circuit;

- decoupling said current generator circuit from said first resistor and coupling said current generator circuit to a second resistor for supplying a second current to said gate and thereby controlling the switching di/dt of said circuit; and

- terminating the supply of said second current when said gate voltage reaches a predetermined value.

7. A method of controlling the switching di/dt and dv/dt of a MOS gate controlled device; said MOS gate controlled device controlling a supply voltage to a load circuit; said method comprising the steps of:

- discharging a gate terminal of said MOS gate controlled device by coupling a common terminal of a current generator circuit to a first resistor which is coupled to a source terminal of said MOS gate controlled device and thereby controlling the rate of discharge;



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decoupling said current generator circuit from said first resistor and coupling said current generator to a second resistor and thereby controlling said switching di/dt of said circuit; and

clamping said gate terminal when the voltage at said gate terminal is below a predetermined value.

8. The method of claim 6 or 7, further comprising the step of detecting a negative value of the switching dv/dt prior to decoupling said current generator circuit from said first resistor.

9. A control circuit for controlling the switching di/dt and the switching dv/dt of a MOS gate controlled device formed in a substrate, said MOS gate controlled device providing a supply voltage to a load circuit; said control circuit comprising:

a current generator circuit having an output coupled to a gate terminal of said MOS gate controlled device for supplying a current thereto;

a calibrated wire bond having a predetermined length and diameter and coupled to one of a source terminal and a drain terminal of said MOS gate controlled device; and

a feed back circuit for controlling the current supplied by said current generator circuit as a function of a value of the di/dt measured across said wire bond.

10. The method of claim 9 wherein the di/dt is measured by determining the voltage difference across the length of said calibrated wire bond.

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