

The invention relates to a method for the transmission and for the reception of information signals, in particular for the digital sound transmission via satellites, in accordance with the introductory part of Patent Claim 1.

In satellite stereo broadcasting it is known to transmit a plurality of different programmes via a transmission path, from which programmes can then be selectively chosen any one whatever on the receiver side. This transmission is effected, e.g. in time multiplex. In this case there are transmitted in each case within a so-called frame, i.e. a defined period of time, chronologically sequential bit words for the lefthand channel of the first programme, the righthand channel of the first programme, the lefthand channel of the second channel, the righthand channel of the second programme, the lefthand channel of the third programme and so on. After the termination of such a frame the sequential transmission begins again once more with the lefthand channel of the first programme and so on.

In the case of the digital information transmission via satellites there occur only statistically distributed single bit errors (Gaussian background noise), as is described in "British Telecommunications: OTS and Digital Television Transmission Investigations of Error Statistics Relevant to the Design of Error Correctors for Television (20.11.60)". The cyclic codes are to a great extent suitable for the correction of statistically distributed errors.

It has been proposed (DE-P 31 34 831 .9) to use a BCH code 63/44 for the recognition and correction of errors. With this code one can recognise with the help of a suitable decoder circuit, e.g. five errors, of which two errors can be corrected by the code. The three other recognised errors are interpolated by a suitable circuit.

In the case of phase difference modulation there result at the demodulator output predominantly double-bit errors which unduly limit the effectiveness of the error correction of block codes. Already three transmission errors are no longer recognised by this code in certain cases and two transmission errors cause an error recognition instead of a complete correction. As a result of the difference evaluation a bit adulterated on the transmission path leads in the demodulator to two incorrect statements: on the one hand this incorrect bit is referred to a preceding correct bit, and on the other hand the following correct bit is referred to this preceding incorrect bit.

It is the object of the invention, in the case of a method according to the introductory part of the Patent Claim 1, in particular in the case of the use of block code 63/44 and phase difference modulation, to improve the error recognition or correction.

The object is achieved by the invention given in Patent Claim 1.

Advantageous further developments of the invention are given in the subsidiary Claims.

The method in accordance with the invention is characterized in that, by spreading, the information bits of a first piece of information are separated by bits of other pieces of information. This is achieved in that the data sequences of two or more BCH blocks are interleaved with each other in the individual bit multiplex method. If there occur e.g. instead of single bit errors only double errors, hitherto only two double bit errors could be recognised in the method mentioned in the DE-P 31 34 831.9 and a double error could be corrected. In the case of spreading of two BCH blocks, whereby erroneous bits are distributed on both blocks, five double errors can be recognised and interpolated or two double errors can be corrected. In the case of this example a recognition of up to ten bits is possible.

An interleaving of the whole part frame (four BCH blocks) further increases the security against block errors. However, what is disadvantageous is an increased probability of hits of the errors occurring. The interleaving in each case of two BCH blocks therefore represents a favourable compromise solution.

A processing rate of the demodulator for a data rate of 10.24 MHz /s is necessary in the original frame without interleaving. In the case of interleaving of two BCH blocks the data rate drops to 5.12 MHz/s. Advantageously a demodulator can be constructed for half the processing rate in MOS technology.

It is proposed to transmit the digital signal to be transmitted in the form of 4-phase angular variations or differences of the carrier from the transmitter to the receiver. This is effected in such a way that a four-stage phase difference modulation is undertaken in the transmitter and a corresponding difference modulation is undertaken in the receiver, such as are described in "Nachrichtentechnische Zeitung (Communications technical Newspaper), 29 (1976), Volume 5, pages 390-294". An alternative demodulator concept in which this invention is likewise applicable uses coherent demodulation of differential decoding. This

system behaviour more favourable in the case of this method is paid for with a higher outlay.

In contrast to the fully coherent modulation, in which case the four meanings of the 4 phase-shift keying in the case of the demodulation has to be eliminated by circuit measures, as is proposed in DE-P 31 25 894.8, these four meanings are no longer present in the case of the phase difference modulation or decoding. The information lies in the difference of two bits following one after the other. Phase difference demodulation is particularly suitable in the case of digital sound transmission in the blanking interval of the television signal. Since the carrier does not have to be derived in the demodulator, in the television multiplex method with transmission of a digital television accompanying sound in the blanking interval in the differential modulation only the bit rate has to be derived from the signal. A continuous examination whether the received frame is correctly synchronised is dispensed with.

The invention will be described in more detail in the following by reference to an embodiment.

In the drawings:

Fig. 1 shows the construction of the interleaving of two BCH blocks,

Fig. 2 shows the construction of a part frame for the 4 phase-shift keying which frame is constructed as a half frame,

Fig. 3 shows a circuit proposal for the BCH block selection.

Fig. 1 shows the construction of an interleaving of two BCH blocks. In the case of 8 stereo channels in a part frame constructed as a half frame, the letter L characterizes a lefthand channel and a letter R a righthand channel of a stereo programme. L1 is e.g. the lefthand channel of a first stereo programme and R3 is the righthand channel of a third stereo programme. A scanning value consists of 14 bits, which are divided into 11 higher value bits, called MSB for short, and 3 lower value bits, called LSB for short. Each two stereo programmes are combined to form a BCH block. A first BCH block consists of the stereo programmes 1 and 2, a second BCH block of the stereo programmes 3 and 4. The first 22 bits are the MSB from L1 and L3. A first bit is bit number 1 of L1, a second bit is bit number 1 of L2, and then follows as third bit No.2 of L1, as fourth bit bit number 2 of L2 and so on. Then follow the 22 MSB from R2 and R4. 19 test bits F1-2 and F3-4 each belong to the two BCH blocks. They are connected to the 88 MSB from L1 to R4.

As is proposed in DE-PS 31 26 880.3 information bits in

the form of identification bits for programme type and programme number are present in the half frame. Each identification bit for a BCH block is connected to the test bits F1-2/F3-4 of the two BCH blocks in this frame in accordance with the invention. Behind these identification bits K1-2, K3-4 follow in all 24 LSB of the two BCH blocks, that is to say the LSB of L1/L3, then R1/R3, further L2/L4 and R2/R4.

This construction is then repeated immediately thereafter up to the end of the half frame for the stereo programmes 5 to 8, so that in all 2×152 bits are interleaved. 16 bits are reserved at the start of a half frame for a synchronous word and/or special services. In all this half frame has a length of 320 bits. The construction of the second half frame for the stereo programmes 9 to 16 is identical.

Fig. 2 shows a complete half frame for 4 phase-shift keying. The half frame begins with 16 non-interleaved bits S for synchronous word and/or special services. After that follows the bit sequences L1/L3 (MSB) to R2/R4 (LSB) shown in Fig. 1 and for the two BCH blocks with two identification bits K1 for programme selection or programme number. The following two interleaved BCH blocks for the stereo programmes 5 to 8 are likewise built up as in Fig. 1 with K2 as identification bit for these blocks.

Fig. 3 shows a circuit for a BCH block selection.

If a synchronous pulse is applied at the input 6 and a signal for the required BCH block is applied at the input 1 of a divider 5, a pulse T1 of 10.24 MHz is divided down to a pulse T2 of 5.12 MHz in this divider 5. At an input 3 of there is applied a frame bit sequence which is fed to an electronic switch 2. Then a required BCH block with a pulse rate of 5.12 MHz/s is blanked out of the frame bit sequence and fed to an output 4.

Patent Claims

1. A method for the transmission and for the reception of digital information signals, in particular for digital sound transmission of stereo- or mono channels of different programmes via satellites in which data sequences of digitised scanning values are arranged chronologically sequentially as 4 phase-shift keyed signals (4-PSK) in a frame formed from part frames, characterized in that an error correction system with block formation via two stereo channels or 4 mono channels is used and the data sequences in each part frame are interleaved by means of at least two blocks in the individual bit multiplex method, so that for each part frame two sequential bits of each scanning value are separated by a bit associated with another scanning value and, in the case of double bit errors, the erroneous bits are distributed in different blocks.
2. A method according to Claim 1, characterized in that the higher value bits (MSB) of each four scanning values are collected together in a cyclic block code.
3. A method according to Claim 1 or 2, characterized in that a bit sequence consists of a cyclic block code, the lower value bits belonging thereto and a bit for additional information.
4. A method according to Claim 3, characterized in that each two bit sequences are interleaved with each other in the individual bit multiplex method.
5. A method according to Claim 1, characterized in that the frame consists of two part frames with 320 bits each.
6. A method according to Claim 1 or 5, characterized in that a part frame contains 16 scanning values, which are assigned to 8 stereo channels or 16 mono channels or a combination of stereo- and mono channels.
7. A method according to Claim 6, characterized in that a scanning value consists of 14 bits which are divided up into 11 higher value bits (MSB) and three lower value bits (LSB).
8. A method according to Claim 1 or 2, characterized in that the first 16 bits of a part frame are reserved for special services and/or for a synchronous word.
9. A method according to Claim 5, characterized in that a 63-44 BCH code is used as cyclic block code.
10. A method according to Claim 1, characterized in that the digital information signals are transmitted



in the form of four phase angular variations or differences of the carrier from transmitter to receiver.

11. A method according to Claim 10, characterized in that there is undertaken in the receiver a phase difference modulation or a coherent demodulation with subsequent differential decoding of the received signal.

